

---

## Flash 8051 MCU

---

### DESCRIPTION

The CW89S52/54 series are 8-bit microcontroller with 8/16KB on-chip flash memory and 512B on-chip RAM. The devices use the 8051 instruction set and are pin-for-pin compatible with industry-standard 8051 microcontroller.

The CW89S52/54 also provides the following features: 32 I/O lines, Watchdog timer, two data pointers, three 16-bit timer/counters, a seven vector four-level interrupt architecture, a full duplex serial port, and clock circuitry. In addition, the CW89S5x is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes.

The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The device can address up to 64KB of external program memory and up to 64KB of external RAM.

### FEATURES

- 8051-Compatible Microcontroller
  - Software, Development Tool, Pin-to-Pin Package Compatible
- Wide Voltage Operation  $V_{CC} = 3V$  to  $5V$
- Operation speed:  $V_{CC} = 3V$  to  $5.5V$  and  $F = 0$  to  $24MHz$ ,  
 $V_{CC} = 4.5V$  to  $5.5V$  and  $F = 0$  to  $33MHz$
- 256 Byte Internal RAM, 256 Byte on-chip XRAM
- Flexible Flash
  - CW89S54 16KB; CW89S52 8KB
- Support External Address Range up to 64 KB of Program and Data Memory
- ISP available
- Three High-Current Port 1 Pins (16 mA each)
- Three 16-bit Timers/Counters
- Full-Duplex, Enhanced UART
  - Framing error detection
  - Automatic address recognition
- Eight Interrupt Sources at 4 Priority Levels
- Programmable Watchdog Timer (WDT)
- Four 8-bit I/O Ports (32 I/O Pins)
- Double DPTR Register
- Low EMI Mode (Inhibit ALE)
- 12 Clocks or 6 clocks Per Cycle
- TTL- and CMOS-Compatible Logic Levels
- Low Power Modes
  - Power-down Mode with External Interrupt Wake-up
  - Idle Mode
- Selectable Operation Clock
  - Divide to 1/4, 1/16, 1/256, or 1/1024th
- Temperature Ranges:  $-40^{\circ}C$  to  $+85^{\circ}C$
- Packages Available
  - 40-pin PDIP、44-pin TQFP、44-pin PLCC, 44-pin LQFP, All Pb-free



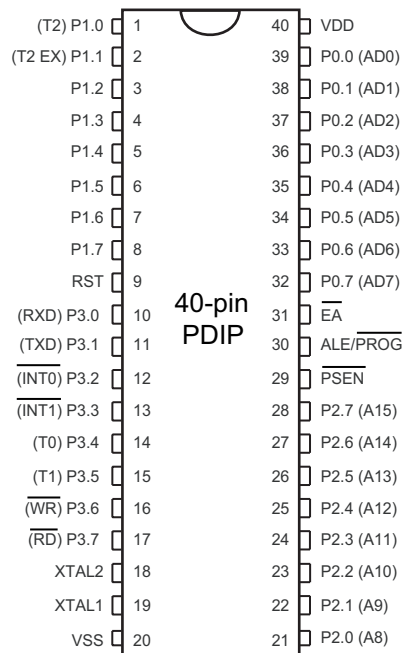
## APPLICATIONS

- Industrial control
- Building and security
- Small Appliances
- Consumer Product

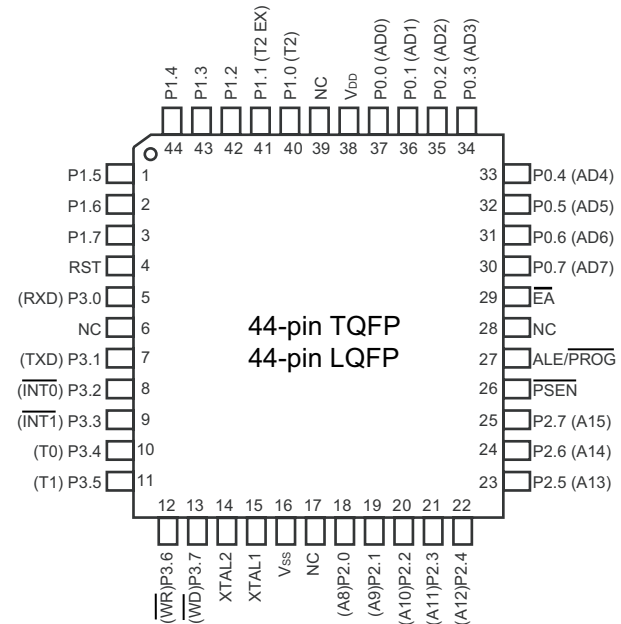
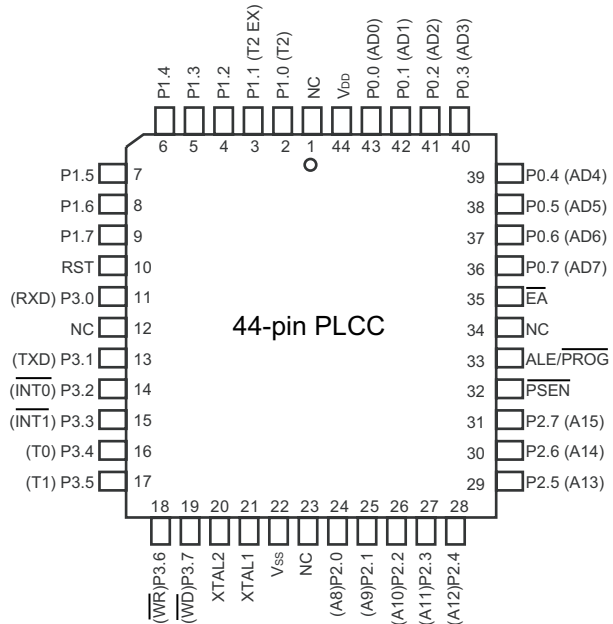
## ORDERING INFORMATION

Temperature Range	Package	Orderable Device	Package Qty.
-40°C to +85°C	PLCC	CW89S52-44N	27Units/Tube
		CW89S54-44N	
	PDIP	CW89S52-40P	9Units/Tube
		CW89S54-40P	
	TQFP	CW89S52-44T	96Units/Tray
		CW89S54-44T	
	LQFP	CW89S52-44L	160Units/Tray
		CW89S54-44L	

## PIN CONFIGURATION



PIN CONFIGURATION(CONTINUED)



BLOCK DIAGRAM

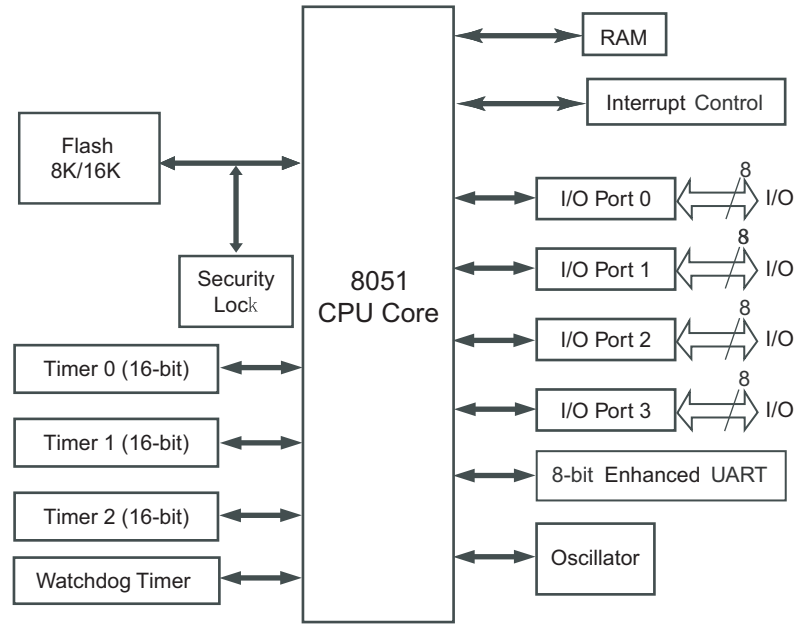


Figure 1. Block Diagram



**PIN DESCRIPTION**

Pin No.			Name	Type	Function Description
PLCC	DIP	(L)TQFP			
2	1	40	P1.0	I/O with internal pull-up	T2: External count input to Timer/Counter 2 or Clock out from Timer/Counter 2
3	2	41	P1.1		T2EX: Timer/Counter 2 capture/reload trigger & direction control
4	3	42	P1.2		-
5	4	43	P1.3		-
6	5	44	P1.4		-
7	6	1	P1.5		-
8	7	2	P1.6		-
9	8	3	P1.7		-
10	9	4	RST	I	While the oscillator is running, a high on the pin for two machine cycles will reset the device.
11	10	5	P3.0	I	RXD: UART Receive input
13	11	7	P3.1	O	TXD: UART Transmit output
14	12	8	P3.2	I	INT0: External Interrupt Input
15	13	9	P3.3	I	INT1: External Interrupt Input
16	14	10	P3.4	I	T0: External count input to Timer/Counter 0
17	15	11	P3.5	I	T1: External count input to Timer/Counter 1
18	16	12	P3.6	O	WR: External Data Memory Write strobe
19	17	13	P3.7	O	RD: External Data Memory Read strobe
20	18	14	XTAL2	O	Output from the inverting oscillator amplifier.
21	19	15	XTAL1	I	Input to the inverting oscillator amplifier and to the internal clock
22	20	16	V <sub>SS</sub>	I	Ground



PIN DESCRIPTION(CONTINUED)

Pin No.			Name	Type	Function Description	
PLCC	DIP	(L)TQFP			main	Alternate
24	21	18	P2.0	I/O with internal pull-up	8-bit bi-directional I/O port with internal pull-ups. Port 2 pins are pulled high by the internal pull-ups when '1's are written to them and can be used as inputs in this state.	Port 2 sends the high-order address during fetches from external program memory and during accesses to external Data Memory that use 16-bit address. In this application, it uses strong internal pull-ups when transiting to '1's.
25	22	19	P2.1			
26	23	20	P2.2			
27	24	21	P2.3			
28	25	22	P2.4			
29	26	23	P2.5			
30	27	24	P2.6			
31	28	25	P2.7			
32	29	26	$\overline{\text{PSEN}}$	I/O	Program Store Enable: it is the Read strobe to external program. When the device is executing from internal program memory, it is inactive (High). When the device is executing code from external program memory, it is activated twice each machine cycle.	
33	30	27	$\overline{\text{ALE/PROG}}$	I/O	Address Latch Enable: ALE is the output signal for latching the low byte of the address during an access to external memory. This pin is also the programming pulse input ( $\overline{\text{PROG}}$ ) for flash programming. Normally the ALE is emitted at a constant rate of 1/6 the crystal frequency. However, if AO is set to 1, ALE is disabled.	
35	31	29	$\overline{\text{EA}}$	I	External Access Enable: $\overline{\text{EA}}$ must be connected to V <sub>SS</sub> for external program execution, and to V <sub>DD</sub> for internal program execution.	
36	32	30	P0.7	I/O	8-bit open drain bidirectional I/O port. As an output port each pin can sink several LS TTL inputs. Port 0 pins that have '1's written to them float, and in this state can be used as high-impedance inputs. External pull-ups are required as a general purpose I/O port.	Port 0 is the multiplexed low-order address and data bus during accesses to external code and data memory. In this application, it uses strong internal pull-ups when transitioning to '1's.
37	33	31	P0.6			
38	34	32	P0.5			
39	35	33	P0.4			
40	36	34	P0.3			
41	37	35	P0.2			
42	38	36	P0.1			
43	39	37	P0.0			
44	40	38	V <sub>DD</sub>	I	Power Supply	



**PIN DESCRIPTION(CONTINUED)**

Pin No.			Name	Type	Function Description	
PLCC	DIP	(L)tQFP			main	Alternate
1	-	6	NC		No Internal Connect	
12		17				
23		28				
34		39				

**Note 1:** It is not necessary to receive a 12V programming voltage during flash programming.

**Note 2:** ALE loading issue: When ALE pin experiences higher loading (>30pf) during the reset, the MCU may accidentally enter into modes other than normal working mode. The solution is to add a pull-up resistor of 3~50 kΩ to V<sub>DD</sub> for ALE pin.

**Note 3:** For 6 clock mode, ALE is emitted at 1/3 of crystal frequency.

**MEMORY ORGANIZATION**

The device has separate address spaces for program and data memory.

**Program Flash Memory**

There is an internal flash memory in the device. The flash memory has 8/16KByte, is organized as 2/4 pages, each page consists of 4KBytes.

**Data RAM Memory**

The data RAM has 512 Bytes on-chip memory. The first 256 Bytes are on-chip RAM and available by default. The second 256 Bytes are on-chip XRAM and enabled by clearing the EXTRAM bit in the AUXR register. The RAM can be addressed up to 64KB for external data memory.

**Expanded Data RAM Addressing**

The CW89S5x have the capability of 512 Bytes of RAM. See Figure 2.

The device has four sections of internal data memory:

1. The lower 128 Bytes of RAM (00H to 7FH) are directly and indirectly addressable.
2. The higher 128 Bytes of RAM (80H to FFH) are indirectly addressable.
3. The special function registers (80H to FFH) are directly addressable only.
4. The expanded RAM of 256 Bytes (00H to FFH) is indirectly addressable by the move external instruction (MOVX) and clearing the EXTRAM bit.

Since the upper 128 bytes occupy the same addresses as the SFRs, the RAM must be accessed indirectly. The RAM and SFRs space are physically separate even though they have the same addresses.



When instructions access addresses in the upper 128 bytes (above 7FH), the MCU determines whether to access the SFRs or RAM by the type of instruction given. If it is indirect, then RAM is accessed. If it is direct, then an SFR is accessed.

To access the expanded RAM, the EXTRAM bit must be cleared and MOVX instructions must be used. The extra 256 Bytes of memory is physically located on the chip and logically occupies the first 256 bytes of external memory (addresses 000H to FFH).

When EXTRAM = 0, the expanded RAM is indirectly addressed using the MOVX instruction in combination with any of the registers R0, R1 or DPTR. Accessing the expanded RAM does not affect ports P0, P3.6 ( $\overline{WR}$ ), P3.7 ( $\overline{RD}$ ), or P2. Access to external memory higher than FFH using the MOVX instruction will access external memory (0100H to FFFFH) and will perform in the same way as the standard 8051, with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals.

When EXTRAM = 1, MOVX @Ri and MOVX @DPTR will be similar to the standard 8051. Using MOVX @Ri provides an 8-bit address with multiplexed data on Port 0. Other output port pins can be used to output higher order address bits. This provides external paging capabilities. Using MOVX @DPTR generates a 16-bit address. This allows external addressing up to 64K. Port 2 provides the high-order eight address bits (DPH), and Port 0 multiplexes the low order eight address bits (DPL) with data. Both MOVX @Ri and MOVX @DPTR generates the necessary read and write signals (P3.6 -  $\overline{WR}$  and P3.7 -  $\overline{RD}$ ) for external memory use.

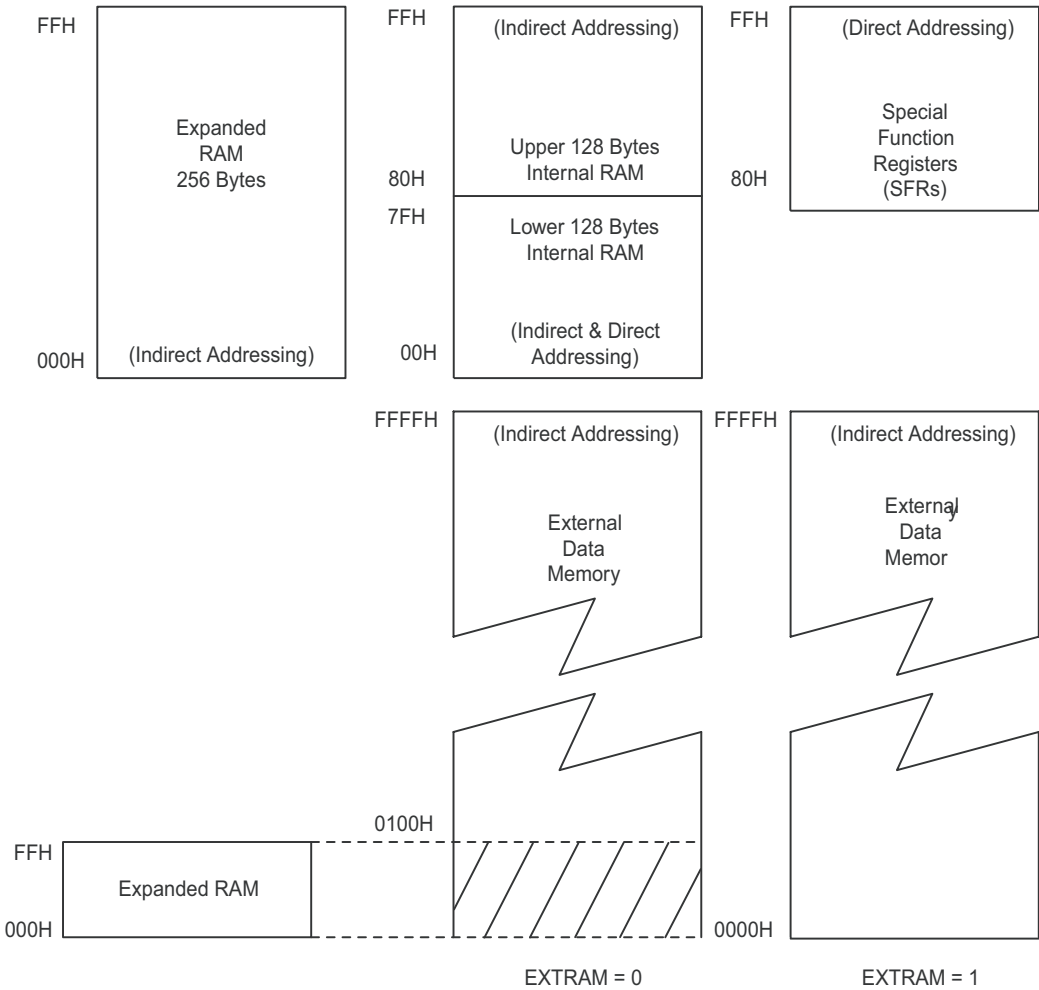
External Data Memory  $\overline{RD}$ ,  $\overline{WR}$  with EXTRAM bit

	MOVX @DPTR, A or MOVX A, @DPTR		MOVX @Ri, A or MOVX A, @Ri
AUXR	ADDR < 0100H	ADDR >= 0100H	ADDR = Any
EXTRAM = 0	$\overline{RD}/\overline{WR}$ not asserted	$\overline{RD}/\overline{WR}$ asserted	$\overline{RD}/\overline{WR}$ not asserted
EXTRAM = 1	$\overline{RD}/\overline{WR}$ asserted	$\overline{RD}/\overline{WR}$ asserted	$\overline{RD}/\overline{WR}$ asserted

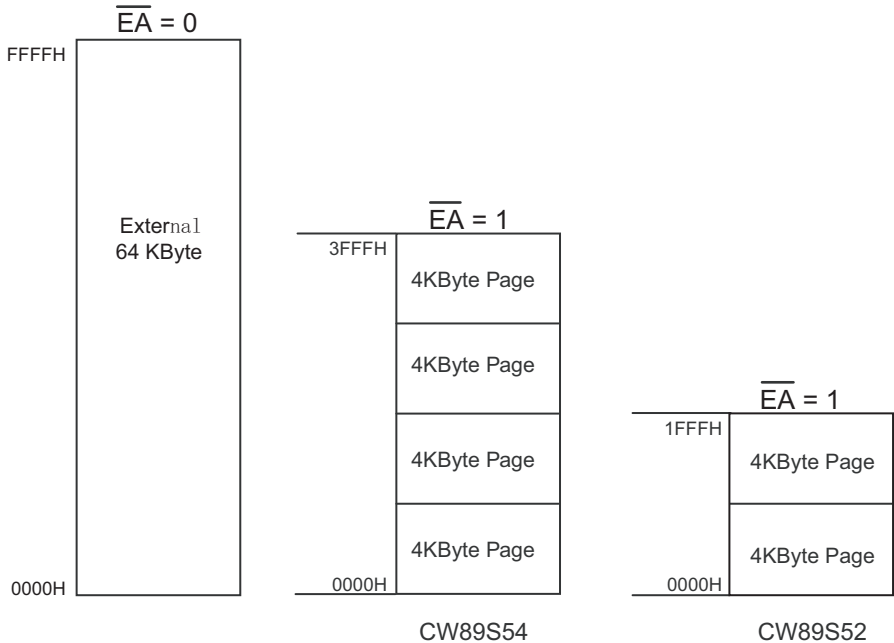
The stack pointer (SP) can be located anywhere within the 256 bytes of internal RAM (lower 128 bytes and upper 128 bytes). The stack pointer may not be located in any part of the expanded RAM.



**Expanded Data RAM Addressing(CONTINUED)**



**Figure 2. Internal and External Data Memory Structure**



**Figure 3. Program Memory structure**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on $\overline{EA}$ Pin to $V_{SS}$	$V_{EA}$	-0.5 to +14.0	V
DC Voltage on Any Pin to Ground	$V_{PIN}$	-0.5 to $V_{DD}+0.5$	V
Transient Voltage (<20ns) on Any Other Pin to $V_{SS}$		-1.0 to $V_{DD}+1.0$	V
Maximum Current per I/O Pins P1.5, P1.6, P1.7	$I_{OL}$	20	mA
Maximum Current per I/O for All Other Pins	$I_{OL}$	15	mA
Power Dissipation ( $T_A=25^\circ\text{C}$ )		1.5	W
Storage Temperature		-65 to +150	$^\circ\text{C}$
Through Hole Lead Soldering Temperature (10 Seconds)		300	$^\circ\text{C}$
Surface Mount Solder Reflow Temperature (10 sec)		260	$^\circ\text{C}$
Output Short Circuit Current		50	mA

**Note 1:** Applied conditions greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2:** All packages are  $260^\circ\text{C}$  capable in all solder versions.

**Note 3:** Outputs shorted for no more than one second. No more than one output shorted at a time.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{DD}$	4.5	5.5	V
Oscillator Frequency	$f_{OSC}$	0	33	MHz
Operating Ambient Temperature	$T_A$	-40	+85	$^\circ\text{C}$

**RELIABILITY CHARACTERISTICS**

Parameter	Symbol	Test Method	Min	Unit
Endurance	$N_{END}$	JEDEC Standard A117	10,000	Cycles
Data Retention	$T_{DR}$	JEDEC Standard A103	100	Years
Latch Up	$I_{LTH}$	JEDEC Standard 78	$100 + I_{DD}$	mA

**RECOMMENDED SYSTEM POWER-UP TIMINGS**

Parameter	Symbol	Min	Unit
Power-up to Read Operation	$T_{PU-READ}$	100	$\mu\text{s}$
Power-up to Write Operation	$T_{PU-WRITE}$	100	$\mu\text{s}$

**PIN IMPEDANCE**

( $T_A=25^\circ\text{C}$ ,  $f=1\text{ Mhz}$ , other pins open)

Parameter	Symbol	Test Conditions	Max	Unit
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	15	pF
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{V}$	12	pF
Pin Inductance	$L_{PIN}$		20	nH



**DC ELECTRICAL CHARACTERISTICS**

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ;  $V_{DD} = 3.0\sim 5.5\text{V}$ ;  $V_{SS} = 0\text{V}$ )

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Low Voltage	$V_{IL}$		-0.5	$0.2 V_{CC} - 0.1$	V
Input High Voltage except RST, XTAL1	$V_{IH}$		$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
Input High Voltage RST, XTAL1	$V_{IH1}^8$		$0.7 V_{CC}$	$V_{CC} + 0.5$	V
Output Low Voltage, (ports 1, 2, 3, 4) <sup>5</sup>	$V_{OL}$	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ $I_{OL} = 100\ \mu\text{A}^4$ $I_{OL} = 1.6\ \text{mA}^1$ $I_{OL} = 3.5\ \text{mA}^4$		0.3 0.45 1.0	V
		$V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ $I_{OL} = 0.8\ \text{mA}^4$		0.45	
Output Low Voltage, (port 0, ALE, $\overline{\text{PSEN}}$ ) <sup>5</sup>	$V_{OL1}$	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$ $I_{OL} = 200\ \mu\text{A}^4$ $I_{OL} = 3.2\ \text{mA}^4$ $I_{OL} = 7.0\ \text{mA}^4$		0.3 0.45 1.0	V
		$V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ $I_{OL} = 1.6\ \text{mA}^4$		0.45	
Output High Voltage, (ports 1, 2, 3, 4)	$V_{OH}$	$V_{CC} = 5\text{V} \pm 10\%$ $I_{OH} = -10\ \mu\text{A}$ $I_{OH} = -30\ \mu\text{A}$ $I_{OH} = -60\ \mu\text{A}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V
		$V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ $I_{OH} = -10\ \mu\text{A}$	$0.9 V_{CC}$		
Output High Voltage, (port 0, ALE, $\overline{\text{PSEN}}$ )	$V_{OH1}$	$V_{CC} = 5\text{V} \pm 10\%$ $I_{OH} = -200\ \mu\text{A}$ $I_{OH} = -3.2\ \text{mA}$ $I_{OH} = -7.0\ \text{mA}$	$V_{CC} - 0.3$ $V_{CC} - 0.7$ $V_{CC} - 1.5$		V
		$V_{CC} = 3.0\text{V}$ to $5.5\text{V}$ $I_{OH} = -10\ \mu\text{A}$	$0.9 V_{CC}$		
RST Pulldown Resistor	$R_{RST}$			250	k $\Omega$
Logical 0 Input Current (ports 1, 2, 3, 4 and 5)	$I_{IL}$	$V_{IN} = 0.45\text{V}$		-50	$\mu\text{A}$
Input Leakage Current for P0 only	$I_{LI}$	$0.45\text{V} < V_{IN} < V_{CC}$		$\pm 10$	$\mu\text{A}$
Logical 1 to 0 Transition Current, (ports 1, 2, 3, 4)	$I_{TL}$	$V_{IN} = 2.0\text{V}$		-650	$\mu\text{A}$
Capacitance of I/O Buffer	$C_{IO}$	$F_C = 3\ \text{MHz}$ $T_A = 25^{\circ}\text{C}$		10	pF
Power Down Current	$I_{PD}$	$4.5\text{V} < V_{CC} < 5.5\text{V}^3$		150	$\mu\text{A}$



**DC ELECTRICAL CHARACTERISTICS(CONTINUED)**

Parameter	Symbol	Test Conditions	Min	Max	Unit
Power Supply Current on normal mode	I <sub>CCOP</sub>	V <sub>CC</sub> = 5.5V <sup>1</sup>		0.4 x Frequency (MHz) + 5	mA
Power Supply Current on idle mode	I <sub>CCIDLE</sub>	V <sub>CC</sub> = 5.5V <sup>1</sup>		0.3 x Frequency (MHz) + 5	mA
Power Supply Current during flash Write / Erase	I <sub>CCProg</sub>	V <sub>CC</sub> = 5.5V <sup>6</sup>			mA

**Note 1:** Operating I<sub>CC</sub> is measured with all output pins disconnected; XTAL1 driven with T<sub>CLCH</sub>, T<sub>CHCL</sub> = 5 ns (see Figure 7.), V<sub>IL</sub> = V<sub>SS</sub> + 0.5V, V<sub>IH</sub> = V<sub>CC</sub> - 0.5V; XTAL2 N.C.; EA = RST = Port 0 = V<sub>CC</sub>. I<sub>CC</sub> would be slightly higher if a crystal oscillator used (see Figure 12).

**Note 2:** Idle I<sub>CC</sub> is measured with all output pins disconnected; XTAL1 driven with T<sub>CLCH</sub>, T<sub>CHCL</sub> = 5 ns, V<sub>IL</sub> = V<sub>SS</sub> + 0.5V, V<sub>IH</sub> = V<sub>CC</sub> - 0.5V; XTAL2 N.C.; Port 0 = V<sub>CC</sub>; EA = RST = V<sub>SS</sub> (see Figure 13).

**Note 3:** Power Down I<sub>CC</sub> is measured with all output pins disconnected; EA = V<sub>SS</sub>, PORT 0 = V<sub>CC</sub>; XTAL2 NC.; RST = V<sub>SS</sub> (see Figure 14).

**Note 4:** Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V<sub>OLS</sub> of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V<sub>OL</sub> peak 0.6V. A Schmitt Trigger use is not necessary.

**Note 5:** Under steady state (non-transient) conditions, I<sub>OL</sub> must be externally limited as follows: Maximum I<sub>OL</sub> per port pin: 15mA; Maximum I<sub>OL</sub> per 8-bit port: 26mA; Maximum I<sub>OL</sub> total for all outputs: 71mA. If I<sub>OL</sub> exceeds the test condition, V<sub>OL</sub> may exceed the related specific- ation. Pins are not guaranteed to sink current greater than the listed test conditions.

**Note 6:** I<sub>CC</sub> Flash Write operation current while an on-chip flash page write is on going.

**Note 7:** Flash Retention is guaranteed with the same formula for V<sub>CC</sub> Min down to 0.



**AC ELECTRICAL CHARACTERISTICS**

(Load Capacitance for Port 0, ALE, and PSEN = 100pF; for All Other Outputs = 80pF.  
Input Rise/Fall Time = 10ns. T = -40°C to +85°C, V<sub>DD</sub> = 4.5~5.5V@33MHz, V<sub>SS</sub> = 0V)

Parameter	Symbol	25MHz(x1Mode) 12MHz(x2Mode) <sup>1</sup>		33MHz(x1Mode) 16MHz(x2Mode) <sup>1</sup>		Variable Oscillator		Unit
		Min	Max	Min	Max	Min	Max	
x1 Mode Oscillator Freq.	1/T <sub>CLCL</sub>	0	25	0	33	0		MHz
x2 Mode Oscillator Freq.	1/2T <sub>CLCL</sub>	0	12	0	16	0		MHz
ALE Pulse Width	T <sub>LHLL</sub>	65		46		2T <sub>CLCL</sub> -15		ns
Address Valid to ALE Low	T <sub>AVLL</sub>			15		T <sub>CLCL</sub> -15		ns
Address Hold After ALE Low	T <sub>LLAX</sub>			15		T <sub>CLCL</sub> -15		ns
ALE Low to Valid Instr. In	T <sub>LLIV</sub>				66		4T <sub>CLCL</sub> - 45	ns
ALE Low to PSEN Low	T <sub>LLPL</sub>			15		T <sub>CLCL</sub> -15		ns
PSEN Pulse Width	T <sub>PLPH</sub>			76		3T <sub>CLCL</sub> -15		ns
PSEN Low to Valid Instr. In	T <sub>PLIV</sub>				41		3T <sub>CLCL</sub> - 50	ns
Input Instr. Hold After PSEN	T <sub>PXIX</sub>					0		ns
Input Instr. Float After PSEN	T <sub>PXIZ</sub>				15		T <sub>CLCL</sub> - 15	ns
PSEN to Address valid	T <sub>PXAV</sub>	32		22		T <sub>CLCL</sub> - 8		ns
Address to Valid Instr. In	T <sub>AVIV</sub>				92		5T <sub>CLCL</sub> - 60	ns
PSEN Low to Address Float	T <sub>PLAZ</sub>		10		10		10	ns
RD Pulse Width	T <sub>RLRH</sub>			152		6T <sub>CLCL</sub> - 30		ns
Write Pulse Width (WE)	T <sub>WLWH</sub>			152		6T <sub>CLCL</sub> - 30		ns
RD Low to Valid Data In	T <sub>RLDV</sub>				102		5T <sub>CLCL</sub> - 50	ns
Data Hold After RD	T <sub>RHDX</sub>	0		0		0		ns
Data Float After RD	T <sub>RHDZ</sub>				49		2T <sub>CLCL</sub> - 12	ns
ALE Low to Valid Data In	T <sub>LLDV</sub>				192		8T <sub>CLCL</sub> - 50	ns
Address to Valid Data In	T <sub>AVDV</sub>				198		9T <sub>CLCL</sub> - 75	ns
ALE Low to RD or WR Low	T <sub>LLWL</sub>			76	106	3T <sub>CLCL</sub> - 15	3T <sub>CLCL</sub> + 15	ns
Address to RD or WR Low	T <sub>AVWL</sub>			91		4T <sub>CLCL</sub> - 30		ns



**AC ELECTRICAL CHARACTERISTICS(CONTINUED)**

Parameter	Symbol	25MHz(x1Mode) 12MHz(x2Mode) <sup>1</sup>		33MHz(x1Mode) 16MHz(x2Mode) <sup>1</sup>		Variable Oscillator		Unit
		Min	Max	Min	Max	Min	Max	
Data Valid to WR High to	T <sub>QVWX</sub>		20		10	T <sub>CLCL</sub> - 20		ns
Low Transition Data Hold After WR	T <sub>WHQX</sub>			10		T <sub>CLCL</sub> - 20		ns
Data Valid to WR High	T <sub>QVWH</sub>			162		7T <sub>CLCL</sub> - 50		ns
RD Low to Address Float	T <sub>RLAZ</sub>		0		0		0	ns
RD or WR High to ALE High	T <sub>WHLH</sub>			15	45	T <sub>CLCL</sub> - 15	T <sub>CLCL</sub> + 15	ns

**Note: 1.** Calculated values are for x1 Mode only.

Description of Symbols:

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

- |  |                                  |
|--|----------------------------------|
| A: Address                               | Q: Output data                   |
| C: Clock                                 | R: RD signal                     |
| D: Input Data                            | T: Time                          |
| H: Logic level HIGH                      | V: Valid                         |
| I: Instruction (program memory contents) | W: WR signal                     |
| L: Logic level LOW or ALE                | X: No longer a valid logic level |
| P: PSEN                                  | Z: High Impedance (Float)        |

For example:

T<sub>AVLL</sub> = Time from Address Valid to ALE Low

T<sub>LLPL</sub> = Time from ALE Low to PSEN Low



AC ELECTRICAL CHARACTERISTICS(CONTINUED)

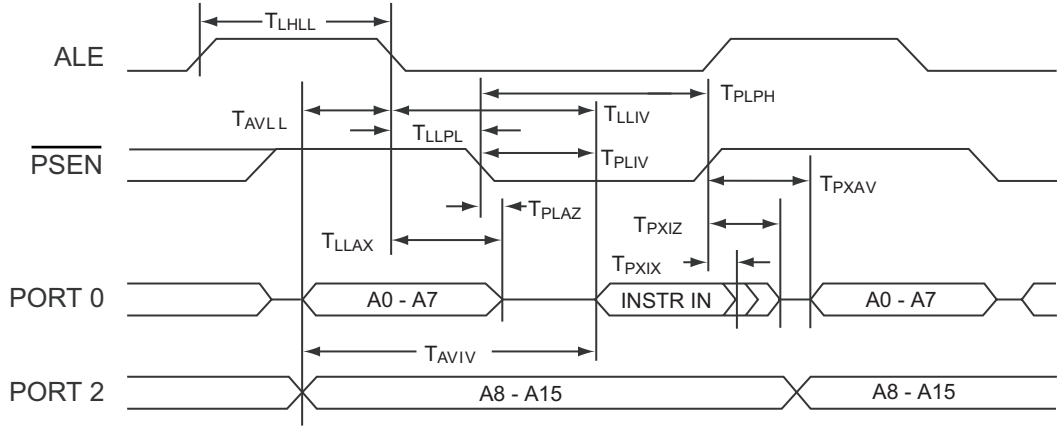


Figure 4. External Program Memory Read Cycle

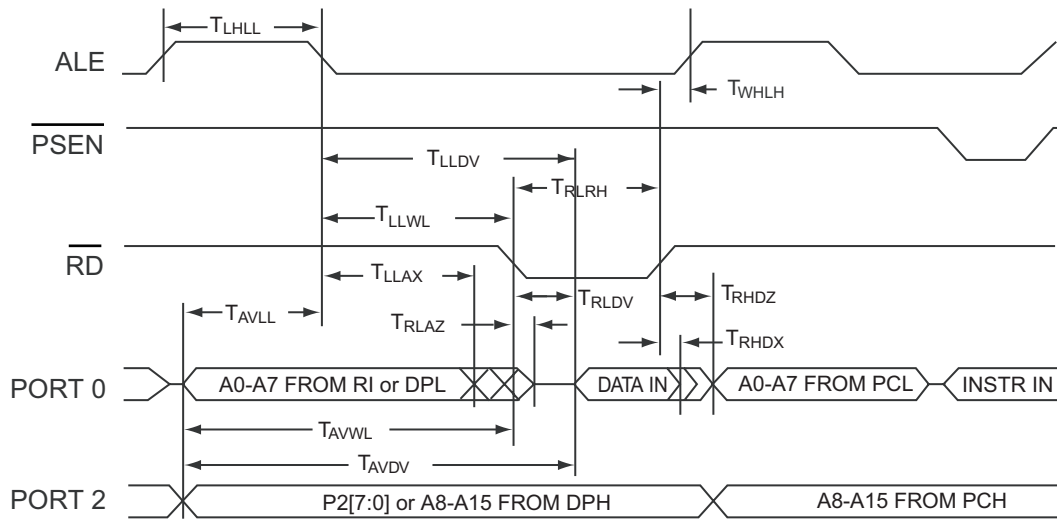


Figure 5. External Data Memory Read Cycle

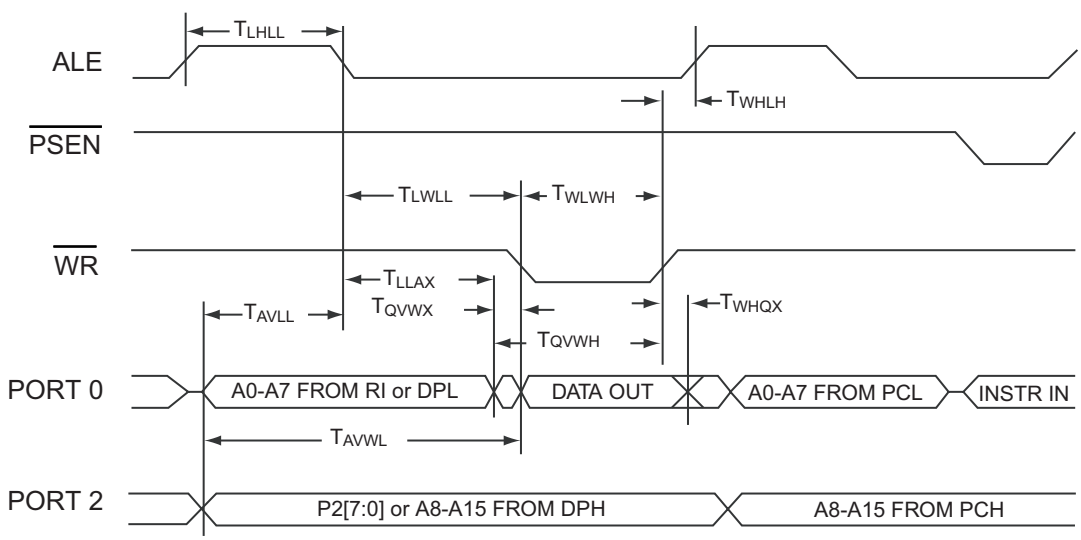


Figure 6. External Data Memory Write Cycle



**EXTERNAL CLOCK DRIVE**

Parameter	Symbol	12 MHz		33 MHz		Variable		Unit
		Min	Max	Min	Max	Min	Max	
Oscillator Frequency	$1/T_{CLCL}$					0	40	MHz
Clock Period	$T_{CLCL}$	83		30.3				ns
High Time	$T_{CHCX}$			10.6		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
Low Time	$T_{CLCX}$			10.6		$0.35T_{CLCL}$	$0.65T_{CLCL}$	ns
Rise Time	$T_{CLCH}$		20		10			ns
Fall Time	$T_{CHCL}$		20		10			ns

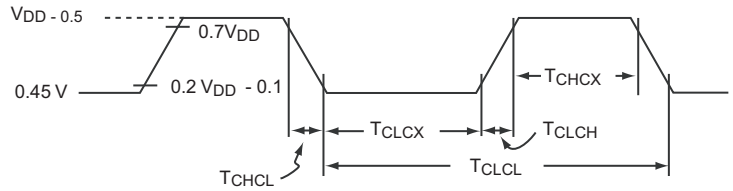


Figure 7. External Clock Drive Waveform

**SERIAL PORT TIMING**

Parameter	Symbol	12MHz		33MHz		Variable		Unit
		Min	Max	Min	Max	Min	Max	
Serial Port Clock Cycle Time	$T_{XLXL}$	1.0		0.364		$12T_{CLCL}$		$\mu$ s
Output Data Setup to Clock Rising Edge	$T_{QVXH}$	700		170		$10T_{CLCL} - 133$		ns
Output Data Hold After Clock Rising Edge	$T_{XHGX}$	50				$2T_{CLCL} - 117$		ns
				11		$2T_{CLCL} - 50$		ns
Input Data Hold After Clock Rising Edge	$T_{XHDX}$	0		0		0		ns
Clock Rising Edge to Input Data Valid	$T_{XHDX}$		700		170		$10T_{CLCL} - 133$	ns

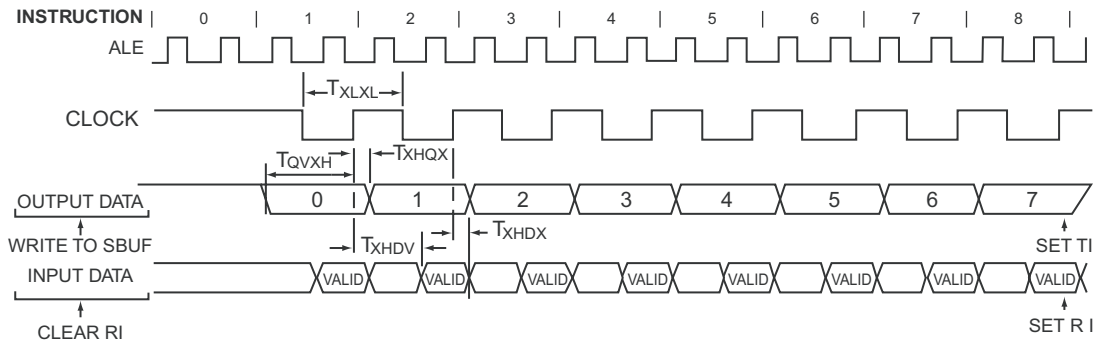
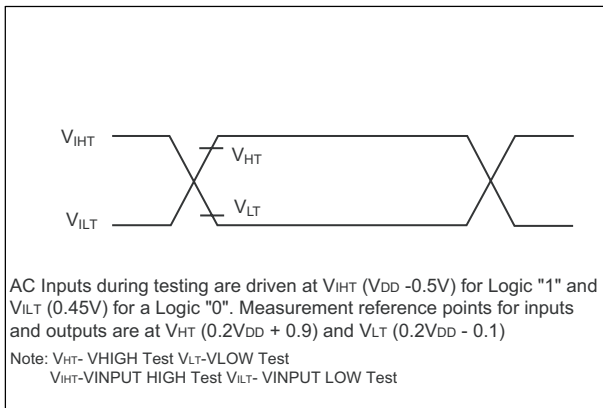


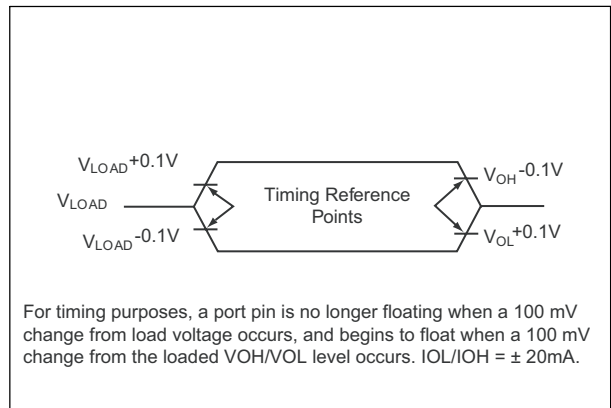
Figure 8. Shift Register Mode Timing Waveforms



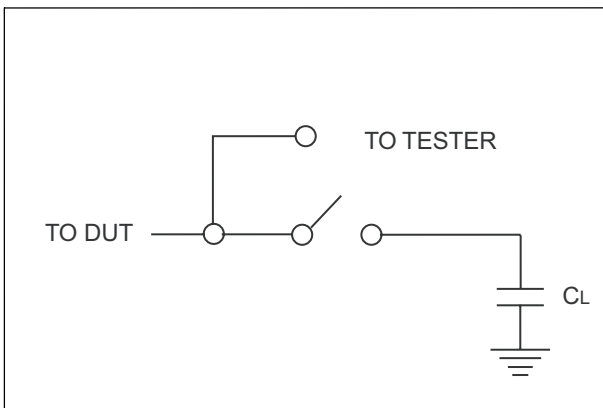
**SERIAL PORT TIMING(CONTINUED)**



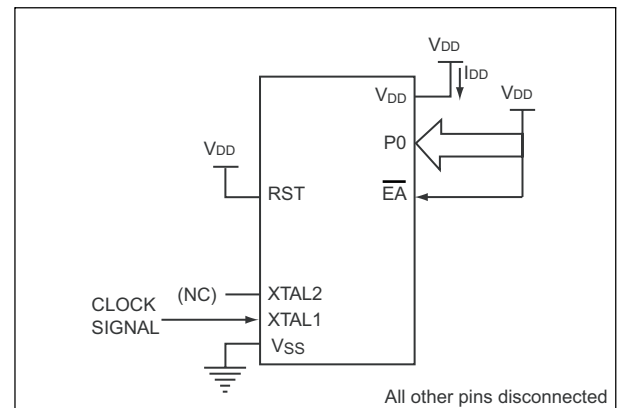
**Figure 9. AC Testing Input/Output Waveform**



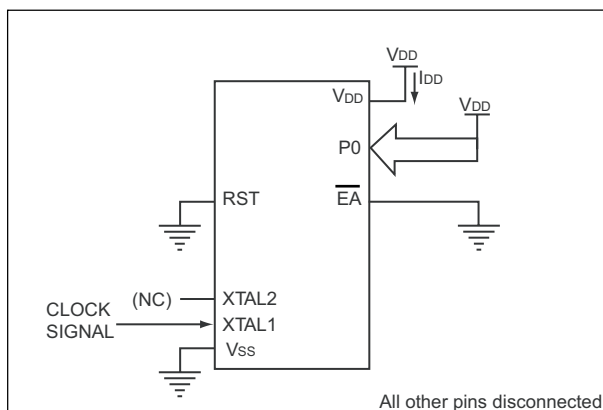
**Figure 10. Float Waveform**



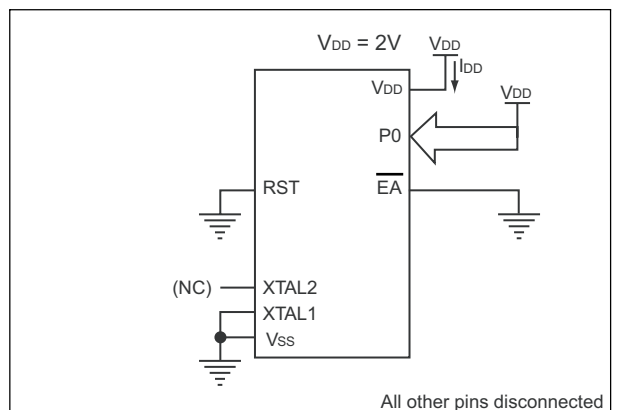
**Figure 11. A Test Load Example**



**Figure 12. I<sub>DD</sub> Test Condition, Active Mode**



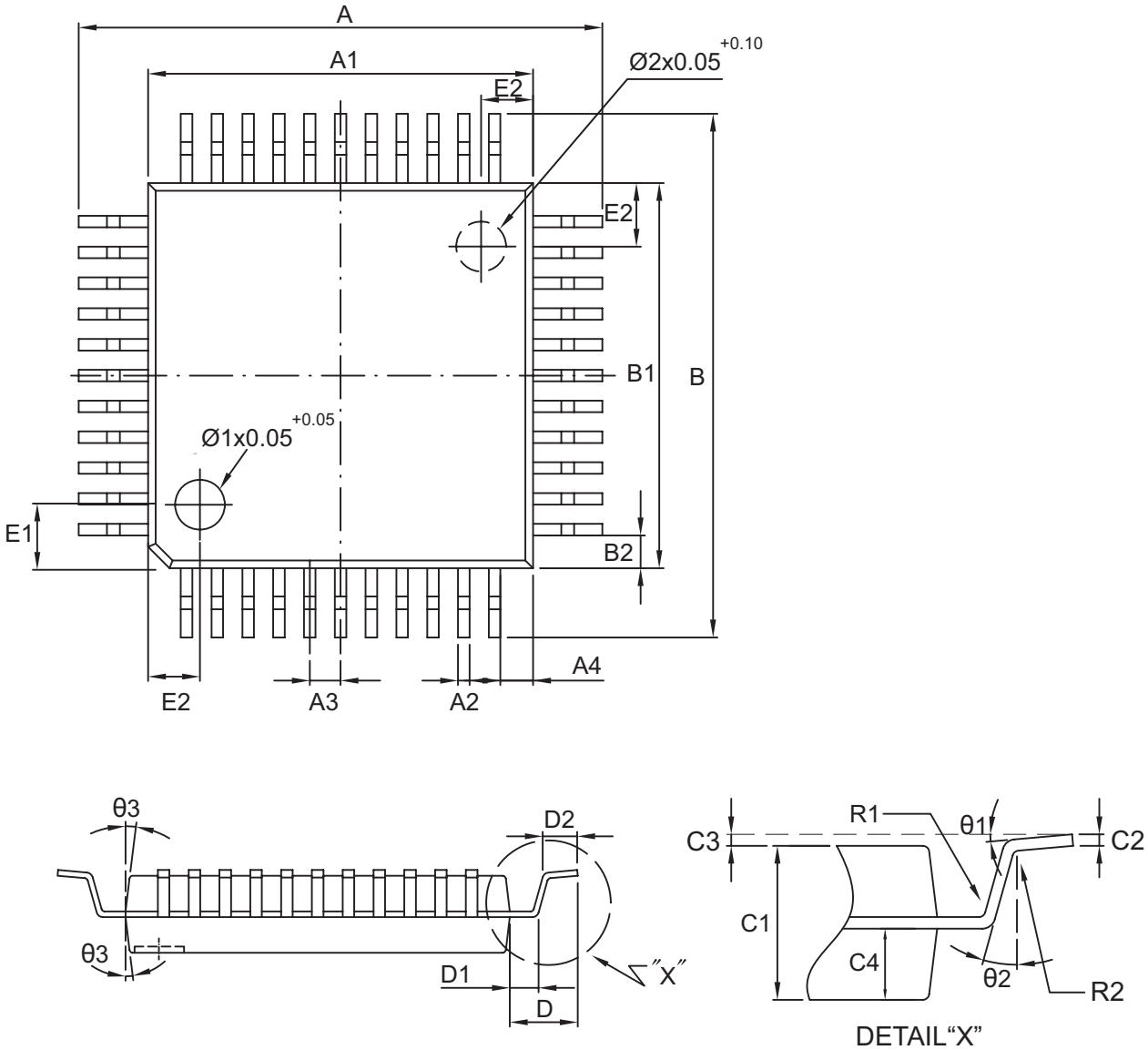
**Figure 13. I<sub>DD</sub> Test Condition, Idle Mode**



**Figure 14. I<sub>DD</sub> Test Condition, Power-down Mode**

**PHYSICAL DIMENSIONS**

QFP44

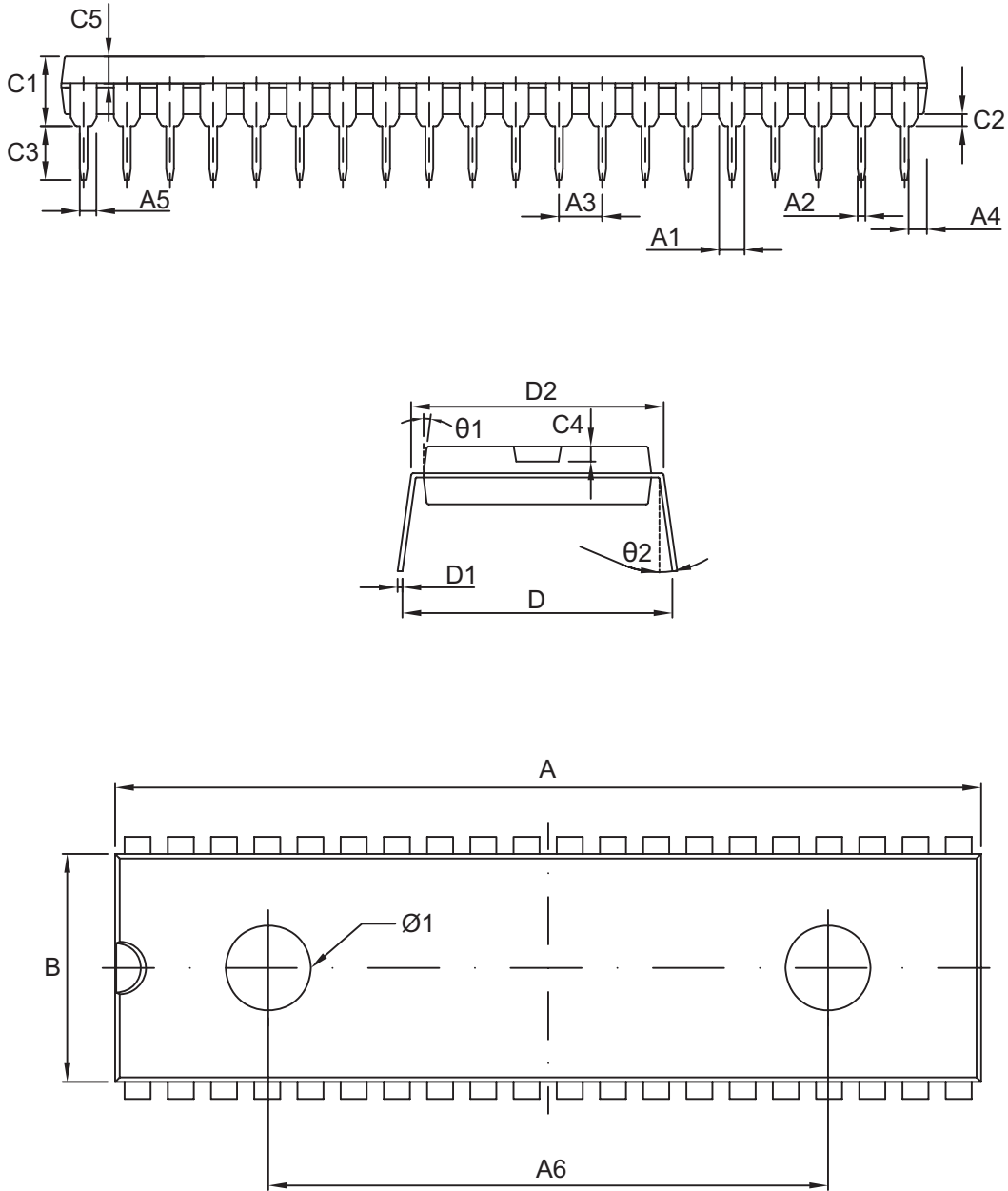


Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	13.20	14.00	D	1.8TYP	
A1	9.90	10.10	D1	0.80TYP	
A2	0.30	0.375	D2	0.60	1.00
A3	0.67	0.93	E1	1.34	1.42
A4	0.85TYP		E2	1.37	1.45
B	13.20	14.00	R1	0.13MIN	
B1	9.90	10.10	R2	0.13	0.3
B2	0.85TYP		Ø3	1.5TYP	
C1	1.90	2.10	Ø2	1.5TYP	
C2	0.11	0.23	θ1	4° TYP	
C3	0.05	0.20	θ2	20° TYP	
C4	0.904	0.944	θ3	8° TYP	



**PHYSICAL DIMENSIONS**

PDIP40

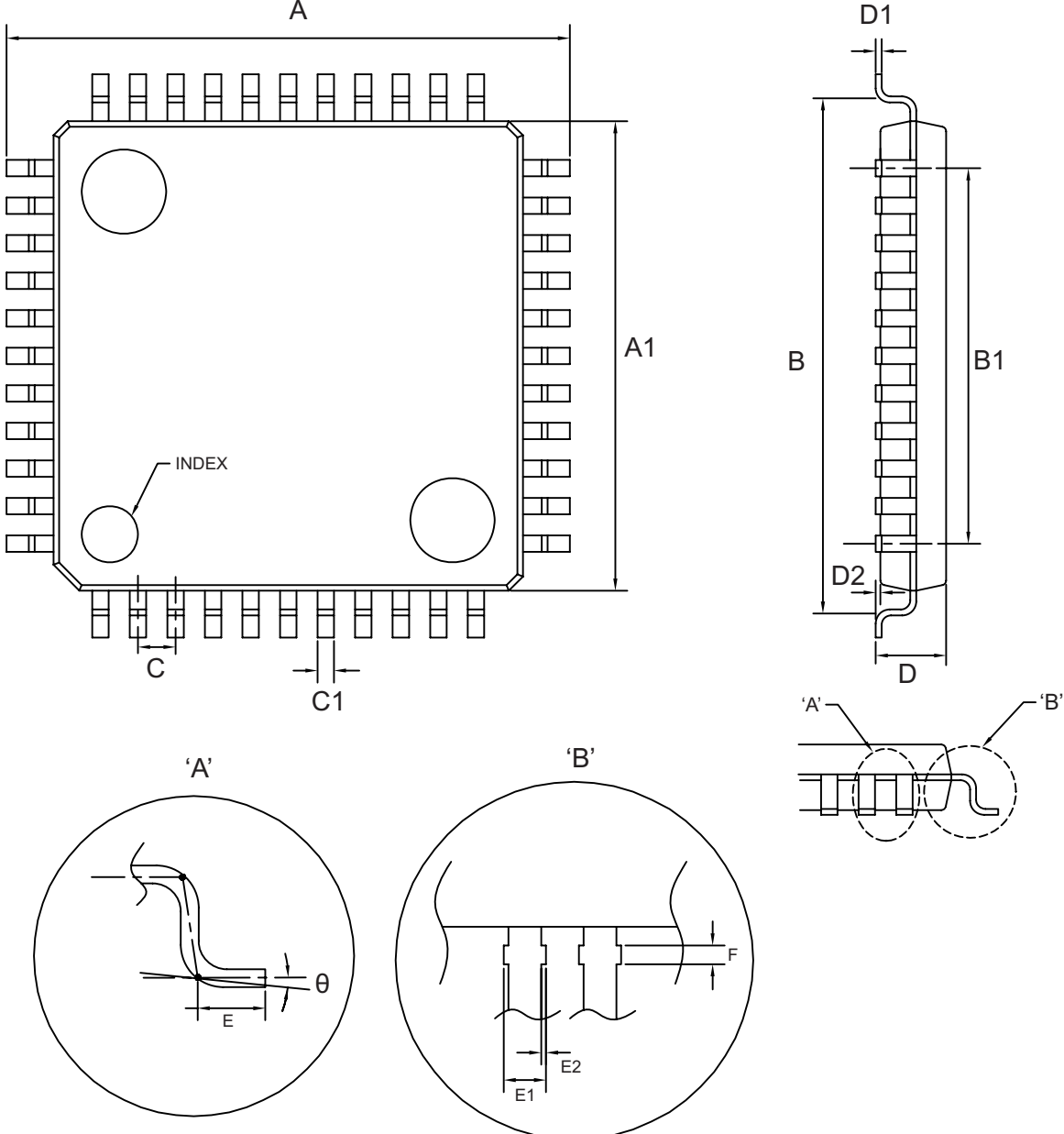


Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	50.55	50.75	C3	3.40	4.00
A1	1.25TYP		C4	0.90TYP	
A2	0.45	0.55	C5	0.90TYP	
A3	2.54TYP		D	15.49	17.38
A4	0.95TYP		D1	0.20	0.35
A5	0.88TYP		D2	15.24	15.49
A6	32.0TYP		R1	1.90TYP	
B	13.75	13.95	$\text{Ø}1$	5.0TYP	
C1		5.10	$\theta_1$	10° TYP	
C2	0.5		$\theta_2$	5° TYP	



**PHYSICAL DIMENSIONS**

LQFP44



Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	11.8	12.2	D1	0.11	0.14
A1	9.9	10.1	D2	0.00	0.20
B	11.00		E	0.30	0.70
B1	8.00		E1		0.50
C	0.80(TYP)		E2		0.15
C1	0.25	0.45	F	0.20	
D	1.40	1.70	θ	10°	



July 2008

Rev 1.0

www.chipwinner.com