ON Semiconductor®

Electromagnetic Compatibility

Agenda

- Basic Information and Market Trends
- EMC Tests
- Design Flow
  - IC Examples
- Case Studies
  - LDO
  - SMPS
  - Drivers
  - IVN
- General PCB Guidelines

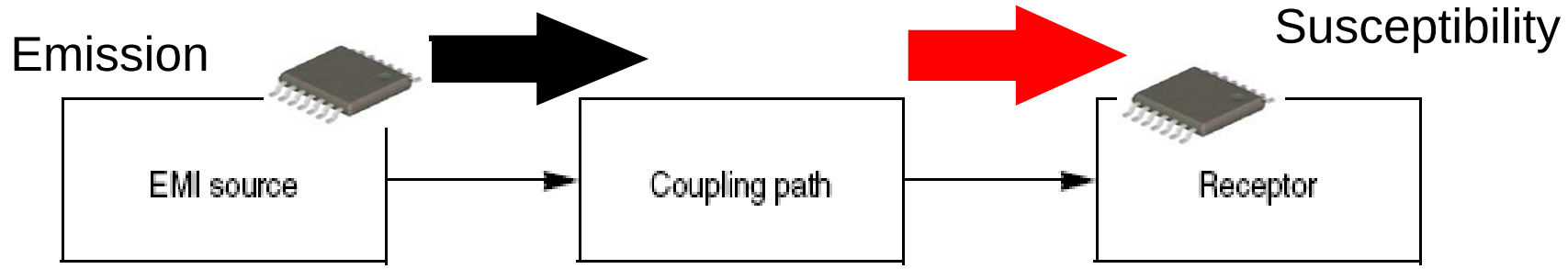
Basic Information and Market Trends

Intro to EMC

- EMC stands for Electro Magnetic Compatibility
  - EMC is the “generalized” terminology used for making electronic systems “compatible” with the magnetic fields that everywhere exist.
  - Magnetic fields like: radio, mobile, TV, power cables, transformers, inductors, etc...
  - “To make compatible” means 2 things:
    - My electronic system should not disturb other systems.
      We talk about Electro Magnetic Emission (EME)
    - My electronic system is immune for disturbances induced by other systems.
      We talk about Electro Magnetic Susceptibility (EMS)
  - For EME we distinguish:
    - “conducted emission” (transferred by coupling or cables)
    - and “radiated emission” (transferred through the air)

Basic Principles

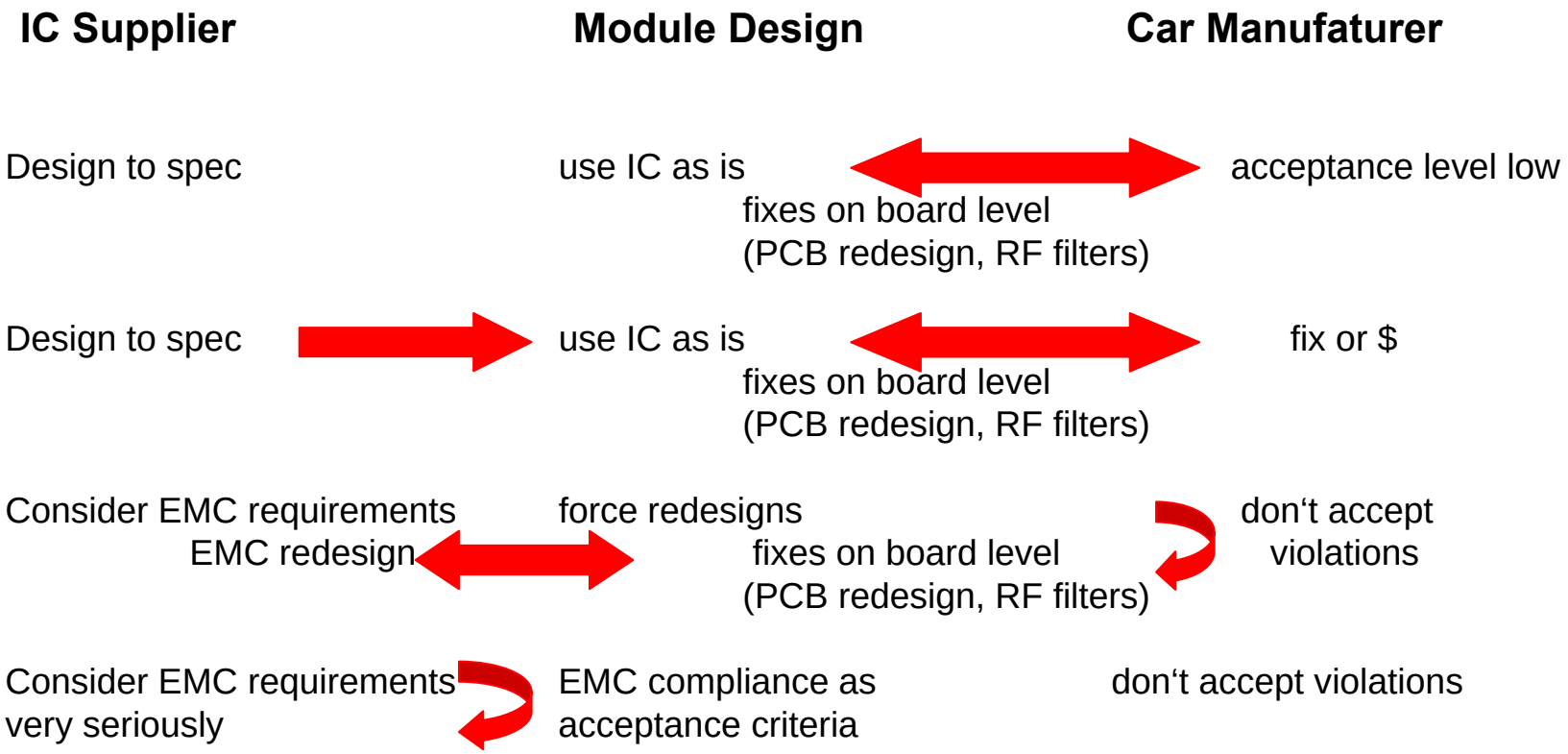
EMC for ICs



of electromagnetic energy

To an electromagnetic wave

Historical Development



EMC characterization results have become a reject criteria for ICs.

Higher Complexity Changes Design Criteria

- Cars are becoming more and more complex w/ each generation.
- With increased complexity (and variety of configurations) it is necessary to guarantee well-defined interface conditions to ensure plug-and-play for all configurations during car-assembly.
- In the past, IEC7637-x was used to “define” the supply conditions.
  - Nominal ratings, load dump, switching transients, etc. are described by this norm.
  - However it does not cover
    - RF susceptibility
    - Emissions
- Spectrum/Power has widened in the recent past due to increased usage of RF-based tools.
- Wide application range of ASSPs vs. ASICs
- Consequently, the EMC requirements must to be considered at IC level to improve system compatibilities.

EMC Tests

EMC Standards

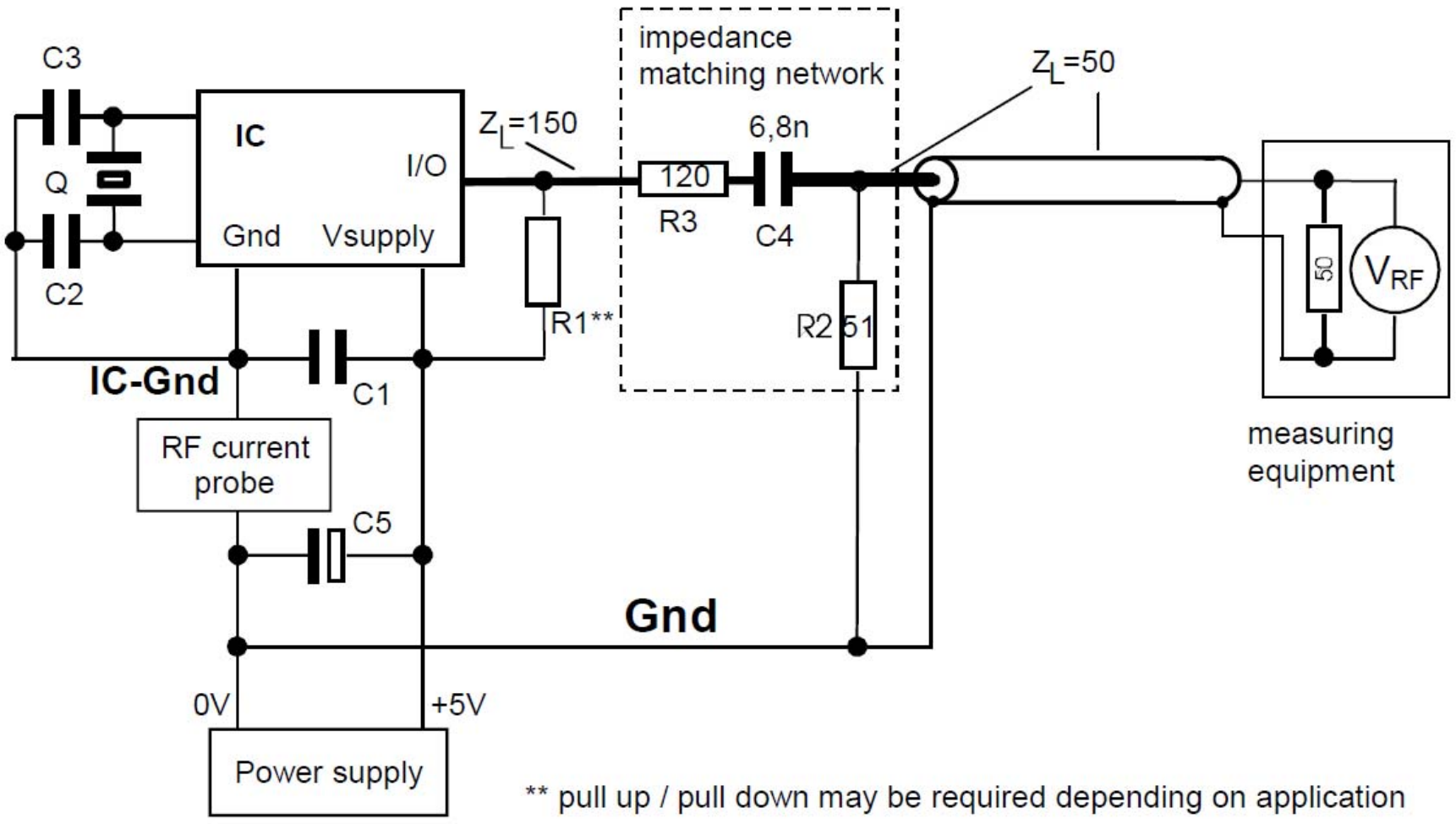
- Acceptance tests Car-level
  - Radiated power (emissions, immision), tested at car
  - Norm: CISPR25 and customs
  - Frequency range: 10kHz – 18GHz

- Since 2003, standards have been released to provide test methods especially for components.

- For *Emission*, IEC-61967 is commonly used. ON Semiconductor uses IEC-61967-4 which is 1 Ω/150 Ω conducted method accepted by car manufacturers. In a few cases IEC-61967-2 (Tem Cell method) can be applied for radiated emission.

- For *Susceptibility*, ON Semiconductor applies IEC-62132-3. The DPI (Direct Power Injection) test method is currently accepted because it is easy to reproduce the set up and close to the perturbations received on the application board.

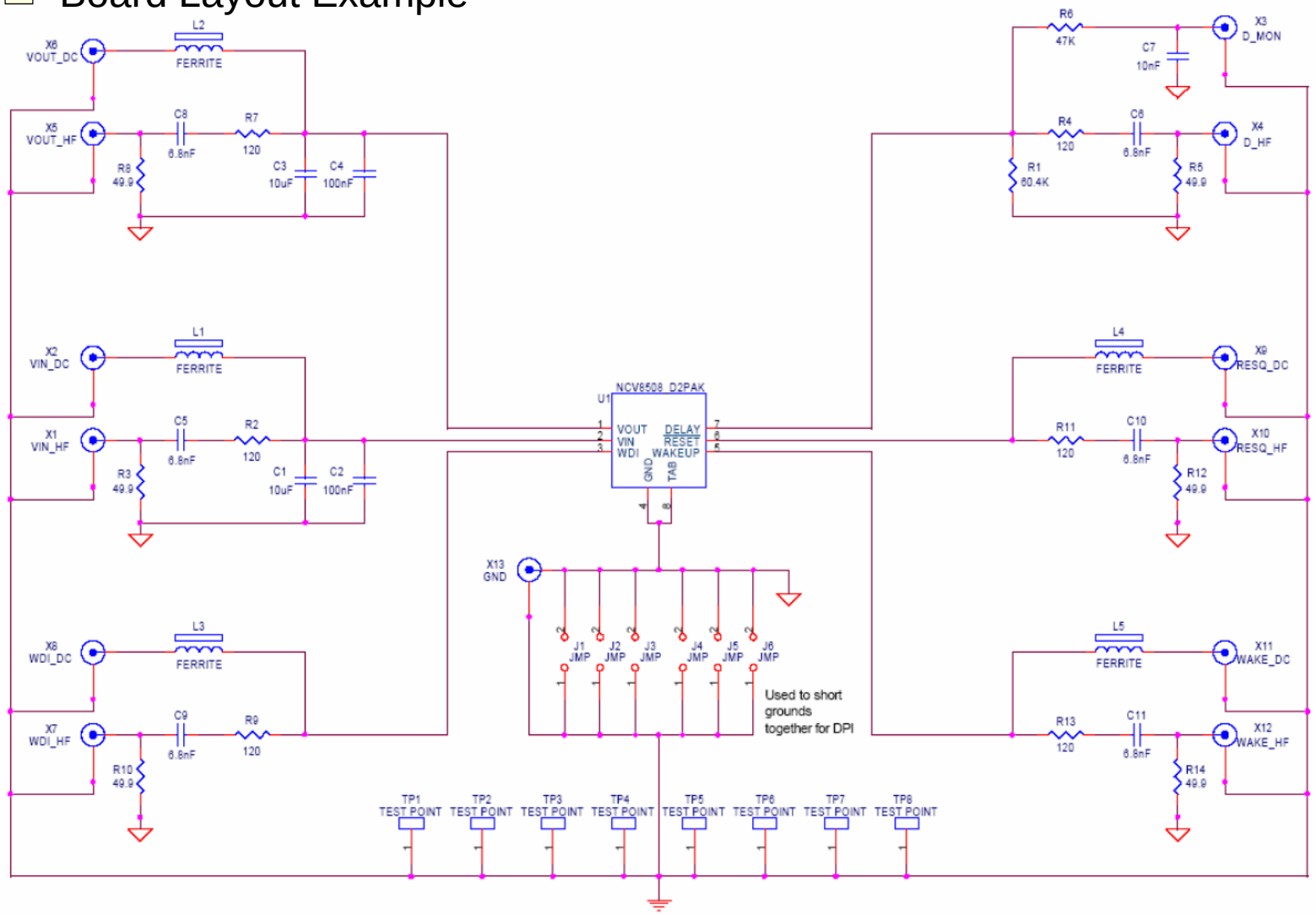
IEC 61967-4



** pull up / pull down may be required depending on application

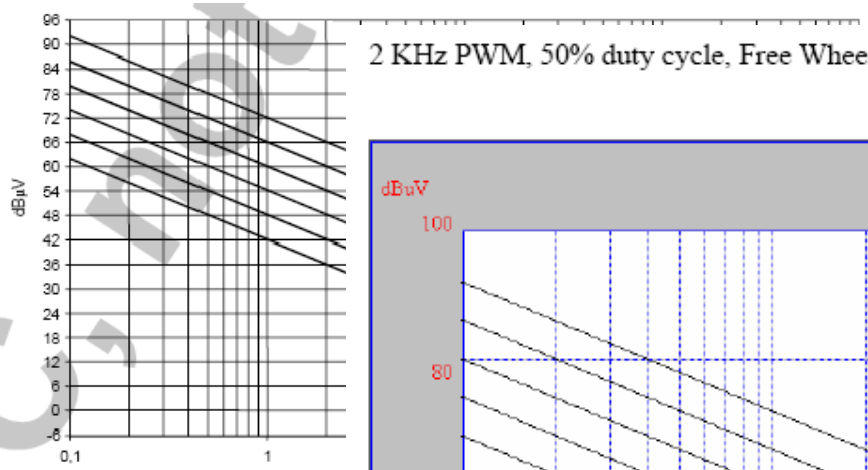
IEC 61967-4

- Board Layout Example

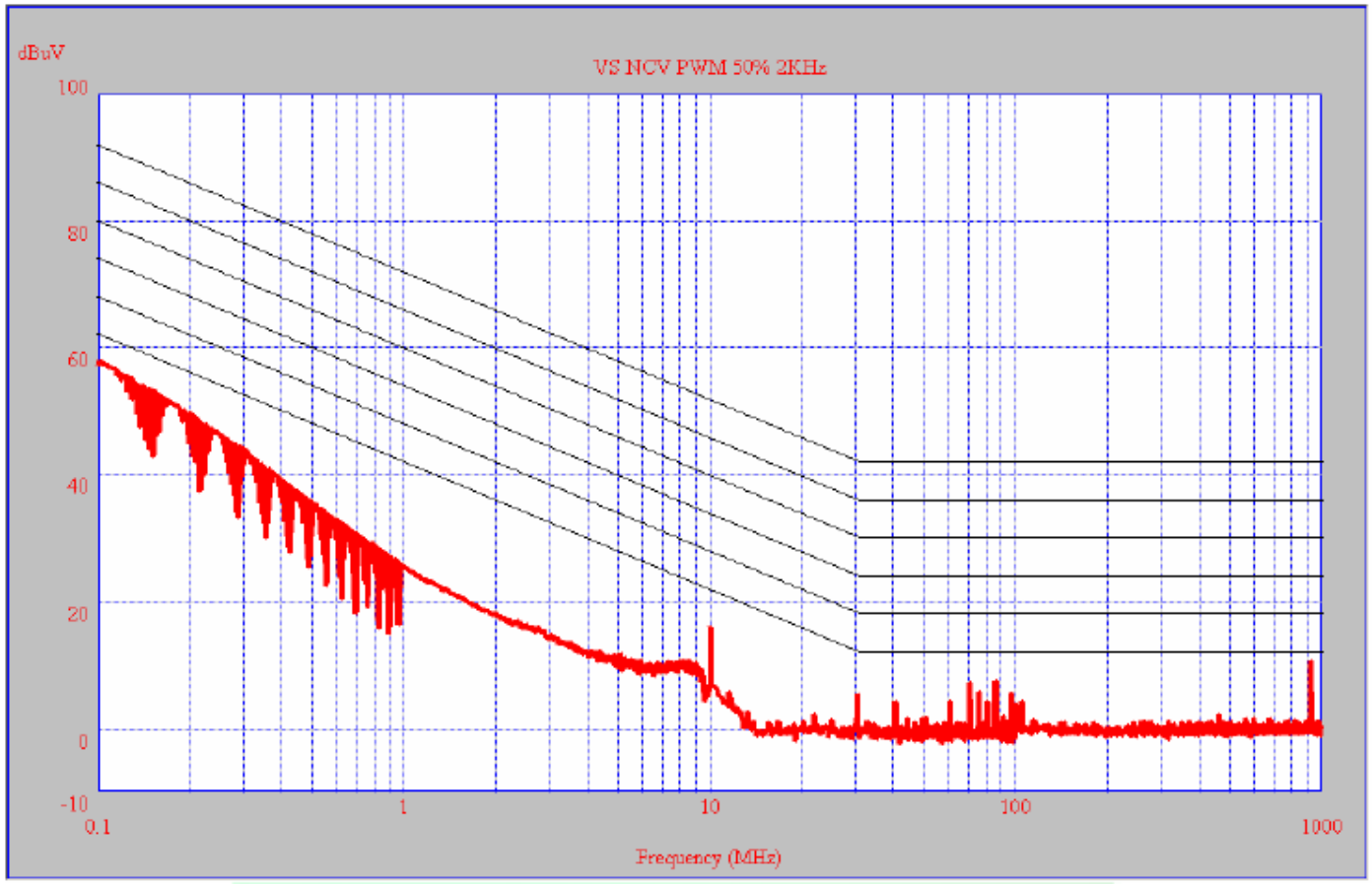


IEC 61967-4

Measurement Levels

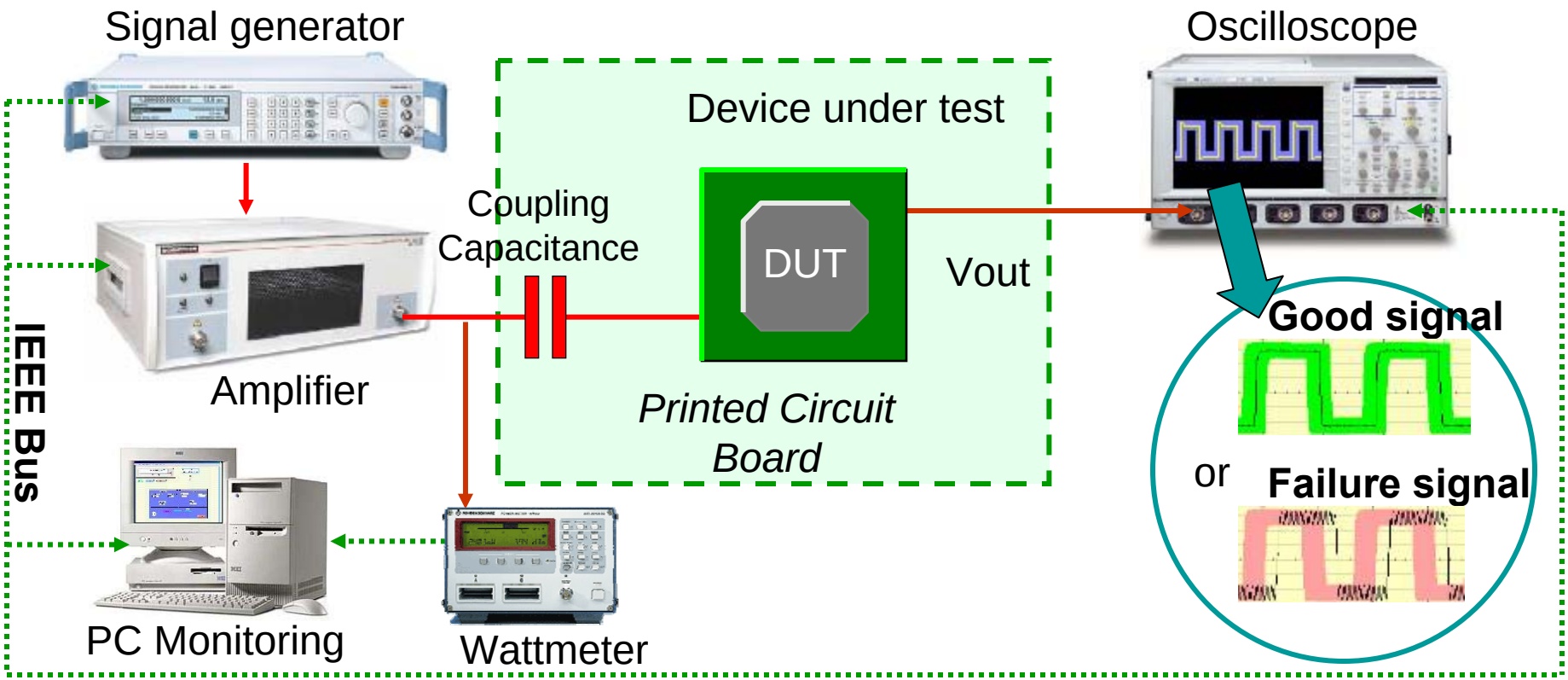


2 KHz PWM, 50% duty cycle, Free Wheeling HS



IEC 62132-4

ON Semiconductor DPI Setup



IEC 62132-4

Measurement levels

Immunity limit classes	*DPI [forward power] dBm*	
	global pin	*local pin*
I	18	0
II	24	6
III	30	12

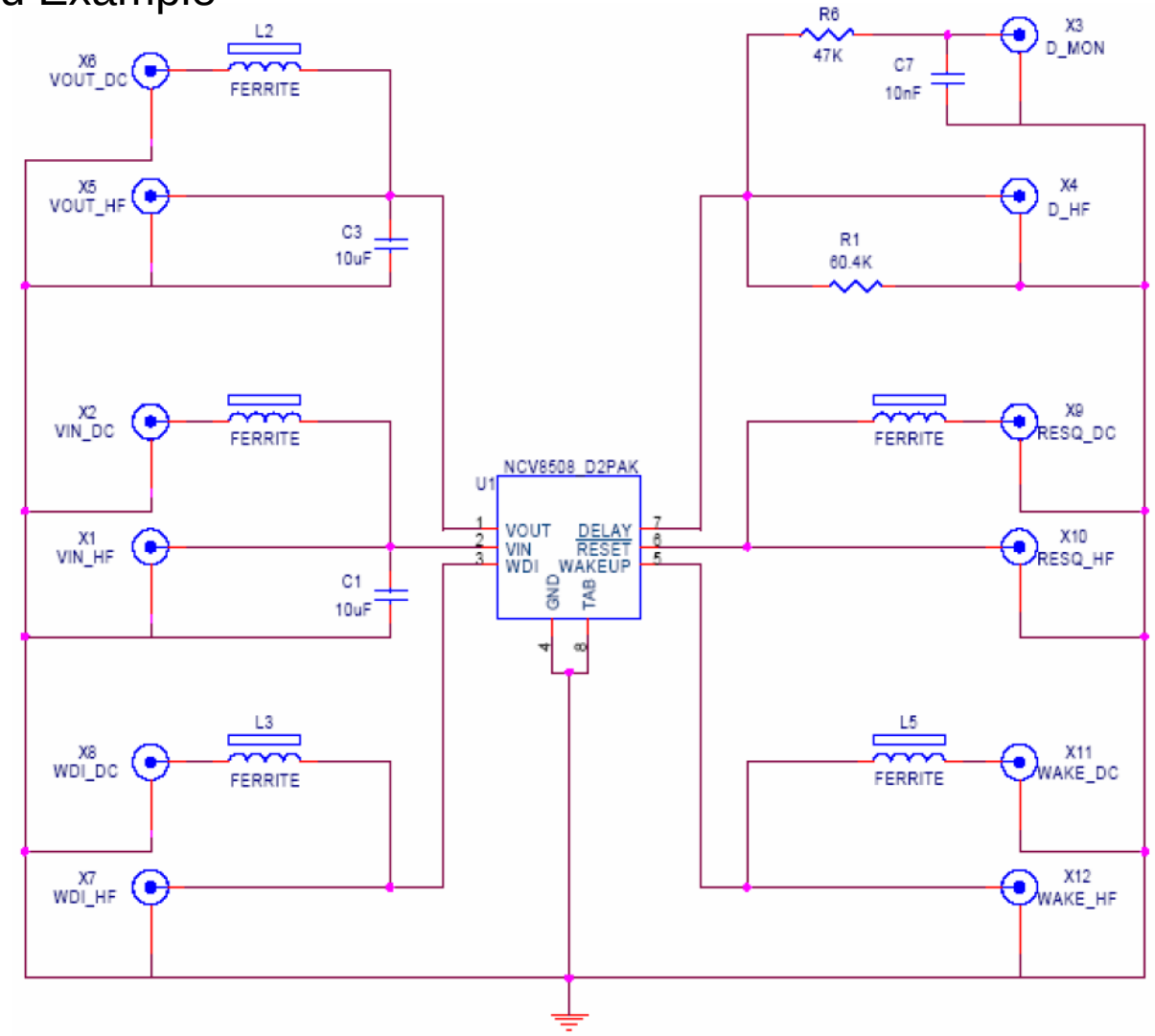
30 dBm = 1 W

A **global** pin carries a signal or power which enters or leaves the application board

A **local** pin carries a signal or power which does not leave the application board. It remains on the application board as a signal between two components

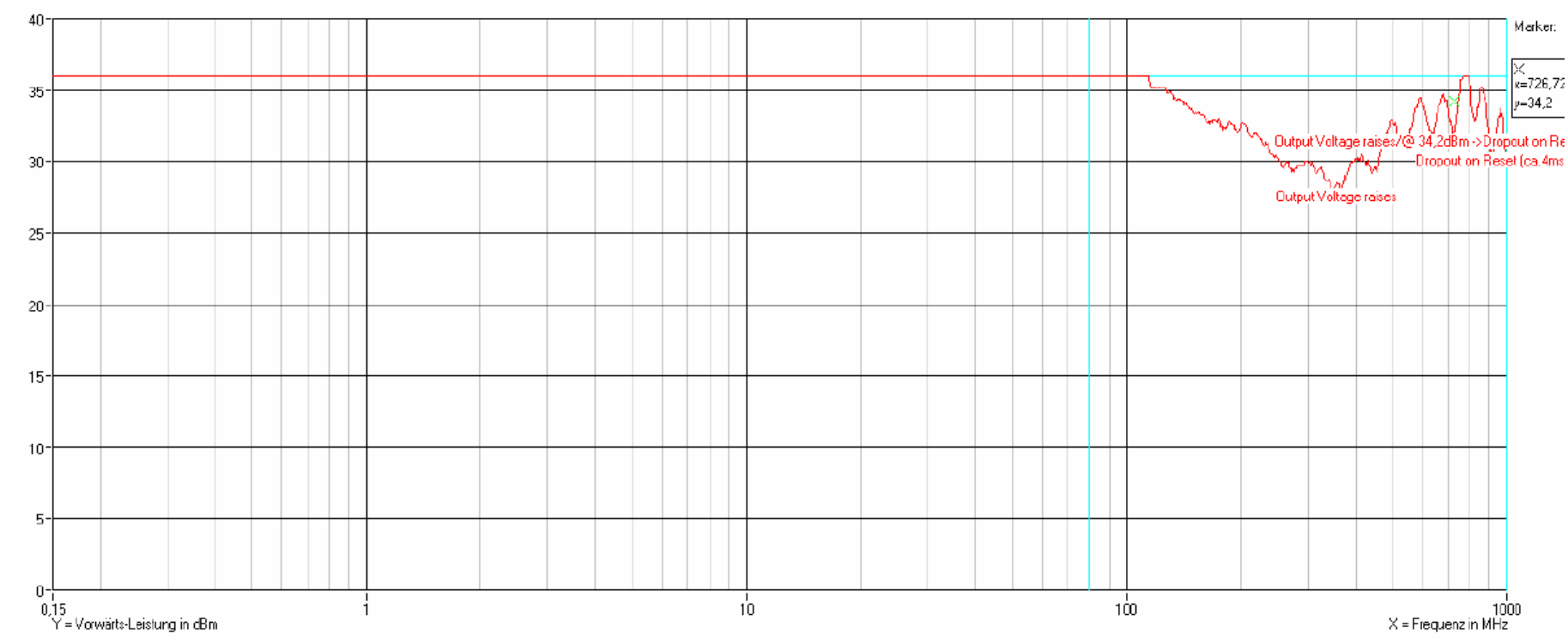
IEC 62132-4

Board Example



IEC 62132-4

DPI Results



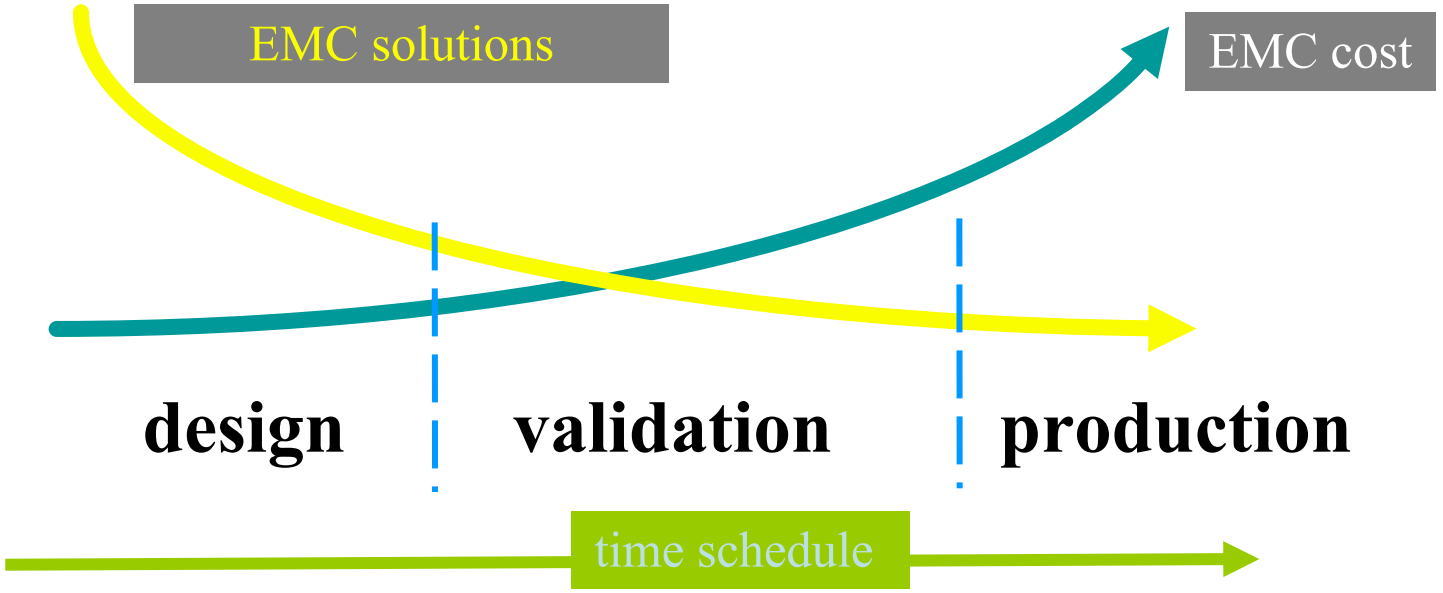
EMC Setup Conclusion

- **Direct power injection (DPI)** - conducted immunity method in accordance to:
  - *IEC 62132 part 4* – measurement of electromagnetic immunity of integrated circuits
  - CISPR25 – limits and methods for measurement
  - ISO 11452 part 7 – component test method for electrical disturbances
  - FTZ recommendation (IBEE tests) for CANs and LINs
- **1 Ω and 150 Ω method** for conducted emission measurement in accordance to:
  - *IEC 61967 part 4* – measurement of conducted emission of integrated circuits
  - CISPR25 – limits and methods for measurement
  - FTZ recommendation (IBEE tests) for CANs and LINs
- **Emission measurements by TEM cell –** radiated electromagnetic emissions method in accordance to:
  - *IEC 61967 part 2* - measurements of radiated electromagnetic emissions of integrated circuits
  - CISPR25 – limits and methods for measurement
- **Bulk current injection (BCI)** – immunity test by magnetic field in accordance to:
  - *IEC 62132 part 3* – immunity test of integrated circuits by bulk current injection 400Mhz
  - ISO 11452 part 4 – component immunity test by bulk current injection

Design Flow

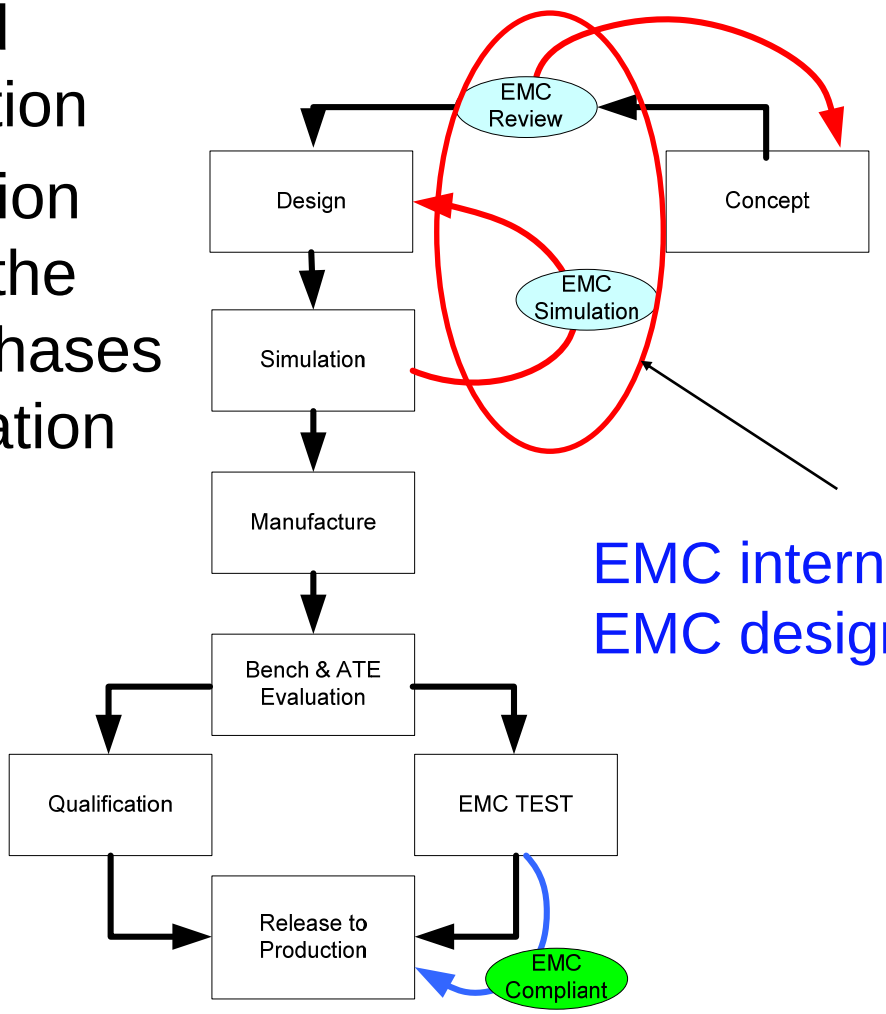
EMC Methodology

- Why taking into account EMC in development phase?
- EMC fails has been one of the most critical success factors in new module developments.
  - There are multiple ways to fail.
  - An EMC issue always impacts the timeline.



EMC Methodology

- EMC validated before fabrication
- Include reduction techniques in the early design phases and run simulation

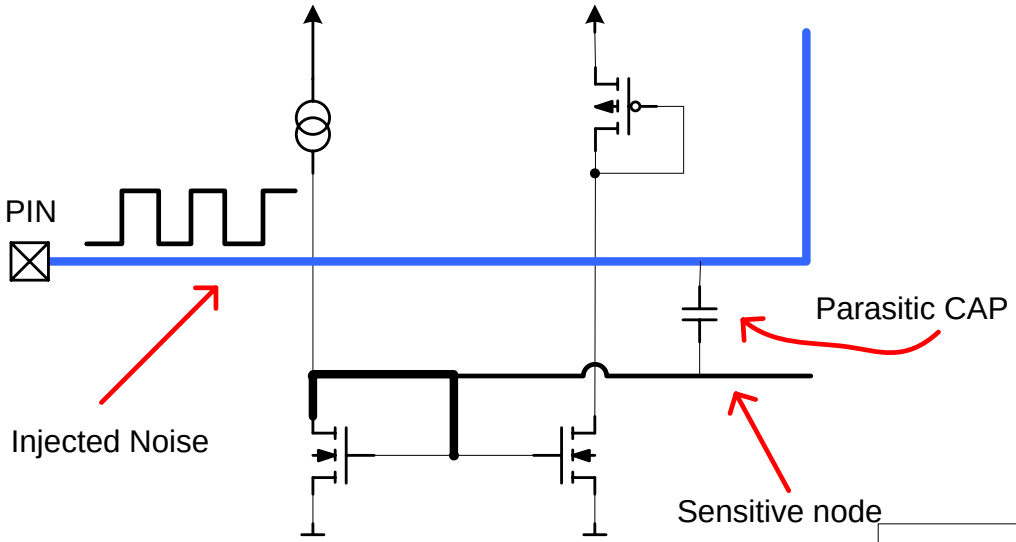


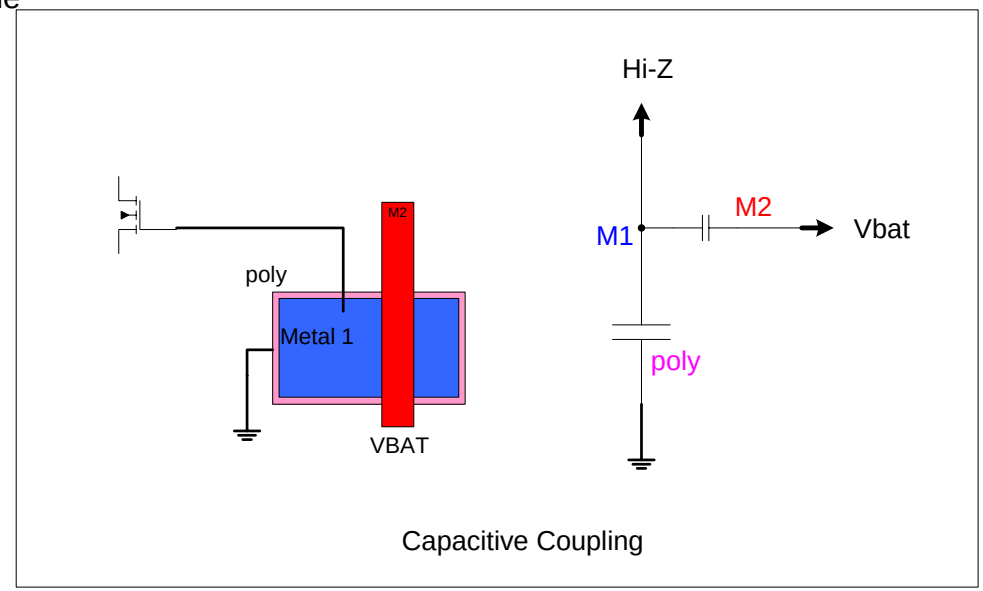
EMC internal Specifications
EMC design/layout review

Impact to design work

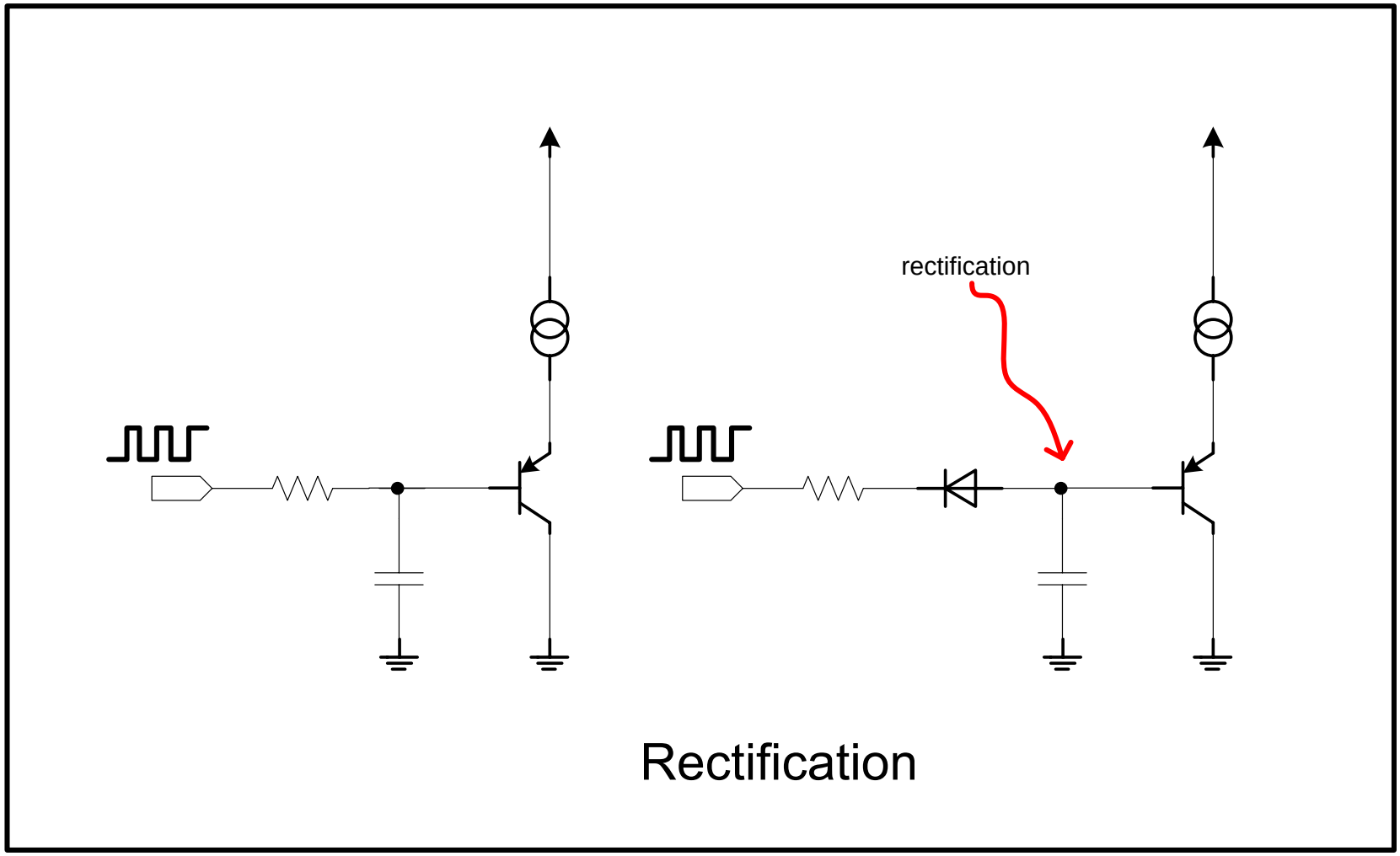
- What can be done at the development phase to improve designs ?
- Individual contributions:
  - Device definition
    - Pinout, Partitioning, Technology selection
  - Circuit concepts
    - Signal processing paths, Biasing, Logic concepts
  - Circuit topologies
    - I/O structures !
  - Layout
    - Floorplanning, Metal routing,...

Capacitive Coupling (Layout)

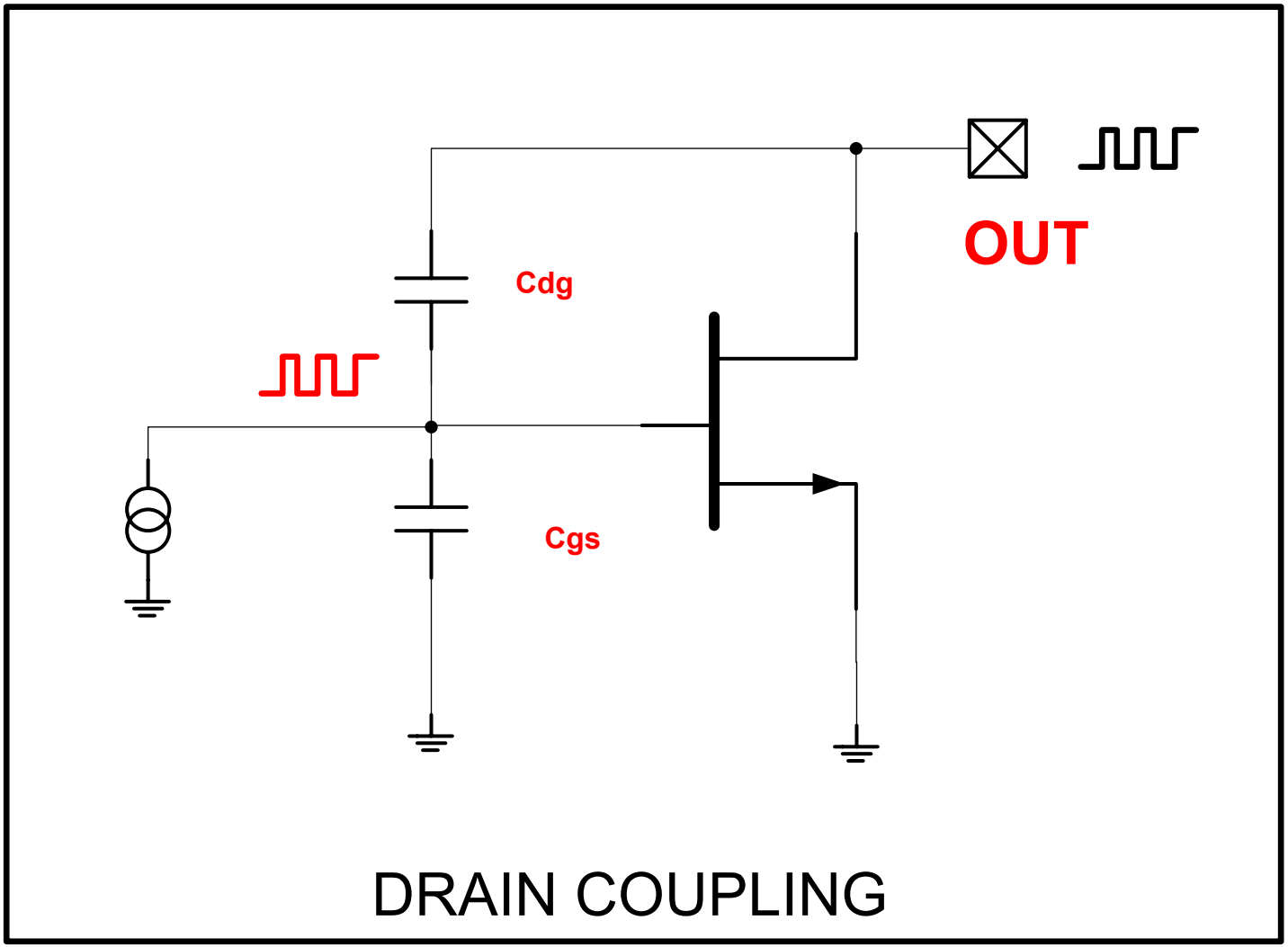




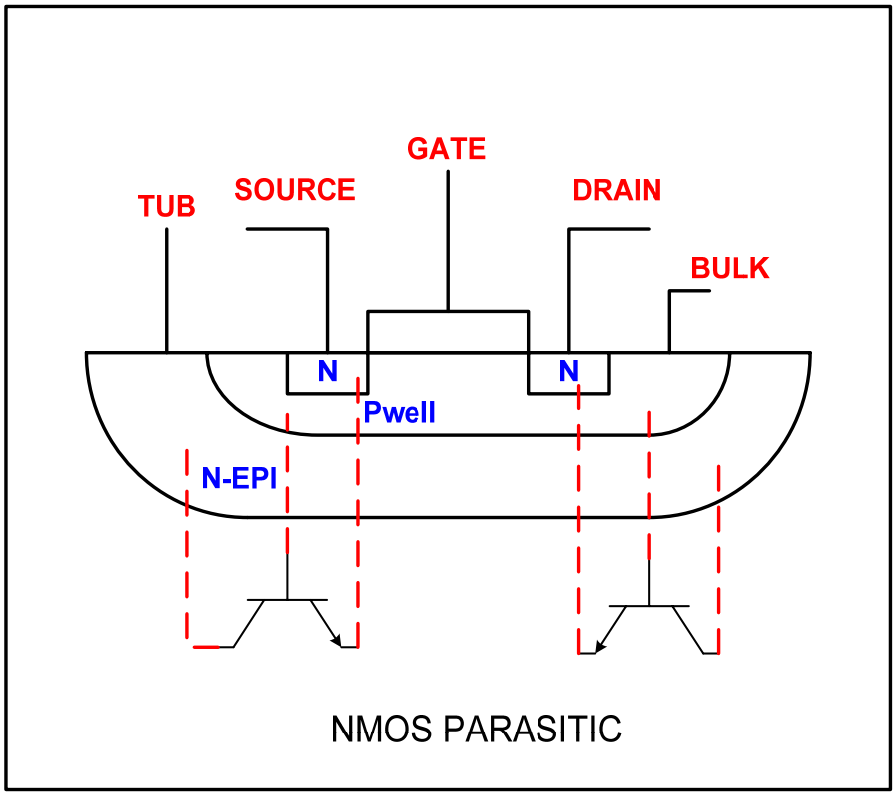
Rectification



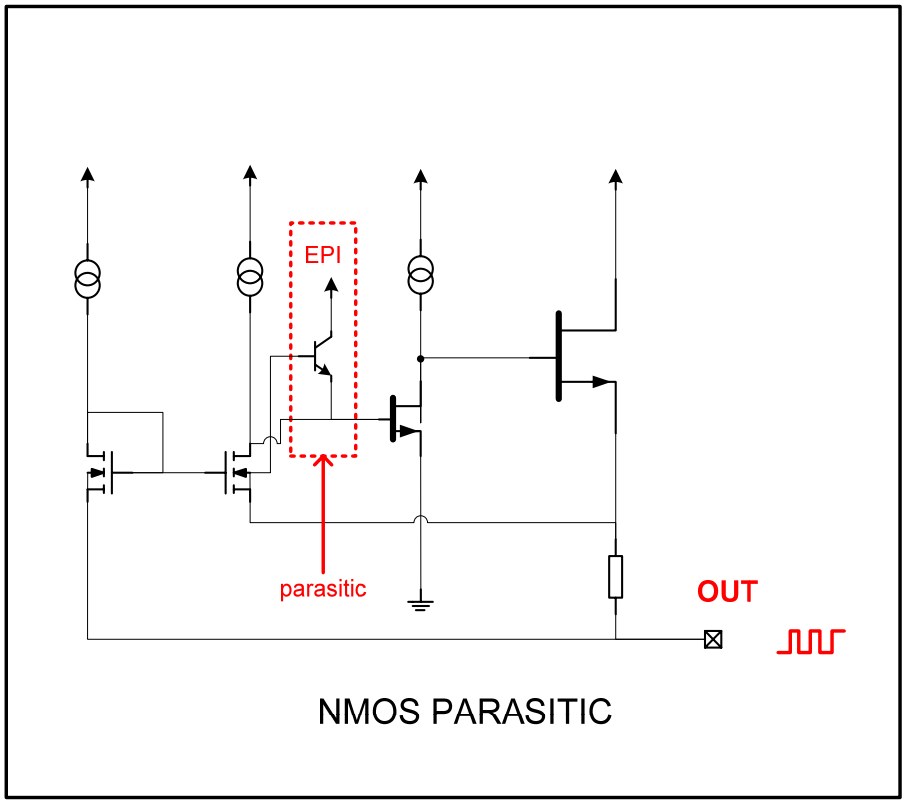
Drain Coupling



Parasitic NMOS



NMOS PARASITIC

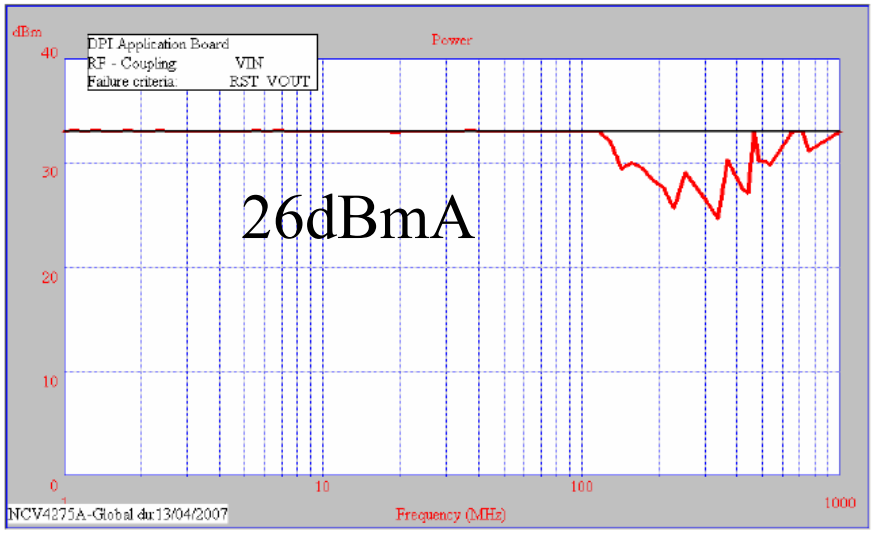


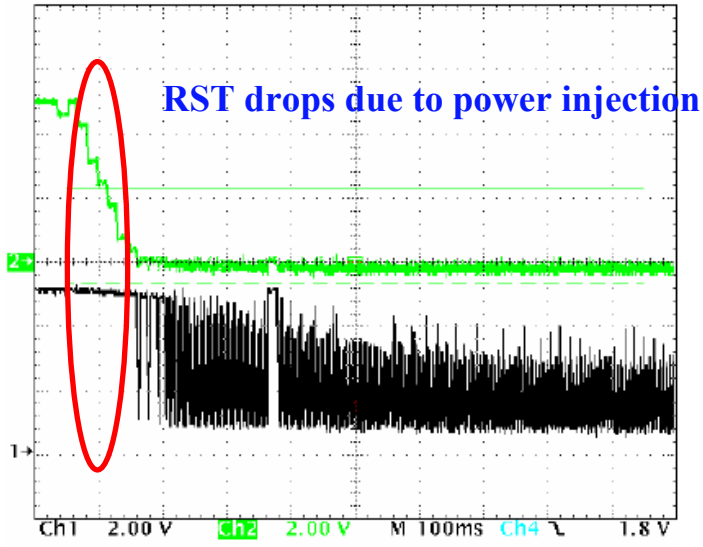
NMOS PARASITIC

Case Study: LDO

NCV4275A BCI Failure

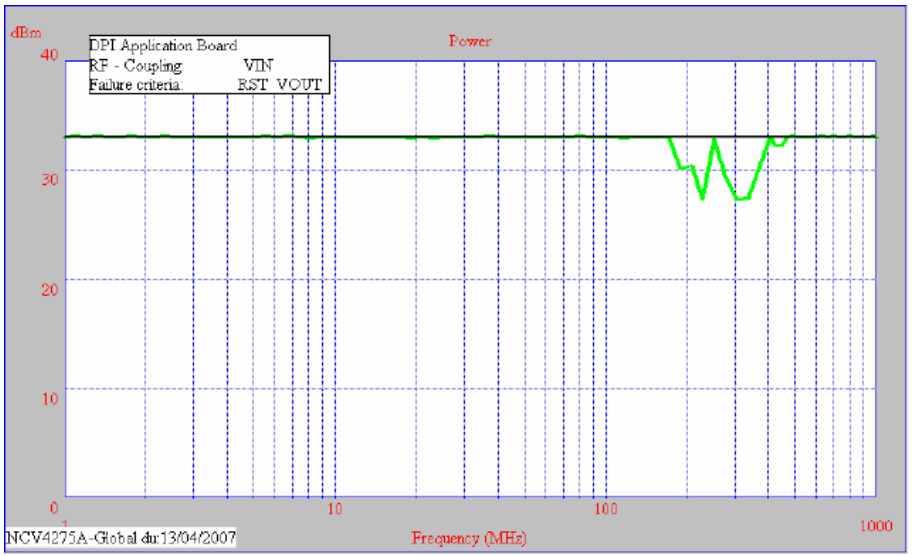
- During VIN injection, the NCV4275 exhibits a non acceptable failure on the RST pin

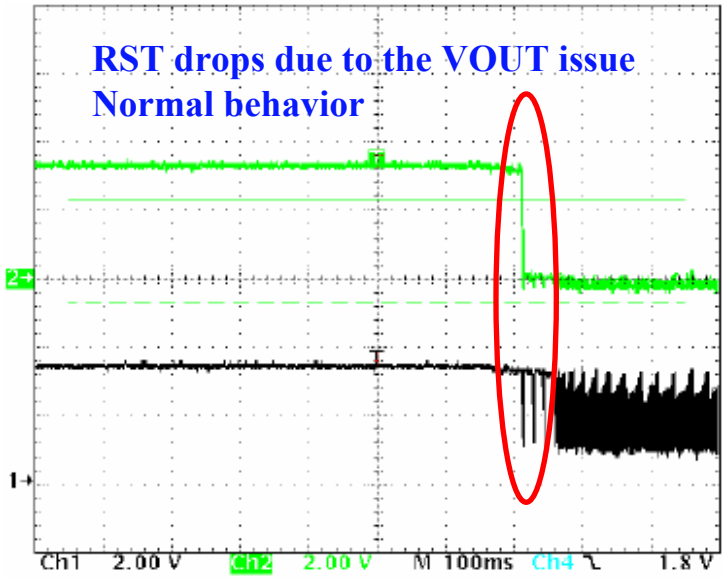




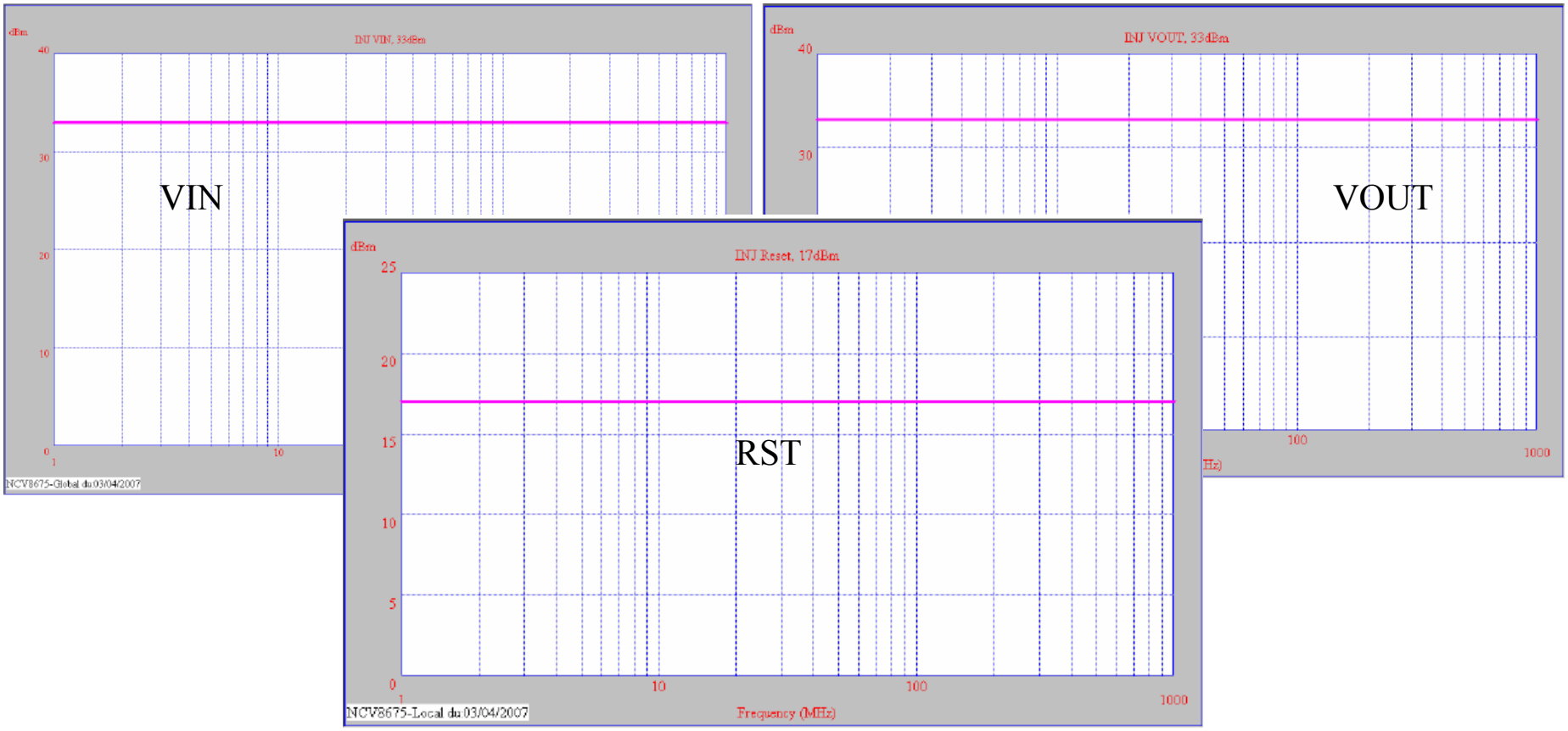
NCV4275A EMC Solution

- By filtering the RST comparator, the failure mode disappears



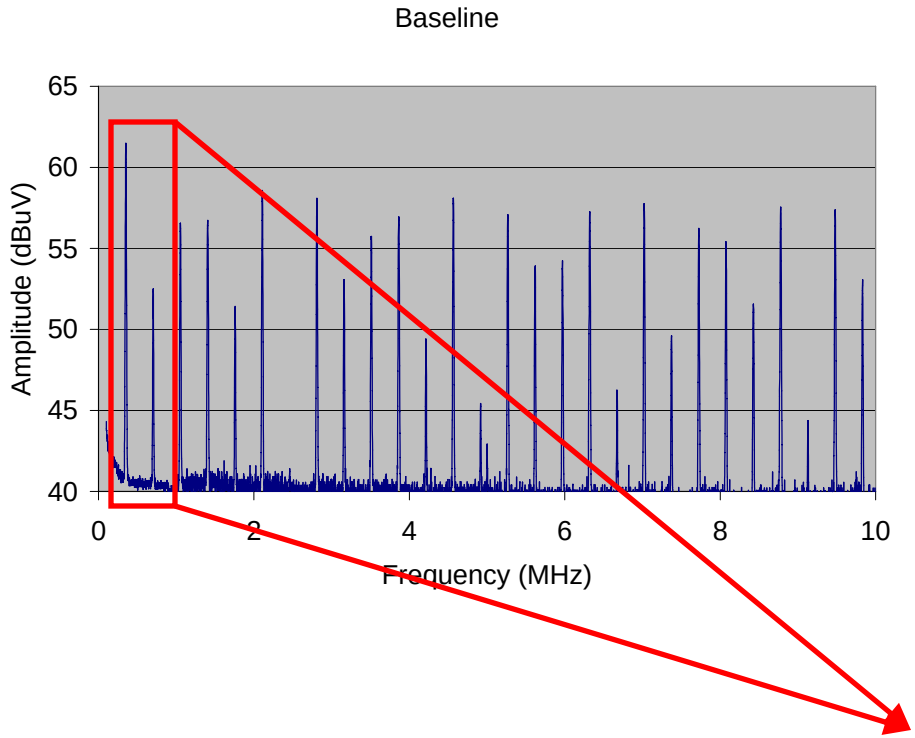


NCV4275A DPI results

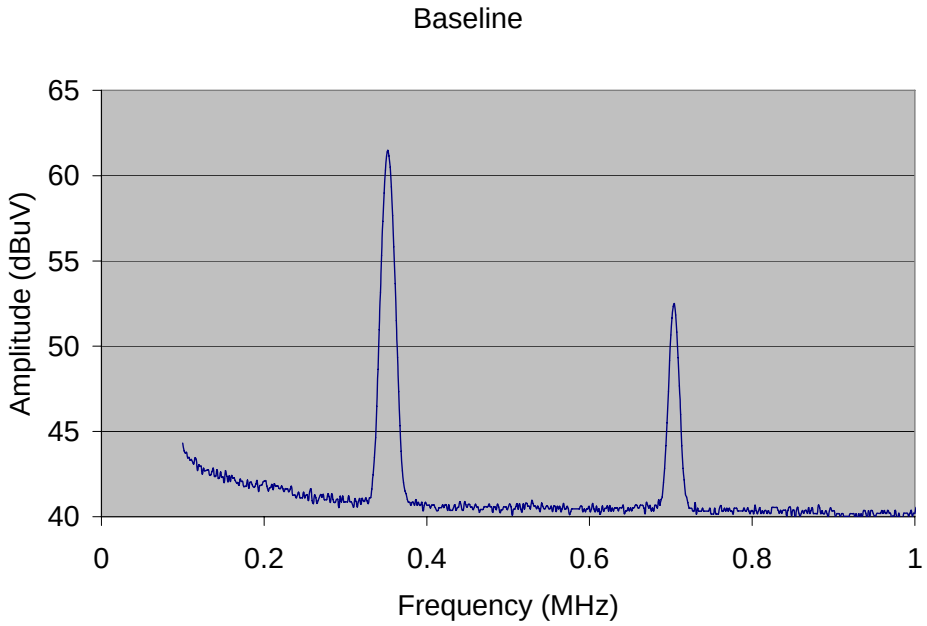


Case Study: SMPS

NCV8851 Emission Levels

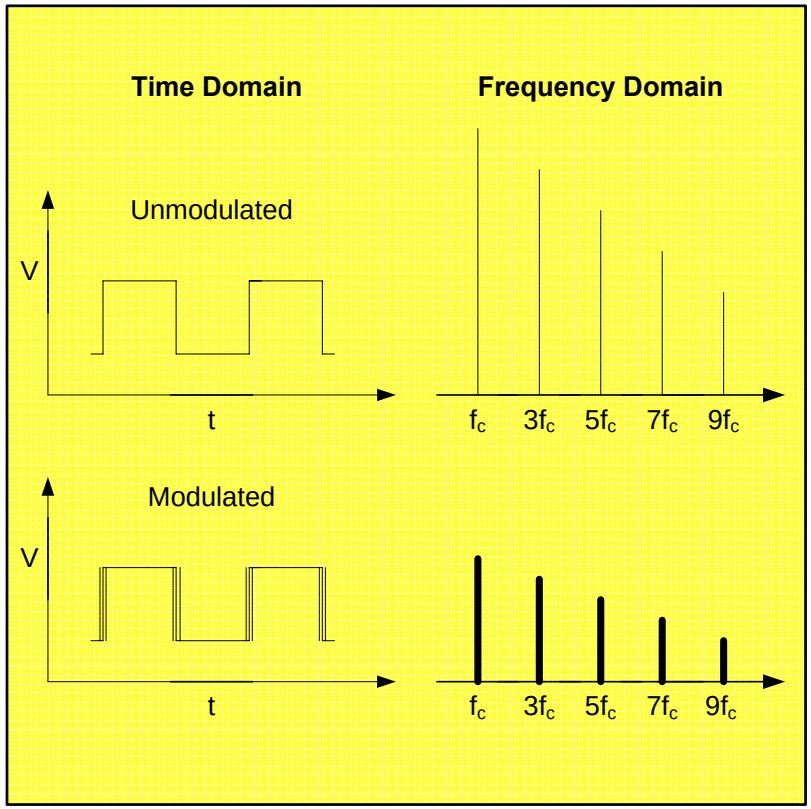


- Radiated emissions testing for switching regulator
- Switching creates a lot of noise



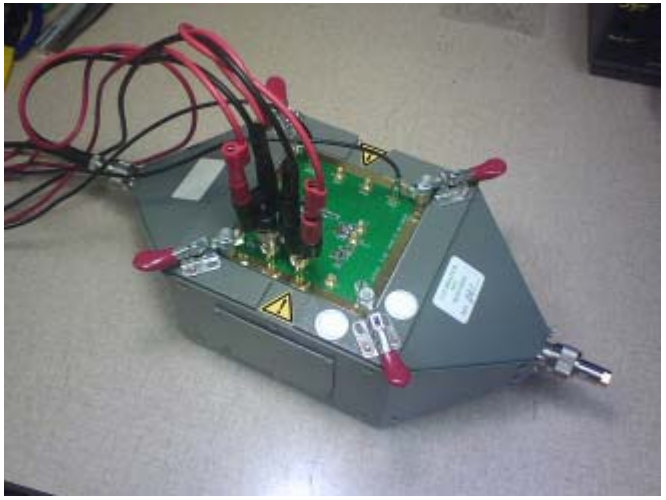
Spread Spectrum Techniques

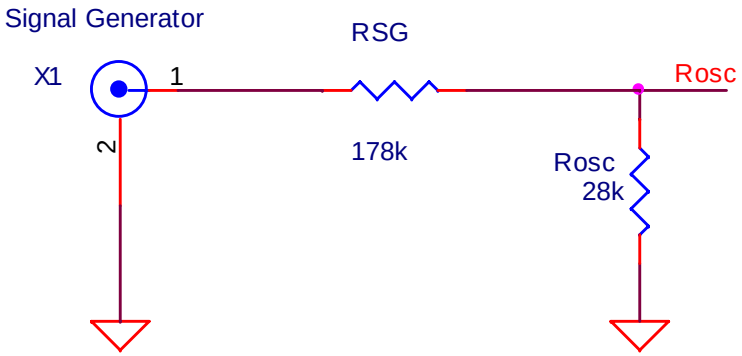
- Spread spectrum modulates the switching frequency
- Reduces peak noise in frequency domain by spreading to sidebands



NCV8851 Spread Spectrum

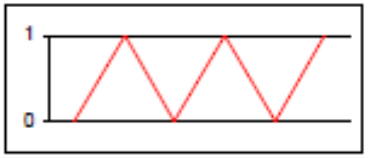
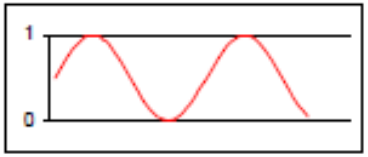
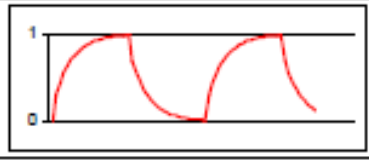
- Typical setup for a TEM cell.





- Signal generator attached to Rosc network to modulate the current.

- Changes the switching frequency

Waveform	Signal Generator
Linear (Triangle Wave)	
Sine Wave	
Square Wave	
RC Filtered Square Wave	

NCV8851 Spread Spectrum

- The switching frequency for the SMPS device tested is set by the Rosc pin which connects to GND through a resistor.

- The resistor value is determined by:

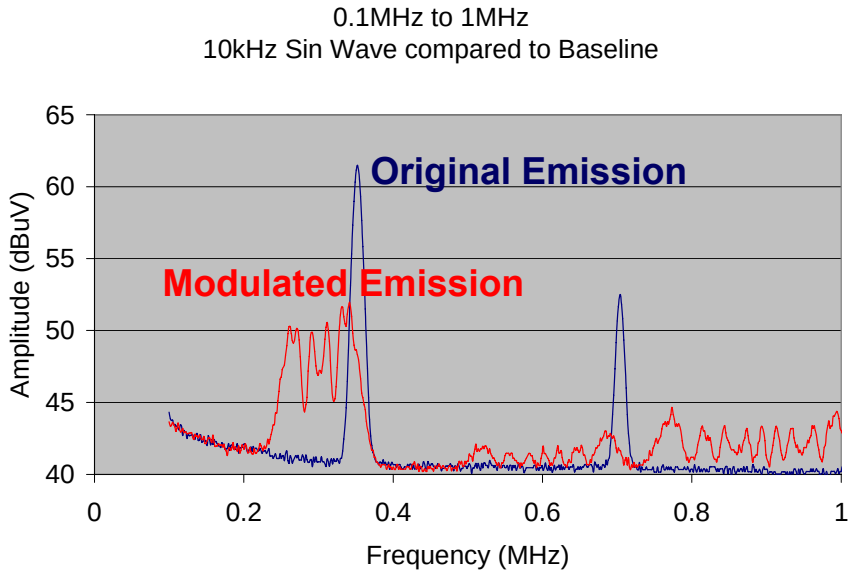
$$R_{OSC} = \frac{8687000}{F_{SW}}$$

- Fsw is the switching frequency [Hz] and Rosc is the pin resistance [kΩ].

Voltage (V)	0	0.5	1
Rosc (kΩ)	24.19	28.00	33.23
Fsw (kHz)	359.05	310.25	261.45

NCV8851 Spread Spectrum

- Peaks are reduced and the sidebands are expanded
- Harmonic peak values are also reduced
- Modulation with a 10 kHz sine wave was the most effective method



Spread Spectrum Conclusions

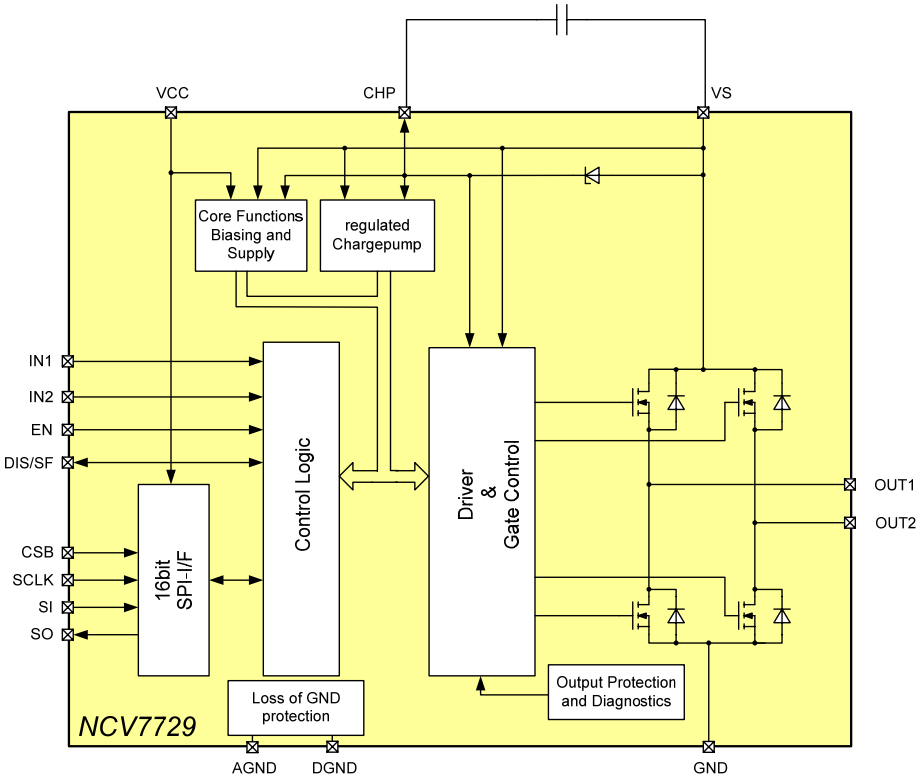
- Spread spectrum methods have the unique ability to reduce the noise at the switching frequency of an SMPS device.

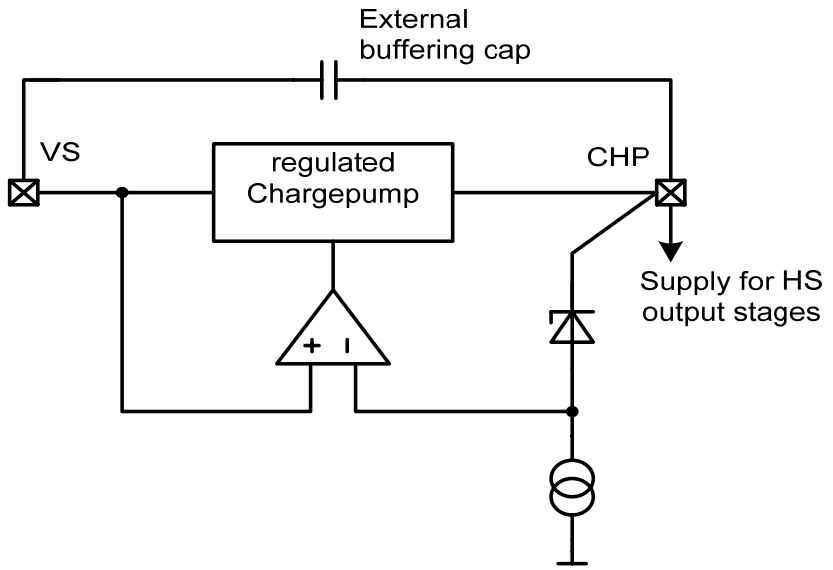
- Through modulation at the Rosc pin, the switching frequency can be spread to nearby frequencies, thereby reducing the peak emission levels at the fundamental frequency and the related harmonics

Case Study: Drivers

NCV7729 Charge pump Architecture

- CHP: Regulated Chargepump (max. -0.3 / 50 V)
  - 2 kHz mode w/ reduced chargepump power





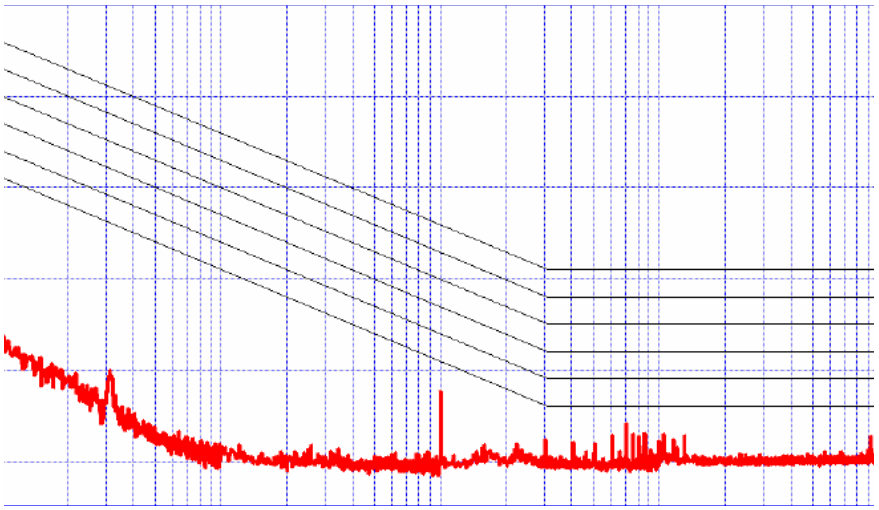
EMI Improvements

- Waveshaping to suppress higher harmonics in load current (d^2I/dt^2)
- Regulated Chargepump principle
  - Reduced RF current consumption of Chargepump
  - Improved Gate control (Voltage control vs. Current control)
  - No RF output voltage ripple
  - Smaller chargepump w/ improved efficiency

Switching frequency	[kHz]	20.00
CHP switching charge Q(CHP)	[nC]	60.00
Slope time	[µs]	3.00
Chargepump charge time	[%]	50.00
Chargepump efficiency	[%]	30.00
ICHP	[mA]	40.00
Unbuffered chargepump		
I(VB) for CHP	[mA]	133.33
Buffered chargepump		
ICHP(average)	[mA]	1.20
I(VB) for CHP	[mA]	4.00
I(VB) buffered/I(VB) unbuffered	[1]	0.03
	dB	-30.46

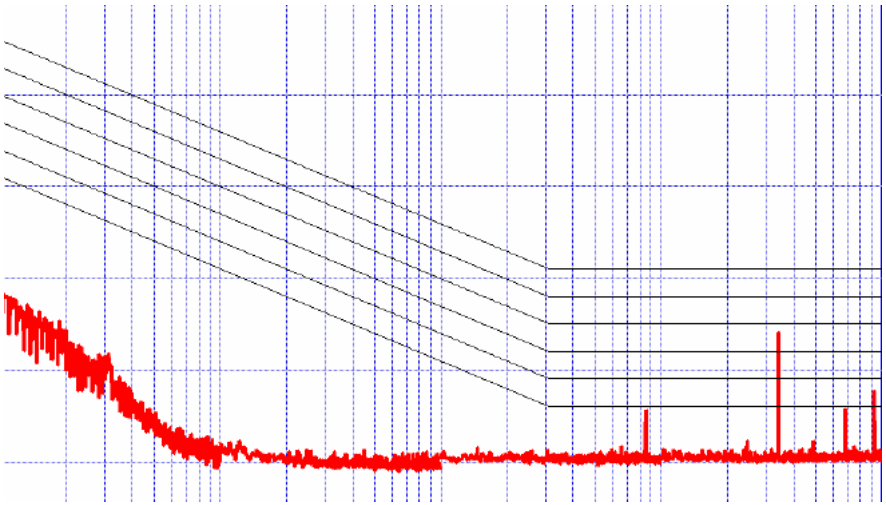
EMI Comparison using 150 Ω on VS pin

Regulated 3 phases charge pump



Device Pass 13-N limit

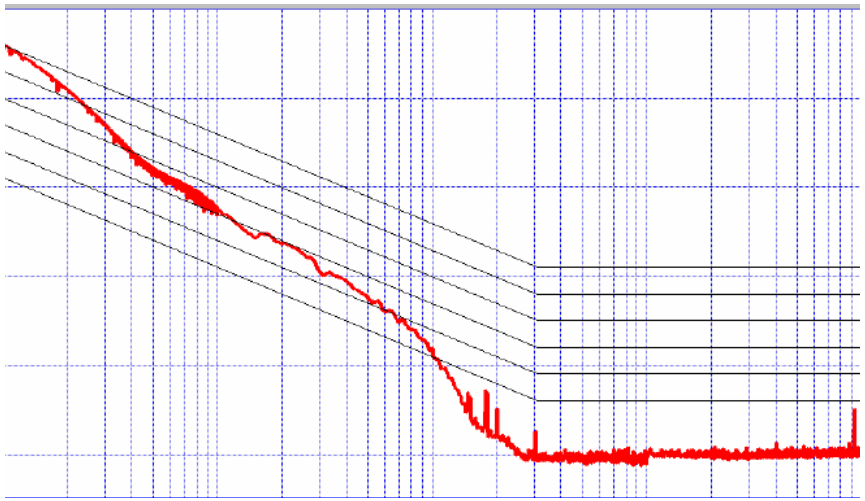
Unregulated 3 phases charge pump



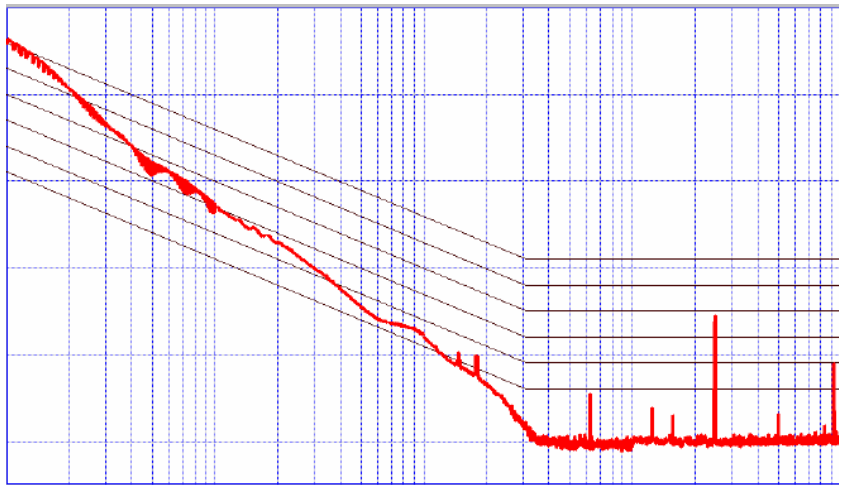
No PWM, IN1, IN2 tied to Vcc

EMI Comparison using 150 Ω on OUT1 pin

Regulated 3 phases charge pump



Unregulated 3 phases charge pump



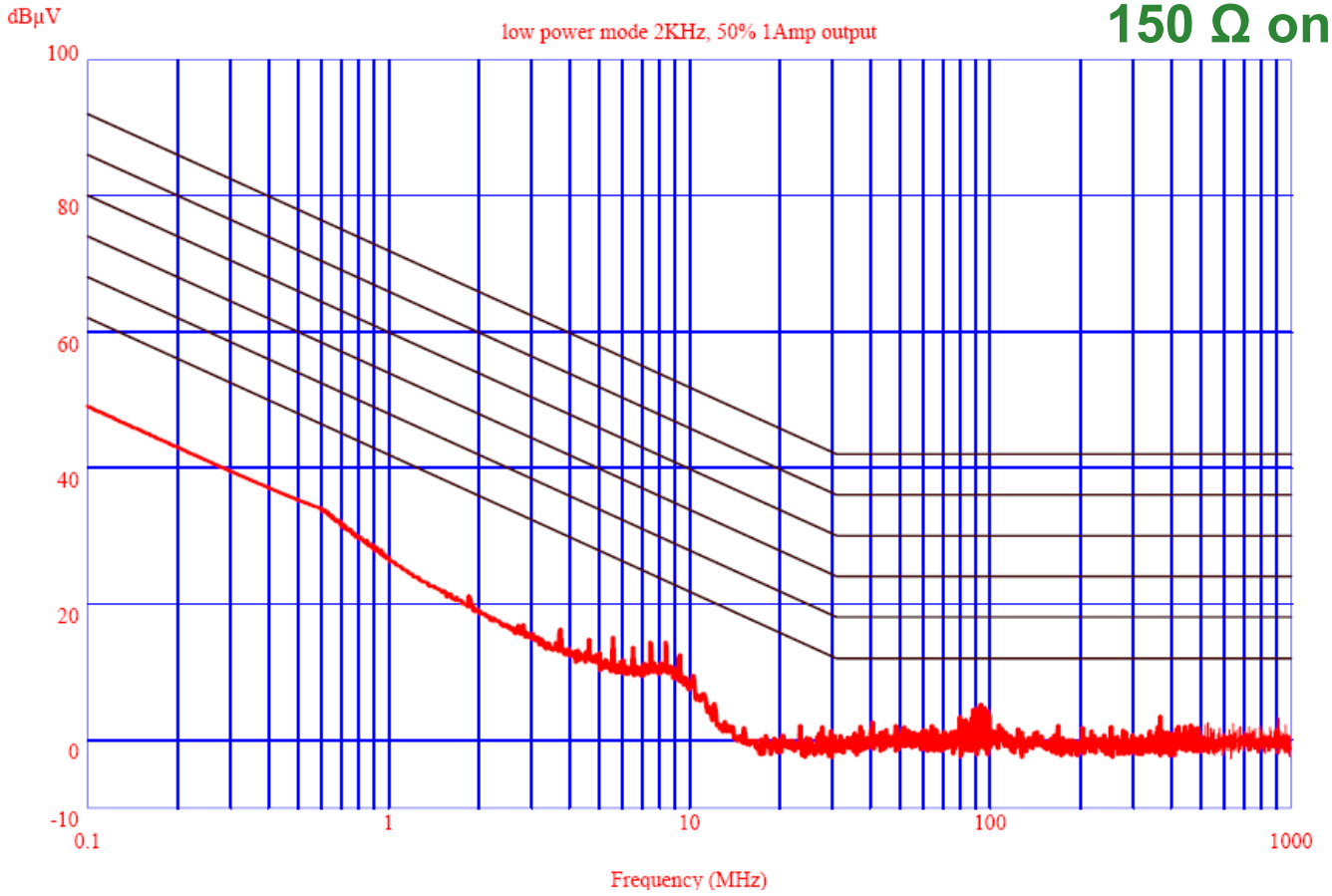
2 KHz PWM, 50% duty cycle, Free Wheeling HS

Load 2.2 mH, 13Ω, 1 Amp load current

Low Power CHP Mode

- By programming the low power mode, the frequency of the CHP is reduced to 1 MHz improving the EMI performance in HF

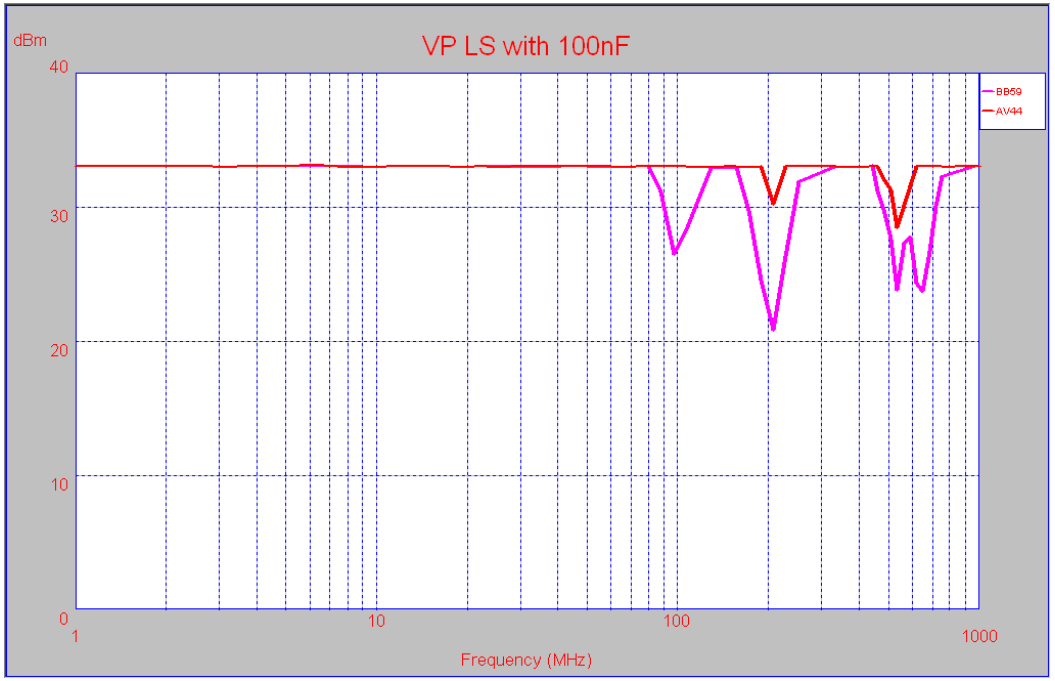
150 Ω on VS pin



NCV7729 DPI Results

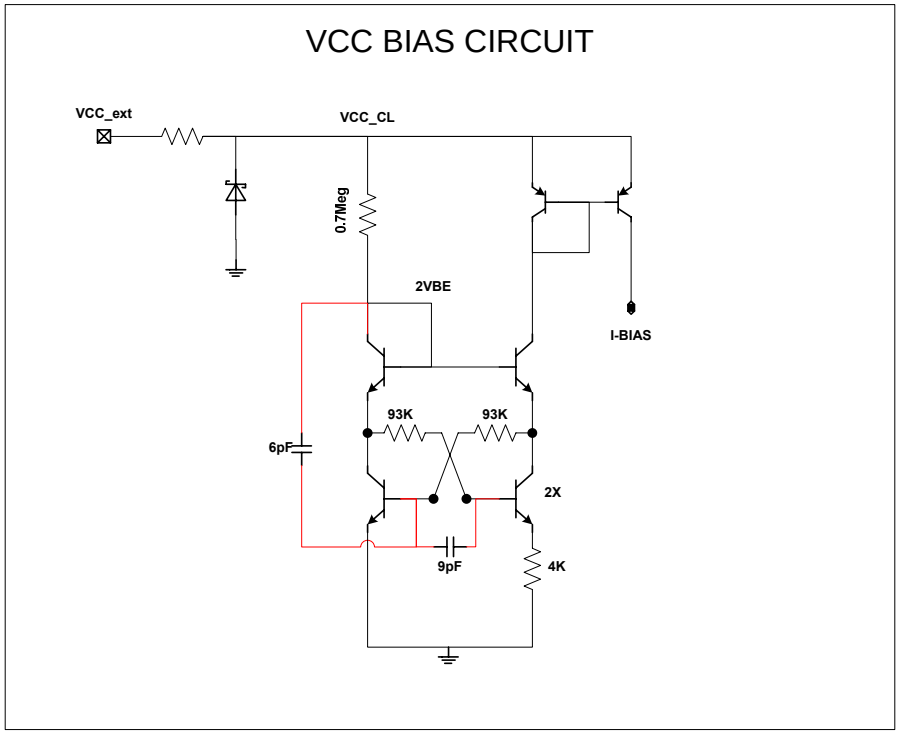
- The device exhibits severe susceptibility at three distinct frequencies during injection on VS pin.
  - 100 Mhz
  - 200 Mhz
  - 600 Mhz

Av44 Vs BB59



Functional Root Cause

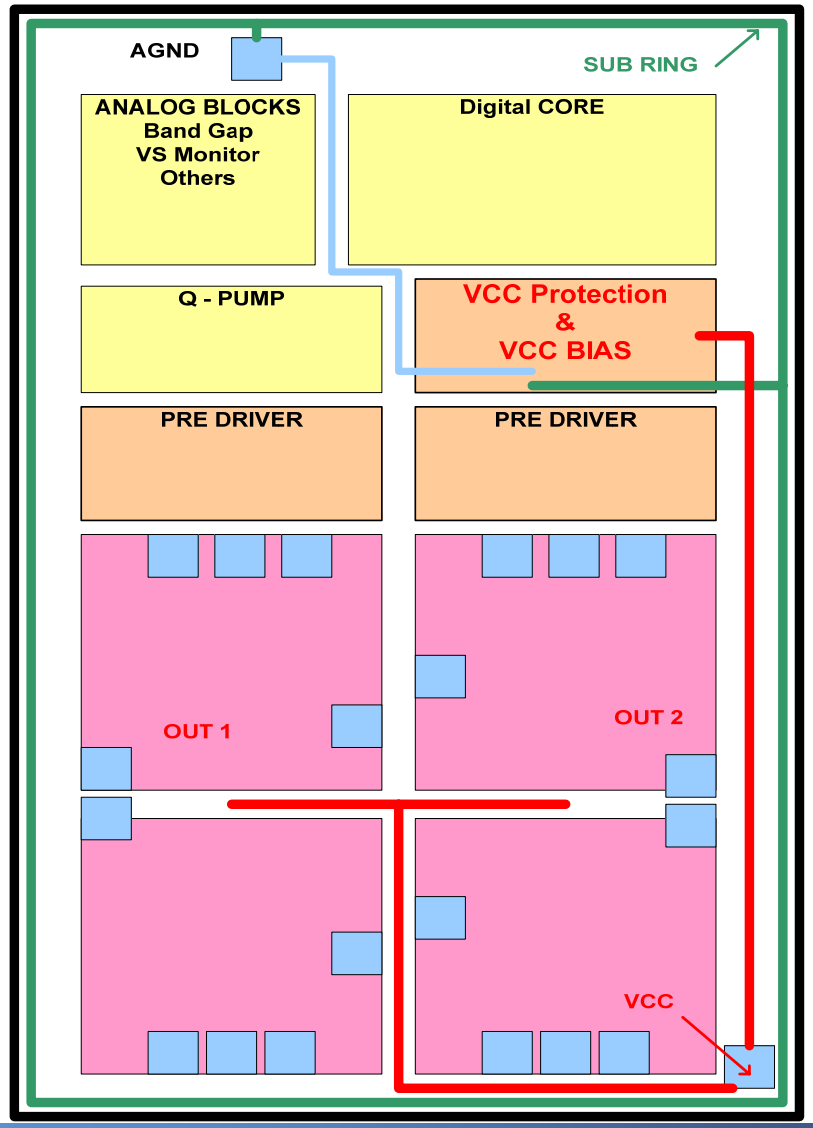
- Functional Root Cause appears to be the death of the ΔVBE/R current source inside the VCC BIAS circuit block.
- The difference in susceptibility of AV44 to BB59 is explained by the capacitors added to the ΔVBE/R bias.
- The same functional behavior was proved to be the root cause during injection on VS, OUT1, and OUT2, throughout the entire frequency range.



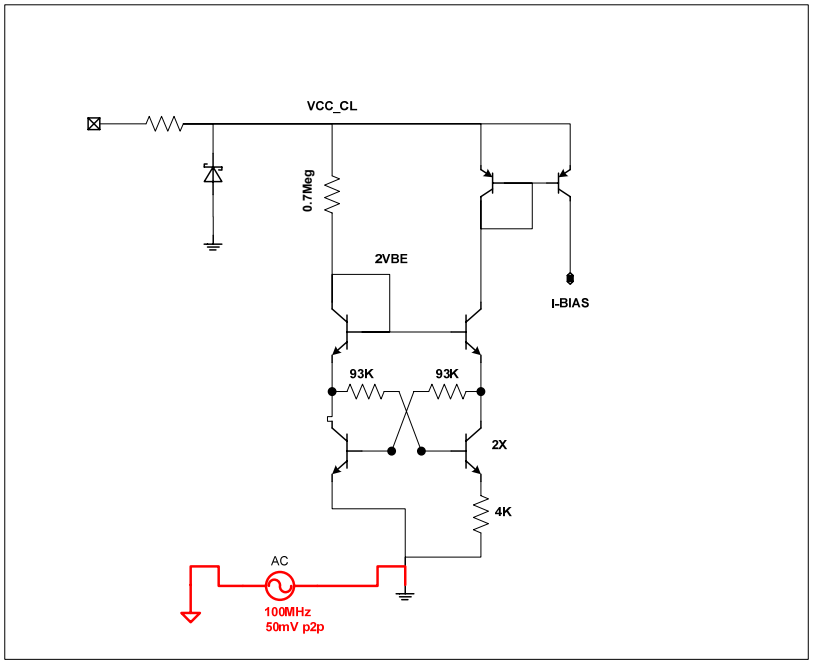
Theory of injection effect

- Injection on VS and OUTx pins injects noise into the substrate thus effecting circuitry that is running on VCC.

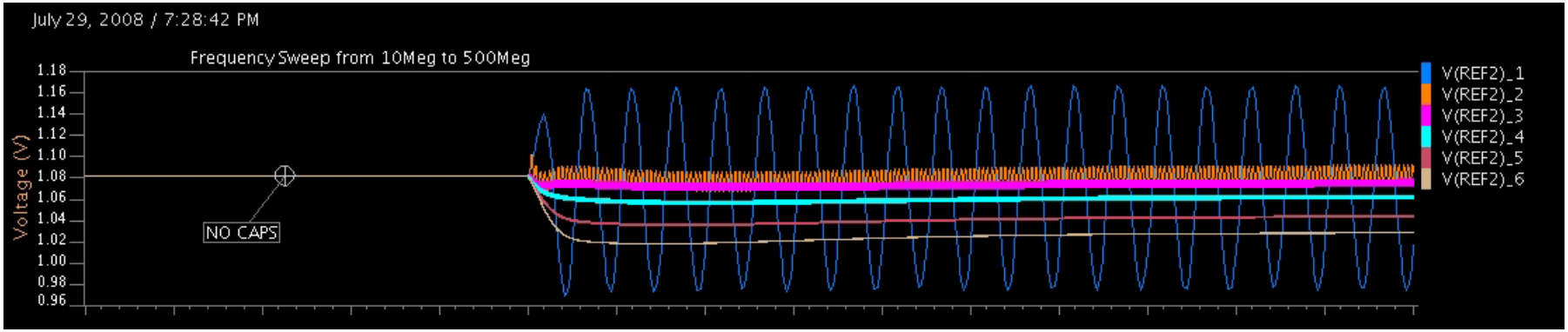
- Voltage difference between SUB and AGND is explained by layout.



ΔVBE/R simulations Sub injection

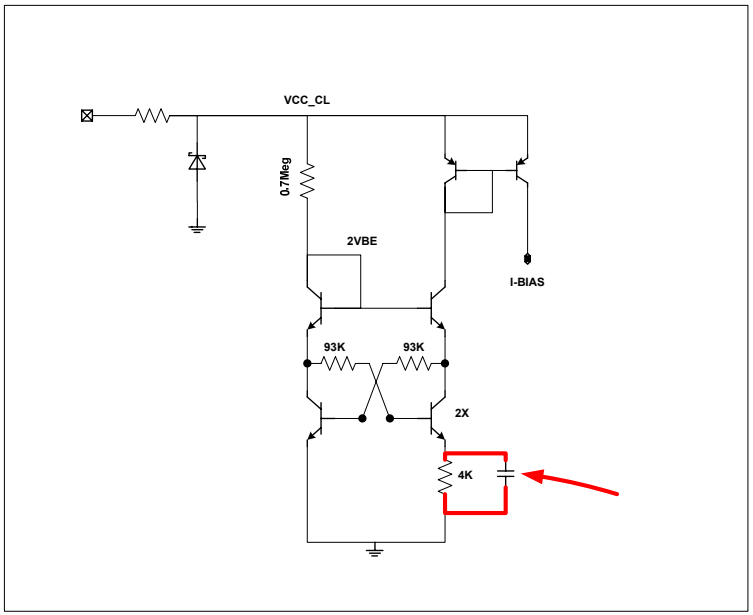


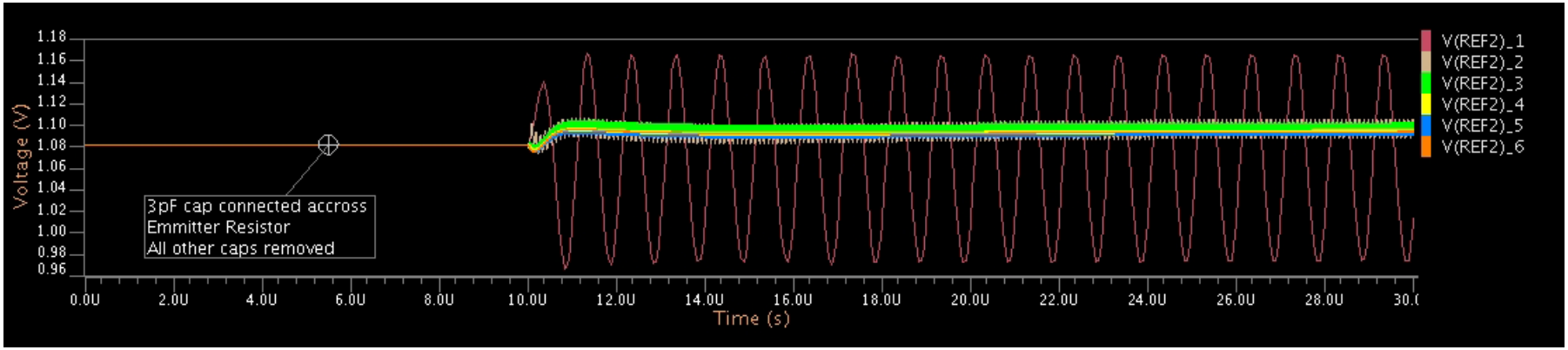
- With 50 mVpp signal the ref can drop from 1.1 V to 1 V.



ΔVBE/R Solution

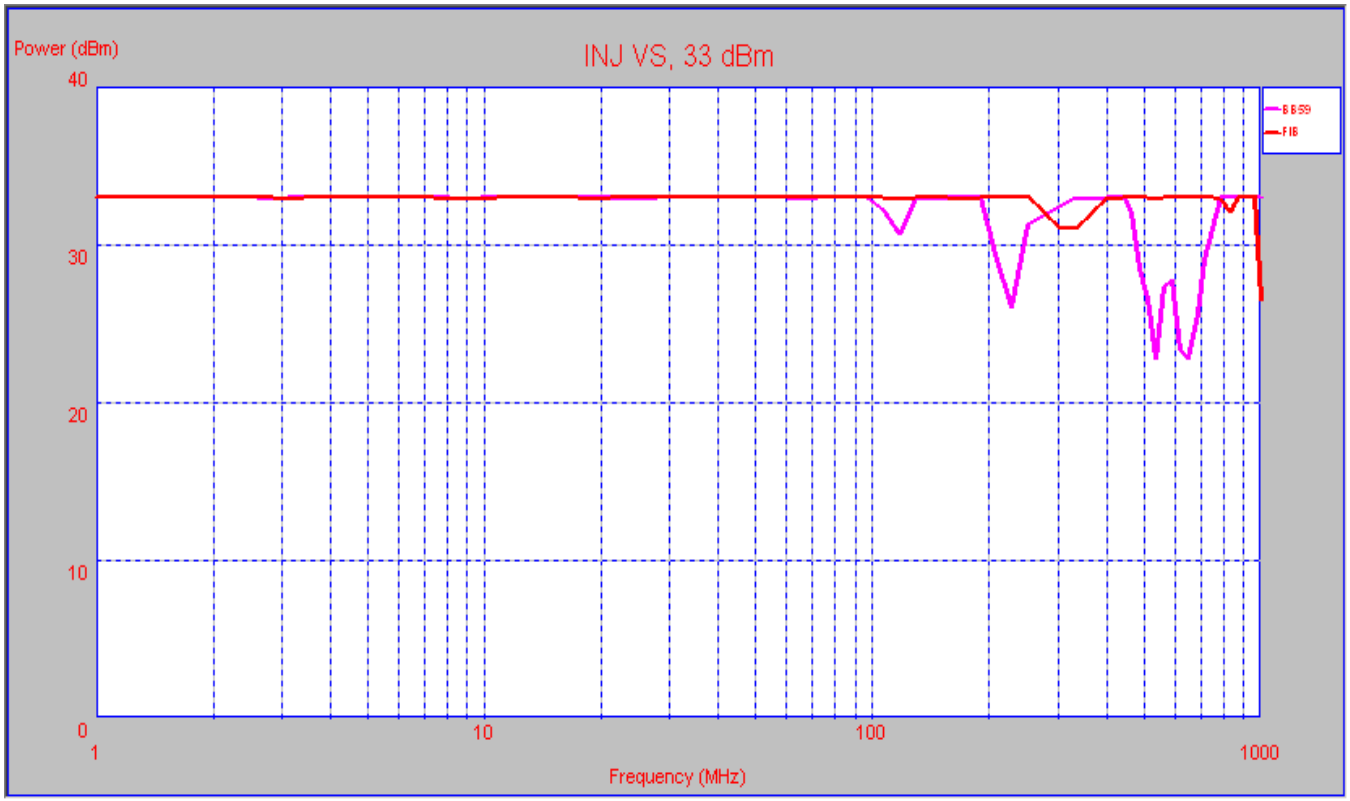
- By balancing the noise on the branches we were able to get a robust bias structure





EMC Conclusion

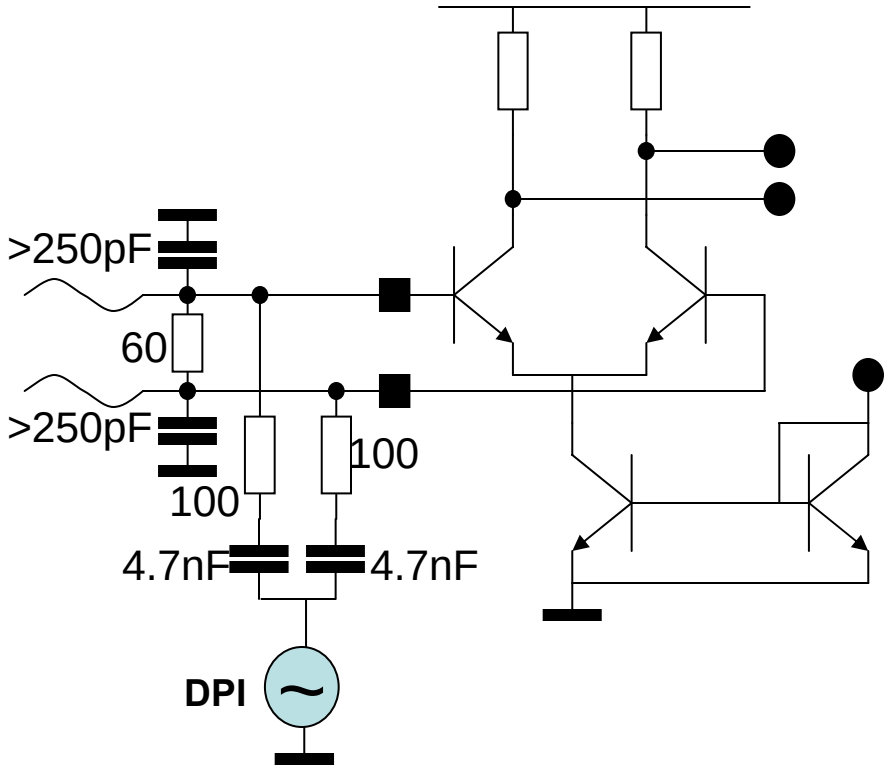
- The susceptibilities at three distinct frequencies during injection on VS pin (100 MHz, 200 MHz, 600 MHz) have been improved



Case Study: IVN

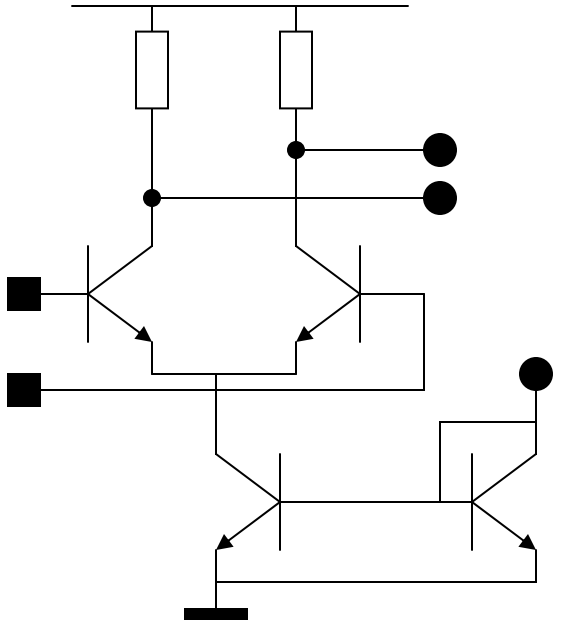
Case Study: Design CAN Receiver

- Requirements:
  - 5 V operation
  - Bit rates up to 1 MB / sec
  - Propagation delay < 200 nsec
  - Zin > 20 kΩ
  - 2 CMP levels in 0.5 V to 0.9 V
  - Hysteresis > 100 mV
  - +7 to –2 V DC input capability
  - Etc…
- Starting topology:
  - Bipolar differential pair
  - High Gm, low offset



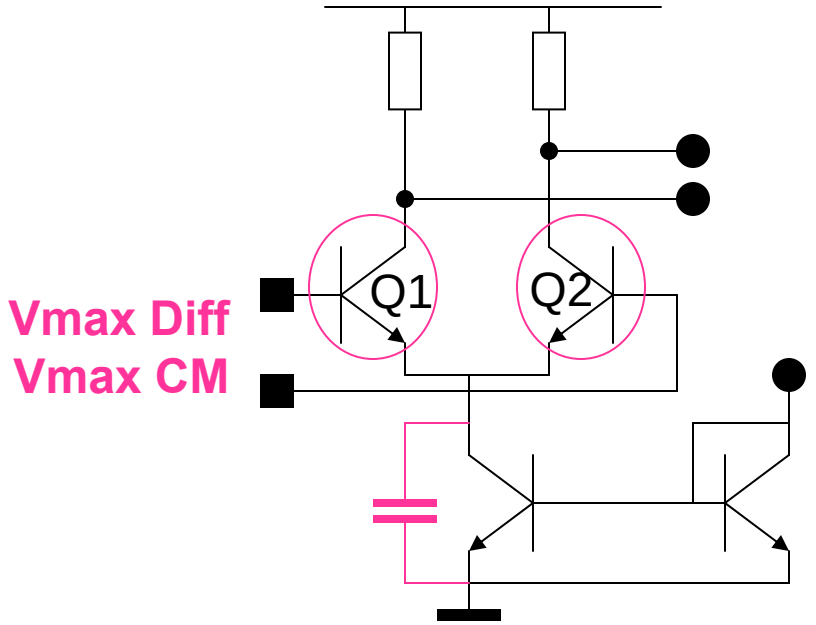
Case Study: Design CAN Receiver

- Step 1: Identify potential rectifiers
  - Most risky: bandwidth limitation



Case Study: Design CAN Receiver

- Step 1: Identify potential rectifiers
  - Most risky: bandwidth limitation
- Step 2: Pass / fail criterion:
  - Eg. DM DC shift |V1 – V2| < 20 mV
  - Eg. CM DC shift V1, V2 < 200 mV
  - Defines max Vemc on Diff pair



Case Study: Design CAN Receiver

- Step 1: Identify potential rectifiers
  - Most risky: bandwidth limitation
- Step 2: Pass / fail criterion:
  - Eg. DM DC shift |V1 – V2| < 20 mV
  - Eg. CM DC shift V1, V2 < 200 mV
  - Defines max Vemc on Diff pair
- Step 3: Impedance + AC analysis
  - Pole at common emitter

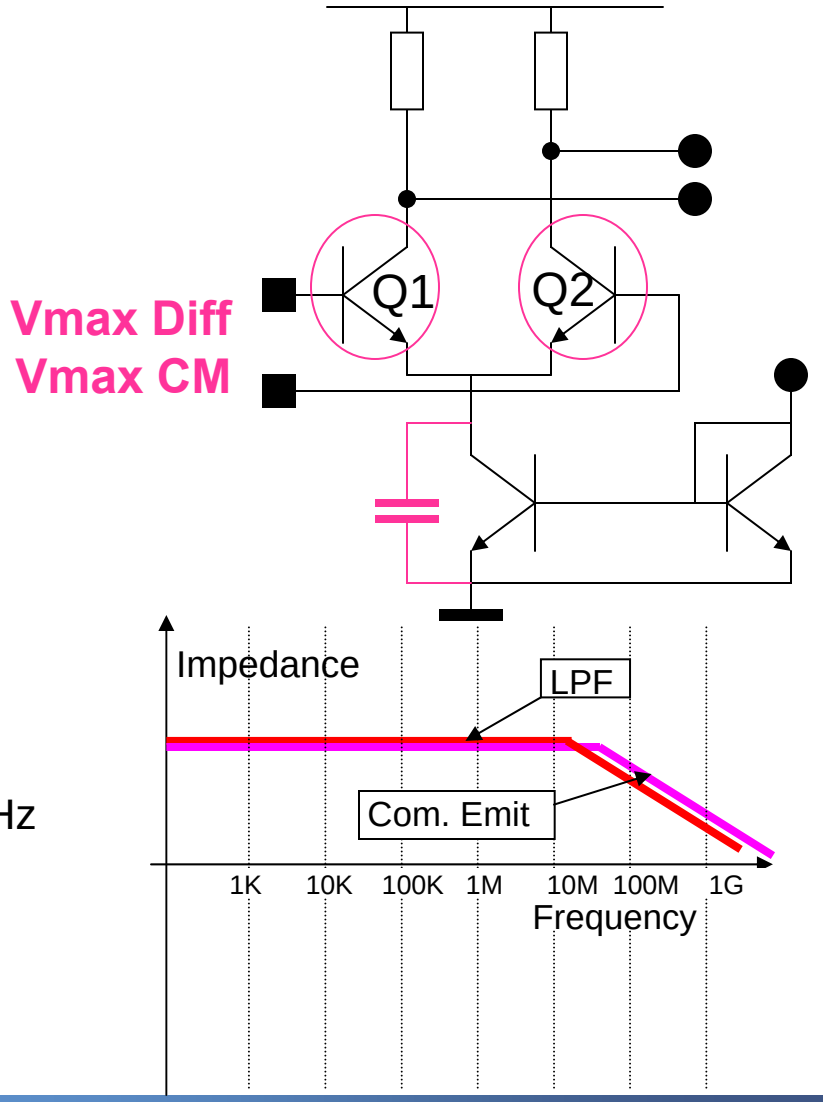
$$F_{-3db} = \frac{Gm}{2 * \pi * C1}$$ ~ 63 MHz (@ Ic=10uA, 1pF)

  - To avoid charge pumping
    - Limit input signal bandwidth << f(pole)
    - Speed requirements allow an LPF >15 MHz with 50% process tolerance

    ⇒ This gives a too low attenuation

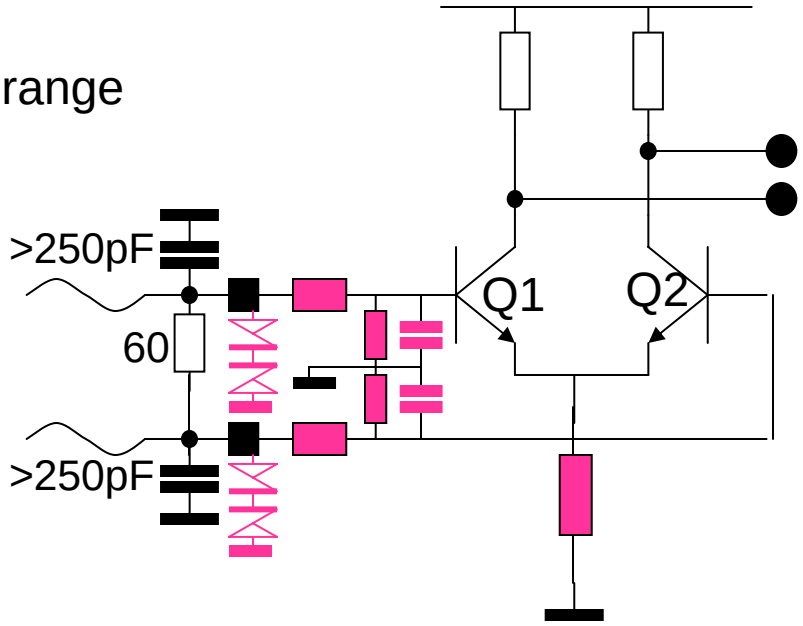
    ⇒ Increase CMP bandwidth

    ⇒ Attenuate the input signal resistively



Case Study: Design CAN Receiver

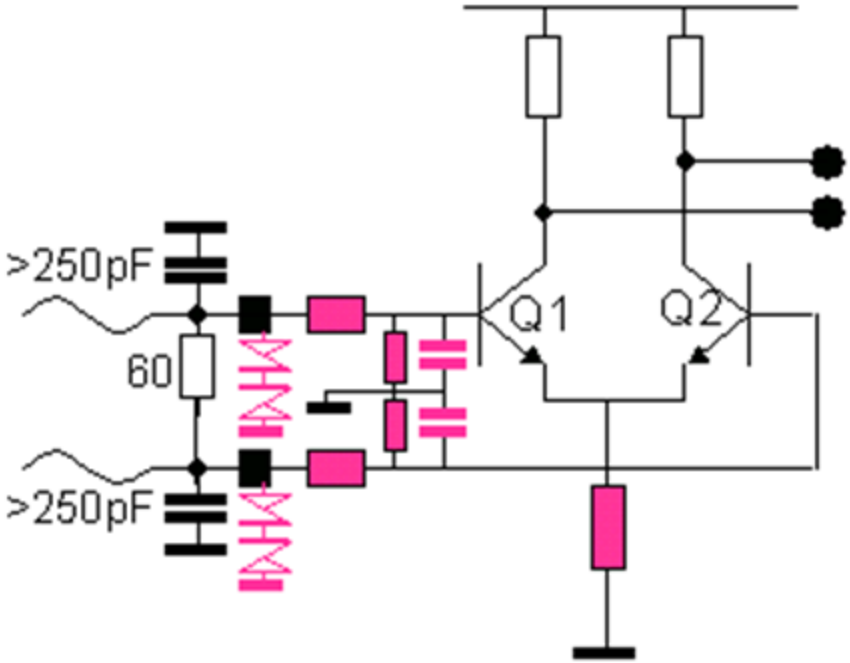
- Step 4: Zin + external components
  - DPI power is common mode, Zin >> 60 Ω
  - Vrms ~45 V peak CM, Mismatch gives also DM
    - LF filtering: NOK due to speed requirements
  - Add strong attenuation at LF !
    - Resistive divider, divide by 25
    - Solves also CM + DM CMP input range
    - Put LPF at 30 MHz
    - Boost bandwidth by Rbias
  - HV ESD protections

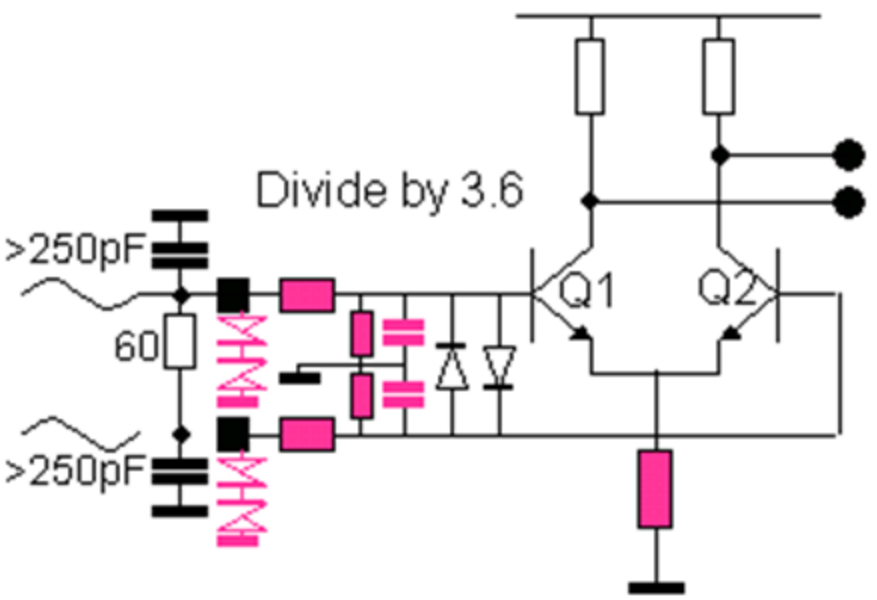


Case Study: Design CAN Receiver

- Better alternative:

Potential circuit solutions





Without clamping:

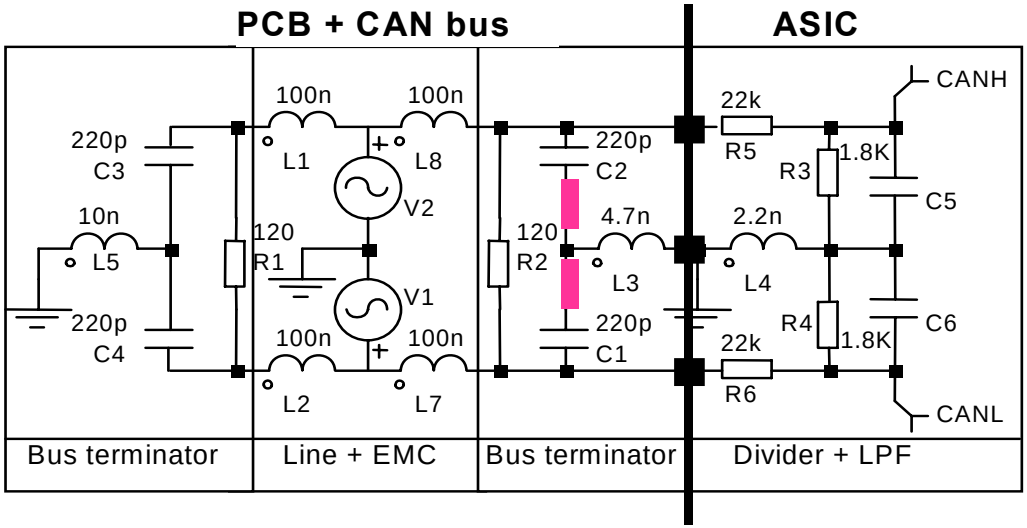
- R-divider factor ~20
- R-divider with matching < 0.1%
- 1st order LPF at 30MHz
- BW of CMP > 300MHz
- ESD protection not conduction in window from –17V to +22V

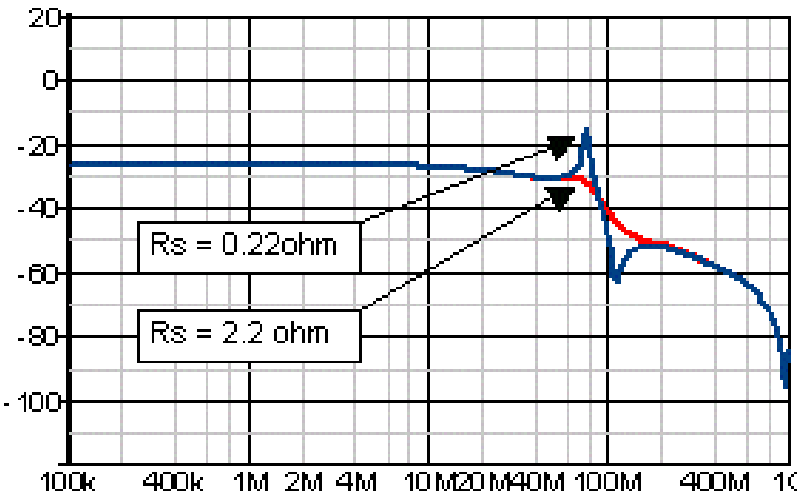
With clamping:

- R-divider factor ~3.6
- R-divider with matching < 0.5%
- 1st order LPF at 30MHz
- BW of CMP > 300MHz
- ESD protection not conduction in window from –17V to +22V

Case Study: Design CAN Receiver

- Step 5: Check for resonance
  - A very basic PCB + package model is used
  - Use PCB back-annotation or “measure”
    - Resonance at ~80 MHz, ~30 dB peak
      - Reduce C1, C2 or L3 (difficult)
      - Add damping resistor(s)





Case Study: Design CAN Receiver

- Step 6: Check by transient simulation
  - *5 frequencies are selected:*
    - *Min and max required EMC frequencies (boundaries).*
    - *Resonance frequency, vulnerable, some soft rectification is expected.*
    - *Comparator pole frequency. No rectification may occur*
    - *LP filter frequency. Frequency where LPF starts to act*

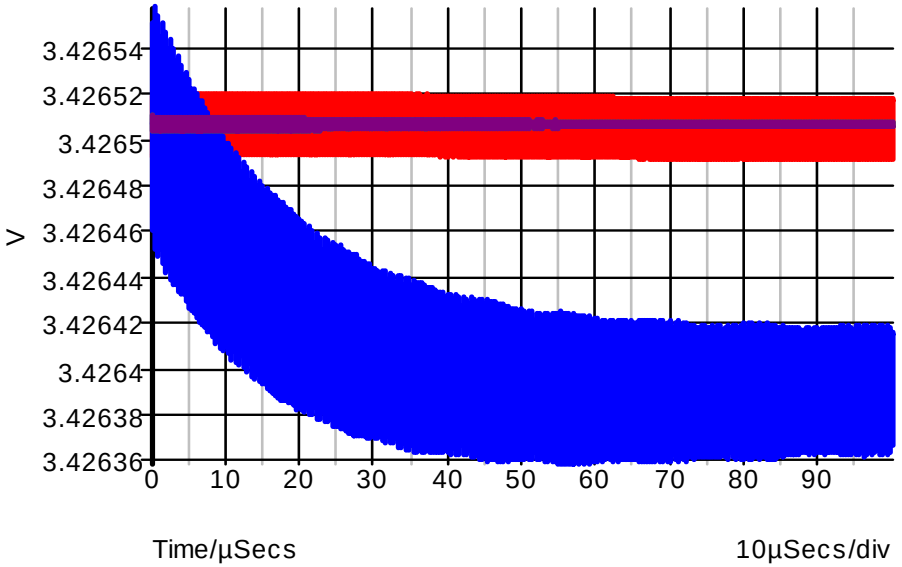


Figure: Transient simulation results
V(Q1_collector) with:
• Femc = 30 MHz (LPF)
• 100 MHz (cmp pole)
• 77.288 MHz (resonance).

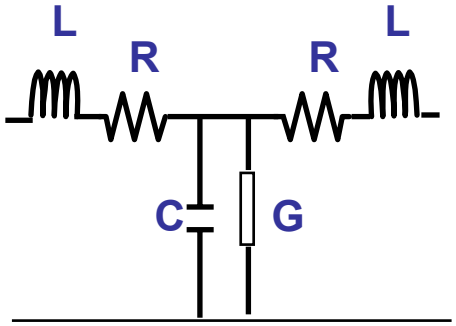
General PCB Guidelines

Why design rules for EMC?

- EMI must reach the conductors in order to disturb the components. This means that the loops, long length and large surface of the conductors are vulnerable to EMI, making the PCB the principal subject of EMC improvements.

PCB tracks are transmissions lines

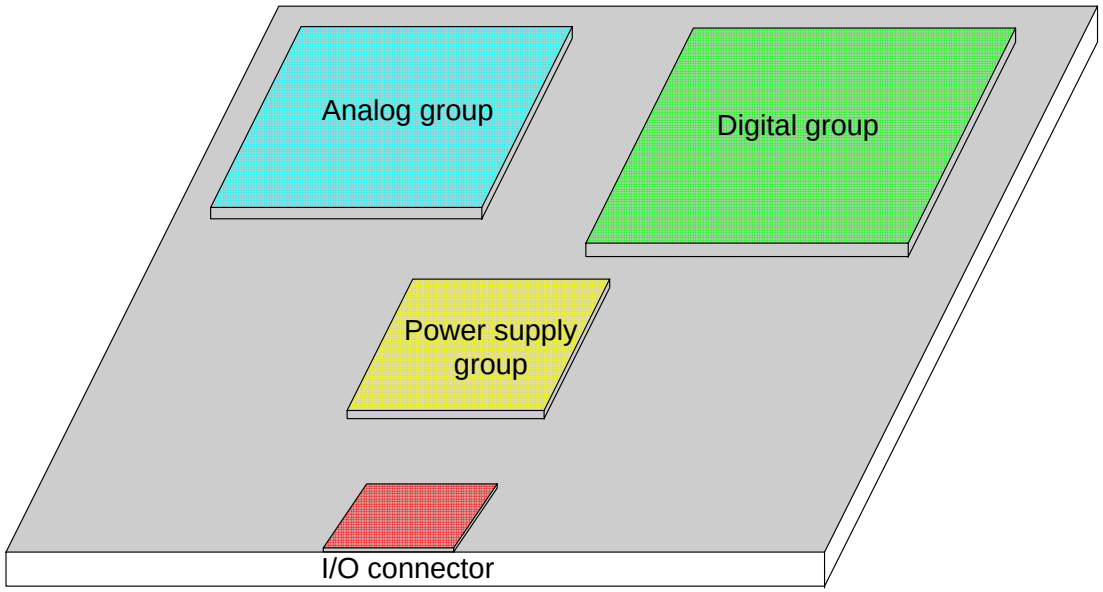
R : resistance Ω / m L : inductance H / m
C : capacitance F / m G : conductance S / m



characteristic impedance $Z = \sqrt{\frac{R + jL\omega}{G + jC\omega}}$

propagation velocity $v = \sqrt{\frac{1}{LC}}$

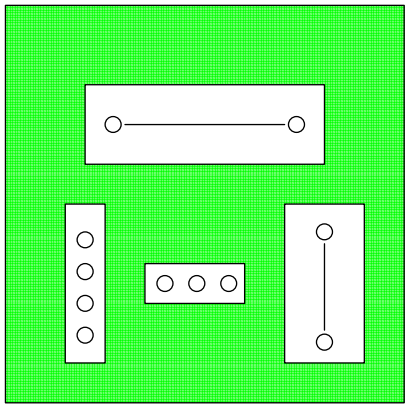
Arrangement of functional groups



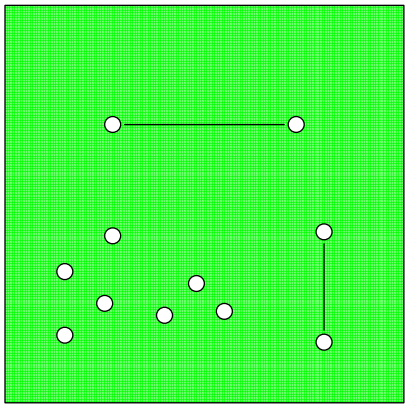
- All components should be placed with an appropriate functional group and their tracks routed within their designated PCB area

Ground Plane

- Place ground plane(s) under all components and all their associated tracks.
- A continuous ground plane with no avoidance
- A good ground plane is achieved by using a complete layer for ground
- Do not cut the ground plane by routing signal lines in GND plane.
- Provide a length / width ratio less than 5 for the PCB. (At a ratio > 5 the inductance of the ground plane increases)



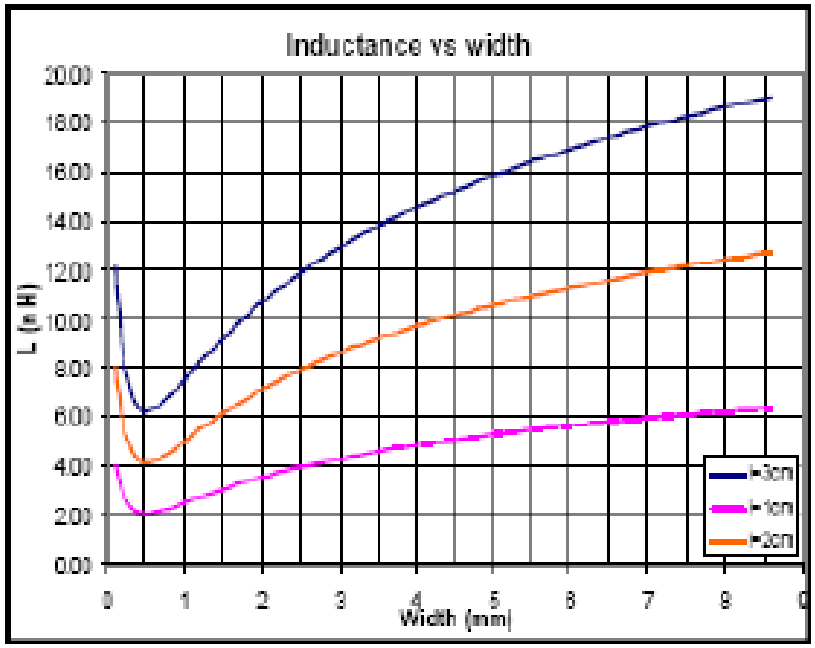
Not acceptable design layout



Acceptable design layout

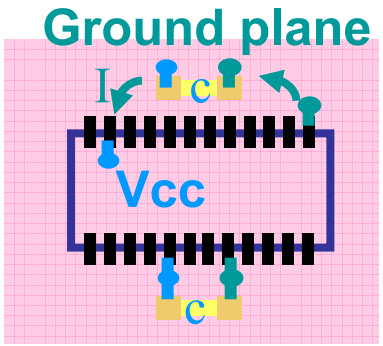
Trace Width

- Connect each component directly to plane.
- Use a via for each component-pin for GND-connection instead of GND-traces.
- Connections to ground must be shorter than 0.5 mm (20 mils).
- Trace widths should be around 20 mils to reduce partial parasitic inductance.

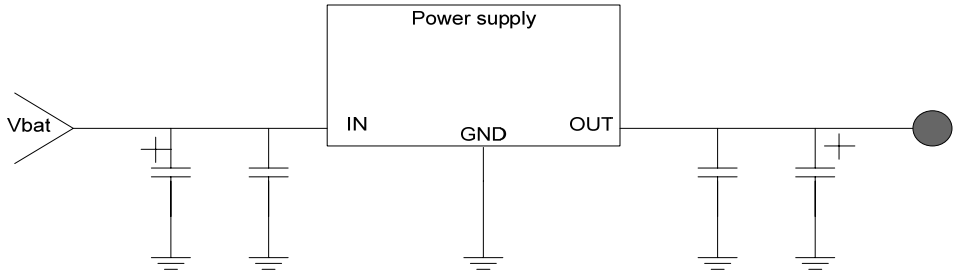


Decoupling Traces

- Decoupling capacitors have to be placed very closely to the VCC and GND pin of the IC.

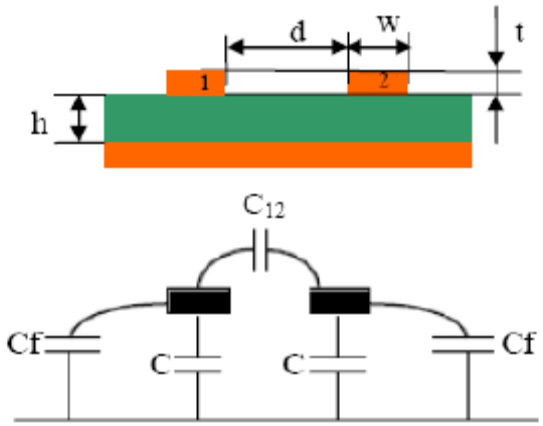


- High-frequency, low-inductance ceramic capacitors should be used for IC decoupling at each power pin. Use 0.1 µF for up to 15 MHz, and 0.01 µF over 15 MHz.



High Switching Current

- Printed circuit board traces which carry high switching current with fast rise/fall times (5 - 10 ns) should maintain at least 3 mm spacing from other signal traces which run parallel to them.



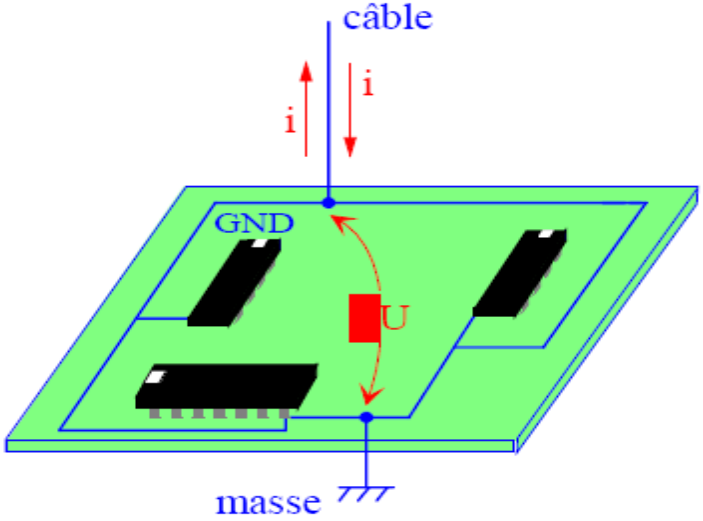
$$C_{12} = k\varepsilon_0 \left\{ \left(\frac{t}{d}\right) + \left[1{,}2\left(\frac{t}{h}\right)^{0{,}1}\right]\left[\left(\frac{d}{h}\right) + 1{,}154\right]^{-2{,}22} + 0{,}253 \ln\left(1 + 7{,}17\frac{w}{d}\right)\left[\left(\frac{d}{h}\right) + 0{,}54\right]^{-0{,}64} \right\} \quad (7)$$

- With high density layout ground guard traces should be placed between them.

PCB Radiated Emission

- Radiated emission is the most important factor in EMC failure and strongly dependant of the PCB design

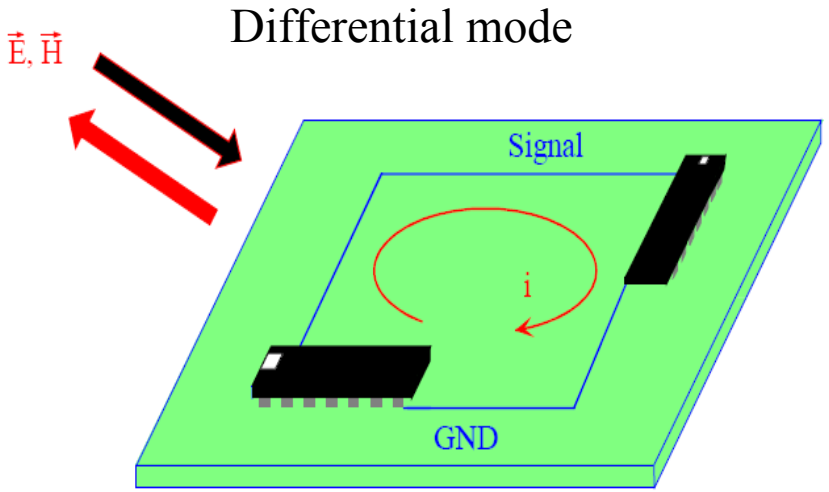
Common mode



Cable length < λ

$$E_c = 4 \cdot \pi \cdot 10^{-7} (f \cdot I \cdot l) \frac{1}{r}$$

Differential mode



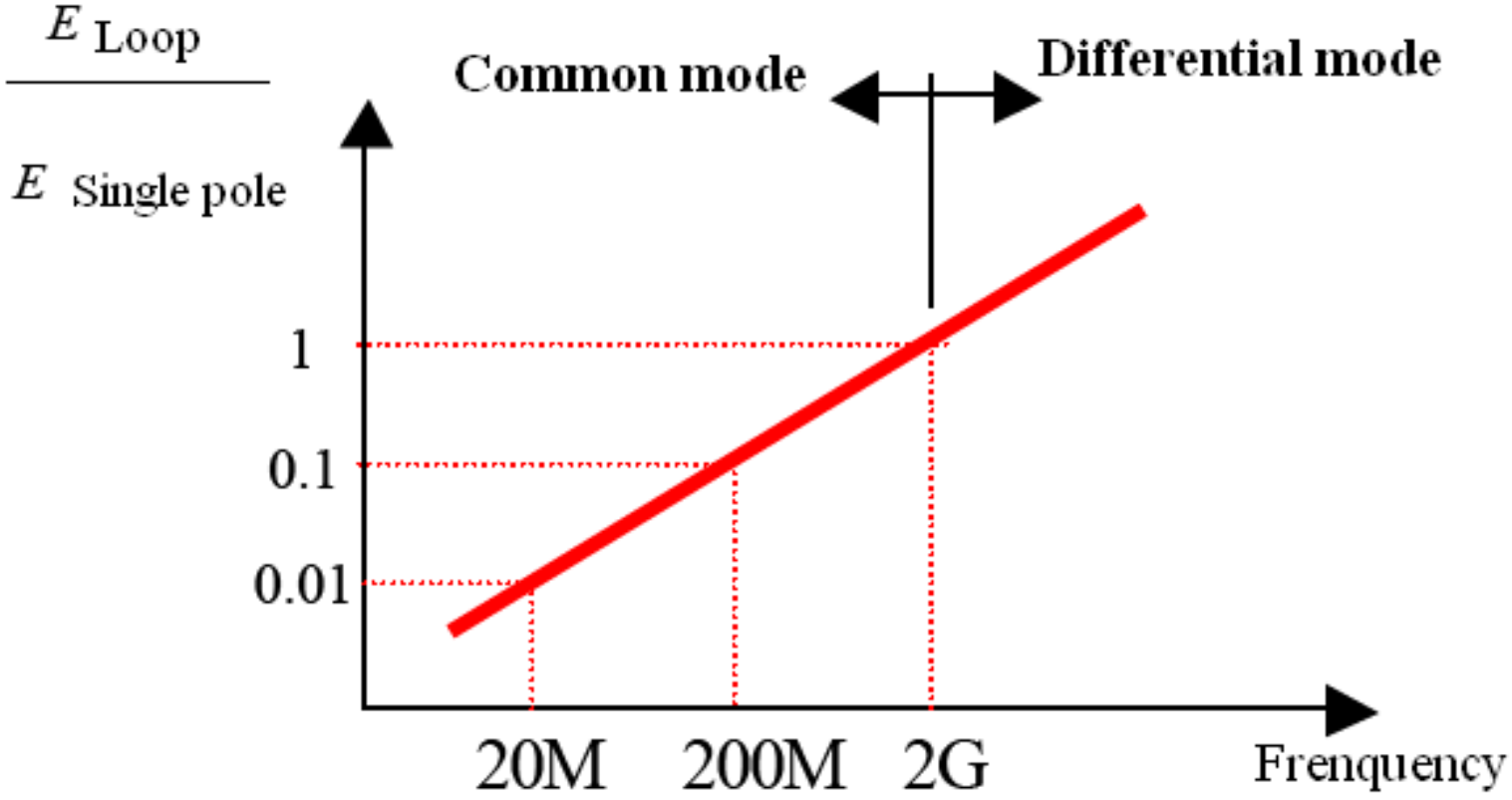
Loop length < ¼ λ

$$E_d = 263 \cdot 10^{-16} \left(f^2 A I \right) \frac{1}{r}$$

A = loop area

PCB Radiated Emission

- Comparison between common mode and differential mode radiated emission



Common mode is the principal source of noise up to 2 GHz

Reduce common mode emission

- Most of the techniques for reducing Differential mode emission can apply to the common mode emission. For example, by using ground plane.
- Reduce the cable length and/or the common mode current reduces the common mode emission
- The common mode radiation is linked to the electric field by the following equation:

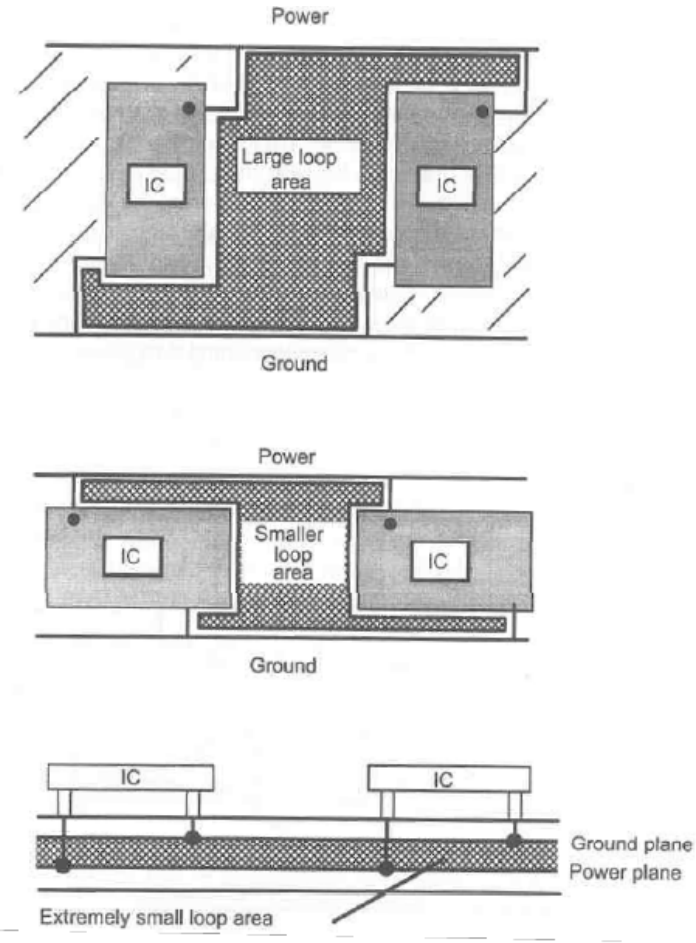
$$I = \frac{0.8 \cdot E \cdot r}{f \cdot l}$$

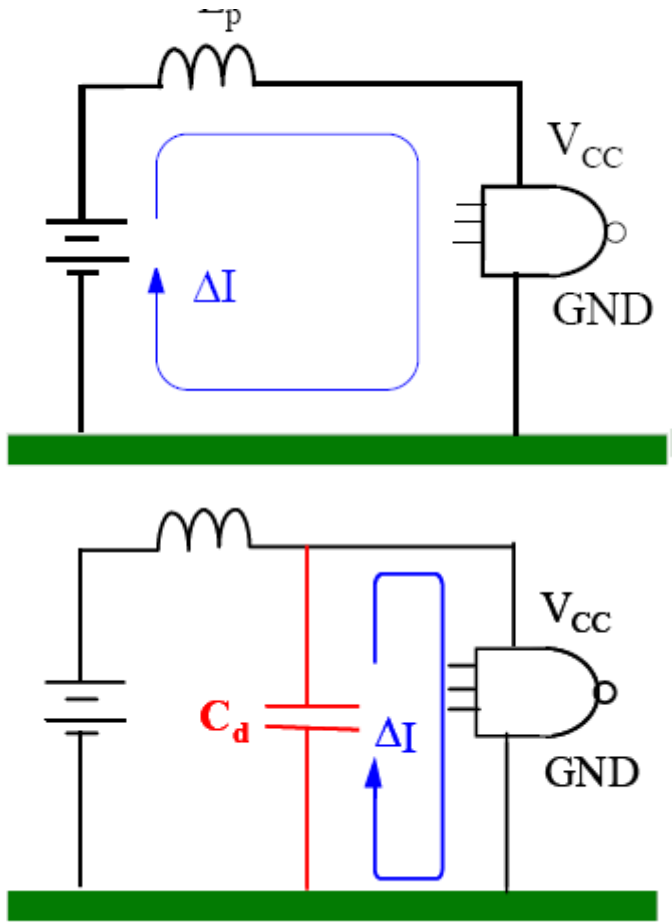
$I\,(\mu\mathrm{A}), E\,(\mu\mathrm{V/m}), f\,(\mathrm{MHz}), r\ and\ l\,(\mathrm{m}).$

- For example, to limit the radiated emission, 3 m distance at 100 uV/m with 1 m cable length.
- Maximum current in common mode should be 15 uA. (This the maximum current due to the voltage drop in the circuit)

Reduce differential mode emission

- Based on the equation, Ed is proportional to the current in the loop (I) and the loop area (A).





Conclusions

- Changes in our modern world:
  - Strong increase in HF signals (more & faster PC's, uP's in about everything, more & faster networks, ADSL, GPS, satellite TV/radio etc…)
  - More and more mobile systems (eg. mouse + keyboard of a PC, Bluetooth, GPS, GSM, TV, radio, PDA, iPod…)
  - Everything gets more compact, merge sensitive and harsh environments together on 1 die
- Car electronics evolved from comfort applications
  - Interior light, radio, heating, climate control, electronic windows etc…
- to safety improving applications
  - Central door locks, light-on warning etc…
- to today also safety critical applications
  - Drive by wire, Engine control, Airbag, In vehicle networking, ABS, Cruse control etc…

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting automotive applications at www.onsemi.com/automotive