ON Semiconductor®

Effective Automotive Quality

4 Pillars


Quality
D·O·M·SVB·INVOC·S·M·MAGDALENAE
Prevent
Promote
Produce
Progress

Agenda

- Prevent
  - Certification
  - APQP
  - AEC-Q100
- Promote
  - Quality democratisation
- Produce
  - Early failure rate control : DVS, PAT, SBA
  - Monitoring
- Progress
  - Failure analysis labs

4 Pillars

Issue Cost Analysis Model

Issue Identification

Reactive

Proactive

Prevention Detection

Issue Resolution

ON Semiconductor Quality & Environmental System Certified


CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of

ON Semiconductor
SCG Philippines Inc.
Bo Maduya, Governor's Drive
Carmona, Cavite 4116, Philippines

has been approved by Lloyd's Register Quality Assurance, Coventry, West Midlands, UK, to the following Quality Management System Standard

ISO/TS 16949:2002

The Quality Management System is applicable to:

Design of Integrated Power Devices, Analog & Power Management Products, Standard Component Products and Clock & Data Management Products.
Manufacture of Semiconductors.

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval Certificate No: UQA 0111883/F — Original ISO/TS 16949 Approval: August 2, 2001
Current Certificate: August 3, 2008
Certificate Expiry: December 13, 2009


CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of

ON Semiconductor
Phoenix, Arizona, USA

has been approved by Lloyd's Register Quality Assurance to the following Quality Management System Standards

ANSI/ISO/ASQ Q9001-2000,
ISO 9001:2000

The Quality Management System is applicable to:

Design of Integrated Power Devices, Analog & Power Management Products, Standard Component Products, and Clock & Data Management Products Including Design, Reliability and Diagnostic Laboratories.

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval Certificate No: UQA 0111883/A — Original Approval: July 15, 1998
Current Certificate: December 15, 2008
Certificate Expiry: December 14, 2009

Issued by: LRQA Inc, Houston

ANAB


CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of

ON Semiconductor
2300 Buckskin Road
Pocatello, Idaho 83201, USA

having been audited in accordance with the requirements of AS9104A has been approved by Lloyd's Register Quality Assurance to the following Quality Management System Standards

ISO 9001:2000
AS 9100:2004 Rev.B

The Quality Management System is applicable to:

Design and Manufacture of Custom Integrated Circuits (ASICs).

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval Certificate No: UQA 4000711/A — Original ISO Approval: July 14, 2008
Original AS Approval: July 14, 2008
Current Certificate: July 14, 2008
Certificate Expiry: July 13, 2011

ANAB


CERTIFICATE OF APPROVAL

This is to certify that the Quality Management System of

ON Semiconductor
Phoenix, Arizona, USA

has been approved by Lloyd's Register Quality Assurance to the following Environmental Management System Standard

ISO 14001:2004

The Environmental Management System is applicable to:

Manufacturing Operations including Wafer Fabrication, Assembly and Test of Semiconductor and Electronic Components as Well as Support Operations

This certificate is valid only in association with the certificate schedule bearing the same number on which the locations applicable to this approval are listed.

Approval Certificate No: UQA 4000711/E — Original Approval: October 15, 2004
Current Certificate: October 15, 2008
Certificate Expiry: October 14, 2011

ANAB

ISO/TS 16949:2002
8 Fabs
4 Assembly/Test Sites
8 Design Centers
Global Distribution
Corporate HQ

ISO 9001:2000
7 Fabs
2 Assembly/Test Sites
12 Design Centers
7 Sales Sites
Global Distribution
Corporate HQ

AS 9100:2004
1 Fab
2 Design Centers

ISO 14001:2004
8 Fabs
4 Assembly/Test Sites
Corporate HQ

ALSO: MIL-PRF-38535, CTPAT, STACK

Certificates and Schedules can be viewed or downloaded at:
http://www.onsemi.com/PowerSolutions/content.do?id=1156

PPAP : Production Part Approval Process

- PPAP provides the methods, procedures and forms to enable the preparation of a component' documentation required for submission and the approval from customers when required.
- The purpose of the PPAP is to ensure that suppliers of components comply with the design specification and can run consistently without affecting the customer line and improving the quality systems.
- PPAP ensures that you will achieve the first time quality and will lower down the cost of quality.

PPAP Elements (Rev 4)

PPAP#	PPAP ITEM	PPAP#	PPAP ITEM
·B0	Table of Contents; Purpose/ Background Statement; PPAP Checklist	·B9.1	Dimensional Results- Cpk to Customer Dimension Outline (Default to ON Semi Dimension Outline)*Critical/ Key parameters
·B1.1	Design Records- Customer Spec	·B9.2	Dimensional Results- Noncompliance report for Cpk<1.33
·B1.2	Design Records- ON Semi Spec	·B10	Records of Performance Test Results- Summary Reliability Test Rpt
·B2	Authorized Engineering Change documents (ie Automotive Change Notification Docs-Customer Specific Form/ Internal Customer Documentation)	·B10.1	Characterization data (Test Results- Noncompliance report for Cpk <1.33 on critical/key items) Note: 1 or 3 lots/ 25pcs as applicable
·B2.1	Change Document- Cof DC B3 Customer Engineering Approvals (note- PEO/Plant approval may also be required)	·B11	Initial Process Studies Performance Cpk for Critical/Key parameters (Front-end for Wafer changes; Back-end for Assy/Test changes)
·B4	FMEA- Design (if applicable)-	·B11.1	Process Performance- see additional comments
·B5	Process Flow Chart-High Level	·B12	Qualified Laboratory Documentation
·B6	FMEA- Process (Front-end for Wafer changes; Back-end for Assy/Test changes)	·B13	Appearance Approval Report- N/A for Semiconductors
·B7	Control Plan (Front-end for Wafer changes; Back-end for Assy/Test changes)	·B14	Sample Production Parts (for customer, if requested)
·B8	Measurement System Analysis Studies (Front-end for Wafer changes; Back-end for Assy/Test changes)	·B15	Master Samples-If required
·B8.1	Measurement System Analysis- Noncompliance report for gage tools with R&R's >10%	·B16	Checking Aids- N/A for Semiconductors
·B9	Dimensional Results -Customer Pkge Outline (Default to ON Semi print)	·B17	Customer Specific Requirements
·B18	**Product Submission Warrants (PSW)**		

PPAP : Part Submission Warrant (PSW)

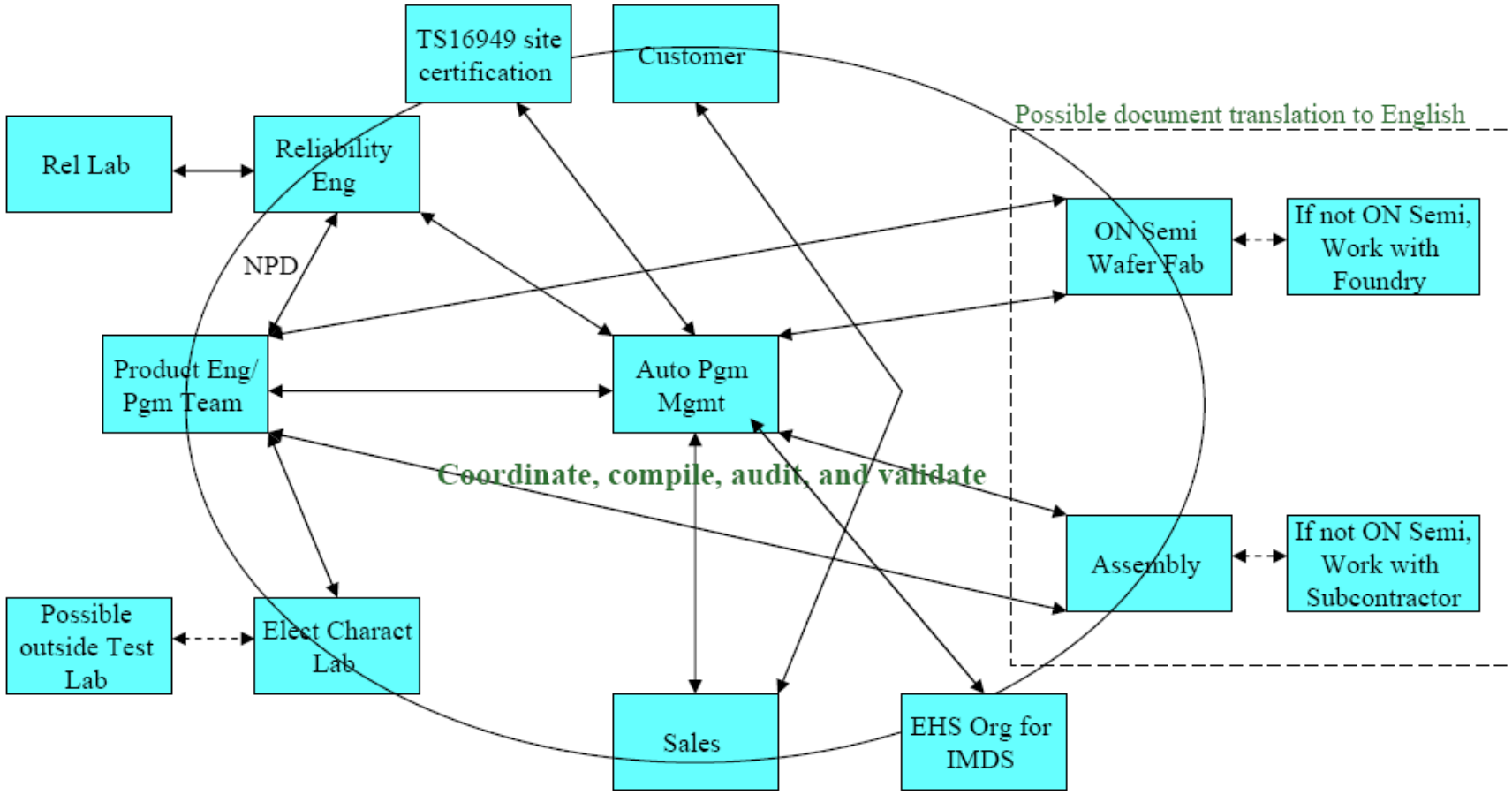
- PSW has 5 levels:
  - **Level 1** - Warrant only submitted to customer (similar to certificate of compliance document, it warrants all the requirements within a PPAP as compliant)..

    → PPAP level 1: 1 to 10 days depending on verification of the part being compliant, capable and workload
  - Level 2 - Warrant with product samples and limited supporting data submitted to customer.
  - **Level 3** - Warrant with product samples and complete supporting data submitted to customer.

    → PPAP level 3: 4 to 6 weeks average*, should be under customer APQP process with typically 6-12 months timing prior to need date.
  - Level 4 - Warrant and other requirements as defined by customer.
  - Level 5 - Warrant with product samples and complete supporting data reviewed at supplier's manufacturing location.

PPAP:ON Semiconductor Integrated Process

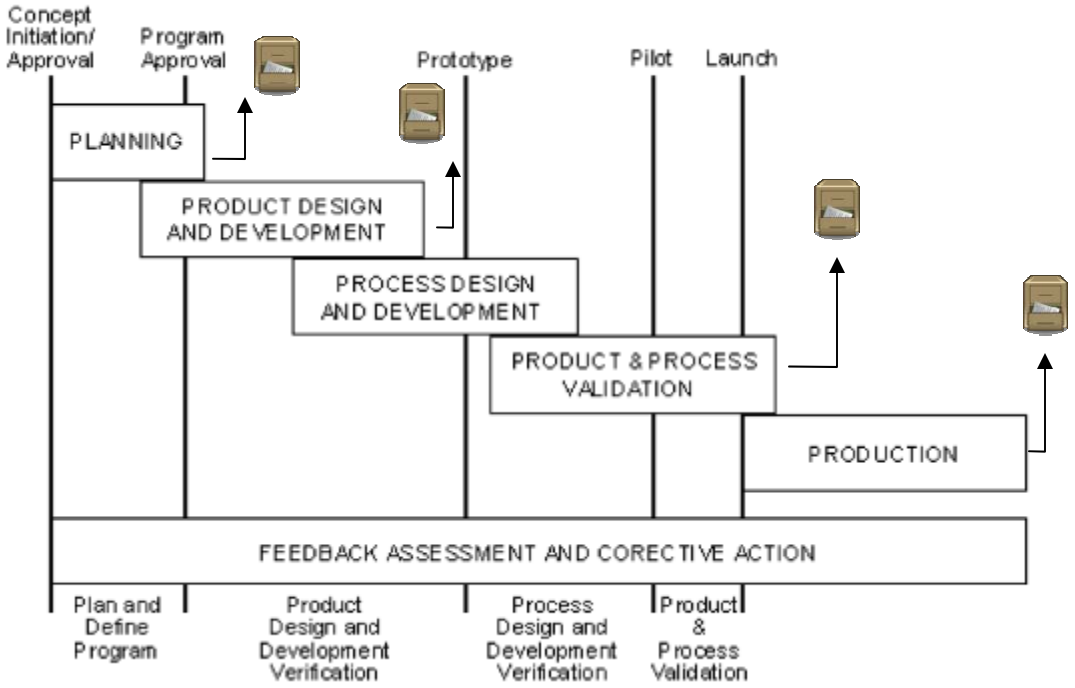
PPAP Level 3 preparation flow (after part has been verified compliant, capable and meets business case)-



PPAP Level 3 is not free and consumes a lot of disciplines time and resources ($$) to assemble.

APQP : Advanced Planning Quality Process

- **Proactivity in product development**



PPAP Filing : Goals, Specifications, Studies, Plans, Results... are documented and filed at the end of each phases to prepare the PPAP

Reliability Testing

- ON Semiconductor's Product/Process Qualification is covered by 12MSB17722C Specification.

ON Semiconductor®

QS WORLDWIDE INSTRUCTION

Title: Reliability Qualification Process	Document Number: 12MSB17722C Page 1 of 37	Revision: T
APPLICABLE TO LOCATION(s): GLOBAL	OWNER (GROUP OR DEPARTMENT): Manufacturing	

Purpose and Scope

1.1 The purpose of this specification is to establish the baseline reliability test requirements for all ON Semiconductor product and process qualifications. Successful completion of these requirements will demonstrate the capability of the product or manufacturing process to meet specified electrical and reliability expectations. The qualification requirements described in this specification represent a subset of the total production release requirements.

1.2 This document applies to all products manufactured by ON Semiconductor product businesses, operations, wafer fabrication, and assembly manufacturing locations, as well as products sold by ON Semiconductor through Buy-Sell agreements.

AEC (Automotive Electronics Council) Specifications

- **Q100 (IC- initial release in June 1994; current Rev G May 2007)**
  - Automotive IC ambient temperature ranges: **Grade 0: -40 C to +150 C** Grade 1: -40 C to +125 C Grade 2: -40 C to +105 C Grade 3: -40 C to +85 C Grade 4: 0 C to +70 C
- **Q101 (Discrete- initial release in May 1996; current Rev C June 2005)**

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality /reliability in the application.

- General Comments
  - 1. AEC contains the minimum guidelines to cover a broad range of semiconductors.
  - 2. AEC targeted product lifetime is targeted 10-15 years versus most consumer products lifetime <3 years.
  - 3. AEC does not replace sound reliability engineering, it compliments it.
  - 4. The AEC documents do not relieve the supplier of their responsibility to meet their own company's internal qualification program.
  - 5. Customer specific requirements may supersede AEC guideline

Reliability Testing

- Required Tests are identified by Market Segment and meet applicable JEDEC, AEC, and Military Standards

Table 4: Extrinsic Reliability Requirements for Discretes and ICs, by Market Segment.

	Market							
	Consumer		Industrial		Automotive		Military	
	IC Tj(max op)=85°C	Discrete Tj(max op)=125°C	IC Tj(max op)=125°C	Discrete Tj(max op)=150°C	IC (Grade 1) Tj(max op)=125°C	Discrete Tj(max op)=by app	IC	Discrete
Stress Test								
HTOL*	77 Units/Lot 504 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=125°C	NA	77 Units/Lot 504 Hours Tj(stress)=150°C	NA	77 Units/Lot 504 hrs@Tj=150°C or 1008 hrs@Tj=125°C	NA
HTRB*	NA	77 Units/Lot 504 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=Tj(max op)	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C
HTGB*	NA	77 Units/Lot 504 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=Tj(max op)	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C
HTBB* VHVIC only	77 Units/Lot 504 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=125°C	NA
HVTHB* VHVIC only	77 Units/Lot 168 Hours Tj = 85 °C/60% RH		77 Units/Lot 168 Hours Tj = 85 °C/60% RH		77 Units/Lot 168 Hours Tj = 85 °C/60% RH		77 Units/Lot 168 Hours Tj = 85 °C/60% RH	
ELFR	NR	NA	500 Units/Lot 48 Hours Tj(stress)=150°C	NA	800 Units/Lot 48 Hours Tj(stress)=150°C	NA	NA	NA
HTSL*	77 Units/Lot 504 Hours Ta(stress)=150°C	77 Units/Lot 504 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C	77 Units/Lot 1008 Hours Ta(stress)=150°C
NVM Endurance and Data Retention* HTSL	77 Units/Lot 504 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA
HTOL	77 Units/Lot 504 Hours Tj(stress)=125°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA	77 Units/Lot 1008 Hours Tj(stress)=150°C	NA

Reliability Testing

- Required Tests continued…

PC surface mount only	Appendix D	Appendix D	Appendix D	Appendix D	Appendix D	Appendix D	Appendix D	Appendix D
TC*	77 Units/Lot 500 cycles -55 to 150 °C	77 Units/Lot 500 cycles -55 to 150 °C	77 Units/Lot 500 cycles -65 to 150 °C	77 Units/Lot 500 cycles -65 to 150 °C	77 Units/Lot 1000 cycles -55 to 150 °C	77 Units/Lot 1000 cycles -55 to 150 °C	77 Units/Lot 500 cycles -65 to 150 °C	77 Units/Lot 500 cycles -65 to 150 °C
IOL	NA	77 Units/Lot Per AEC Q101 Table 2A Mid Read Point	NA	77 Units/Lot Per AEC Q101 Table 2A Final Read Point	NA	77 Units/Lot Per AEC Q101 Table 2A Final Read Point	NR	77 Units/Lot Per MIL STD 750 Method 1036
AC or UHAST*	77 Units/Lot 48 hrs	77 Units/Lot 48 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs
HAST*	77 Units/Lot 48 hrs	77 Units/Lot 48 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs	77 Units/Lot 96 hrs
THB in lieu of HAST*	77 Units/Lot 504 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs	77 Units/Lot 1008 hrs
H^3TRB in lieu of HAST	NA	77 Units/Lot 1008 Hours 85°C/85%RH	NA	77 Units/Lot 1008 Hours 85°C/85%RH	NA	77 Units/Lot 1008 Hours 85°C/85%RH	NA	Moisture Resistance MIL STD 750 Method 1021
Mechanical Shock hermetic packages only	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA
Variable Frequency Vibration hermetic packages only	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA
Constant Acceleration hermetic packages only	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA
Gross/Fine Leak hermetic packages only	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA	39 Units/Lot	NA
Construction Analysis	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes	Platform or Topographical Changes

Reliability Testing

- Required Tests continued…

Manufacturing Data	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test	5 Units/Lot/Test
Board Level Drop Test handheld applications only	15 Units/Lot	15 Units/Lot	15 Units/Lot	15 Units/Lot	15 Units/Lot	15 Units/Lot	15 Units/Lot	15 Units/Lot
Electrical Characterization	30 Units/Lot	30 Units/Lot	30 Units/Lot	30 Units/Lot	30 Units/Lot	30 Units/Lot	30 Units/Lot	30 Units/Lot
ESD - HBM	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.
CDM	5 Units/Lot	5 Units/Lot ESD Protected Devices only. Not required on pkgs smaller than SO8	5 Units/Lot	5 Units/Lot ESD Protected Devices only. Not required on pkgs smaller than SO8	5 Units/Lot	5 Units/Lot ESD Protected Devices only. Not required on pkgs smaller than SO8	5 Units/Lot	5 Units/Lot ESD Protected Devices only. Not required on pkgs smaller than SO8
MM	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.	5 Units/Lot	5 Units/Lot ESD Protected Devices only.
Latch-up - LU (+)	6 Units/Lot	NA	6 Units/Lot	NA	6 Units/Lot	NA	6 Units/Lot	NA
LU (-)	6 Units/Lot	NA	6 Units/Lot	NA	6 Units/Lot	NA	6 Units/Lot	NA

Note: Manufacturing Data includes: Package Drop, Lid Torque, Die Shear, Internal Water Vapor, Bond Shear, Bond Pull, Solderability, Physical Dimensions, Ball Shear, and Lead Integrity, as appropriate.

Reliability Testing

- Required Tests continued…

Table 5: Intrinsic Reliability Requirements by Qualification Category.

	Platform Qualification		Base Qualification		Qualification by Similarity	
	IC	Discrete	IC	Discrete	IC	Discrete
Electromigration or Isothermal Electromigration	1 Lot Mandatory	NR	Required if Process Module Affected	NR	Use Generic Platform Data	NR
Stress Migration	1 Lot Mandatory	NR	Required if Process Module Affected	NR	Use Generic Platform Data	NR
Thermal Cycling for copper interconnect	1 Lot Mandatory	NR	Required if Process Module Affected	NR	Use Generic Platform Data	NR
Inter/Intra Metal Dielectric Integrity for non-SiO2 Dielectrics	3 Lots Mandatory	NR	Required if Process Module Affected	NR	Use Generic Platform Data	NR
DC Hot Carrier Injection	3 Lots Mandatory	3 Lots Mandatory	Required if Process Module Affected	Required if Process Module Affected	Use Generic Platform Data	Use Generic Platform Data
Gate Oxide Dielectric Integrity	3 Lots Mandatory	3 Lots Mandatory	Required if Process Module Affected	Required if Process Module Affected	Use Generic Platform Data	Use Generic Platform Data
Capacitor Dielectric Integrity	3 Lots Mandatory	NR	Required if Process Module Affected	NR	Use Generic Platform Data	NR
Plasma Process Induced Damage	3 Lots Mandatory	3 Lots Mandatory	Required if Process Module Affected	Required if Process Module Affected	Use Generic Platform Data	Use Generic Platform Data
Bias Temperature Stress	3 Lots Mandatory	3 Lots Mandatory	Required if Process Module Affected	Required if Process Module Affected	Use Generic Platform Data	Use Generic Platform Data
Negative Bias Temperature Instability	3 Lots Mandatory	3 Lots Mandatory	Required if Process Module Affected	Required if Process Module Affected	Use Generic Platform Data	Use Generic Platform Data

4 Pillars

ON Semiconductor Strategy

Our business strategy is to become the supplier of choice by:

- Leveraging our operational strengths
- Building intimate relationships with market-making customers
- Improving our technological capabilities to provide leadership in power and signal management solutions

To follow this strategy we need to continuously:

- Dedicate resources to understand the needs of our key customers and develop solutions for their key applications
- Increase our rate of technological innovation
- Shorten our development cycle times
- Lower manufacturing costs
- **Improve Quality** and supply chain

People Powering the Future

July 15, 2008

ON Semiconductor Corporate Social Responsibility Statement of Commitment

As a global supplier to customers worldwide, ON Semiconductor operates across a diverse range of cultures and international marke We are committed to providing our customers with inventive, high quality products that are environmentally sound, conducting our operations in an environmentally, socially and ethically responsible manner and complying with all applicable laws and regulations o those countries worldwide where we do business. This commitment is deeply ingrained in our Core Values, certain policies and our Code of Business Conduct ("Code"). As further evidence of our commitment to corporate social responsibility, we have embraced specific standards that are modeled after the Electronic Industry Code of Conduct ("EICC"). Many if not all of these standards are reflected already in one way or another in our Code and other policies which, like the EICC standards, address, among other things, conduct across several areas of social responsibility including labor practices, health and safety, environmental, ethics and which promote management systems designed to ensure conformance with these standards. ON Semiconductor is committed to incorporating these standards into our facilities' auditing program and to work toward continuous improvement in these areas.

Sincerely,

ON Semiconductor Executive Management Team

Keith Jackson, President and Chief Executive Officer Officer

John Nelson, Executive Vice President and Chief Operating Officer Chief

Donald Colvin
Executive Vice President and Chief Financial Officer

Sonny Cave
SVP, General Counsel and Compliance & Ethics Officer

Bob Mahoney, Executive Vice President, Sales and Marketing Officer

Colleen McKeown
Senior Vice President of Human Resources and Communications

Andy Williams
SVP & General Manager, Automotive & Power Regulation

Bill Schromm,
SVP & General Manager, Computing Products

Bill Hall,
SVP & General Manager, Standard Products

Bob Klosterboer
Senior Vice President - Custom and Foundry

Manor Narayanan
VP & GM, Digital & Consumer Products Group

Charlotte Diener
SVP, Chief Integration Officer

Keenan Evans, VP
Global Quality & Reliability

Dave Wagner
SVP & Chief Information Officer

Walt Guy
SVP, Global Supply Chain

Peter Zdebel, SVP
Chief Technology Officer

ON Semiconductor®

- **Superior Quality**
- **Superior Reliability**
- **Superior Responsiveness**
- **Superior Ethics & Social Responsibility**
- ***Superior Value***

QUALITY POLICY:

"We will exceed Customer Expectations with our Superior Products and Services."

QUALITY STATEMENT:

"Every ON employee is personally responsible for ensuring the highest Quality in the products and services delivered to internal and external customers. Continuous improvement in the quality of our processes, products and service is fundamental to the achievement of customer satisfaction."

Keith Jackson, President and CEO, ON Semiconductor

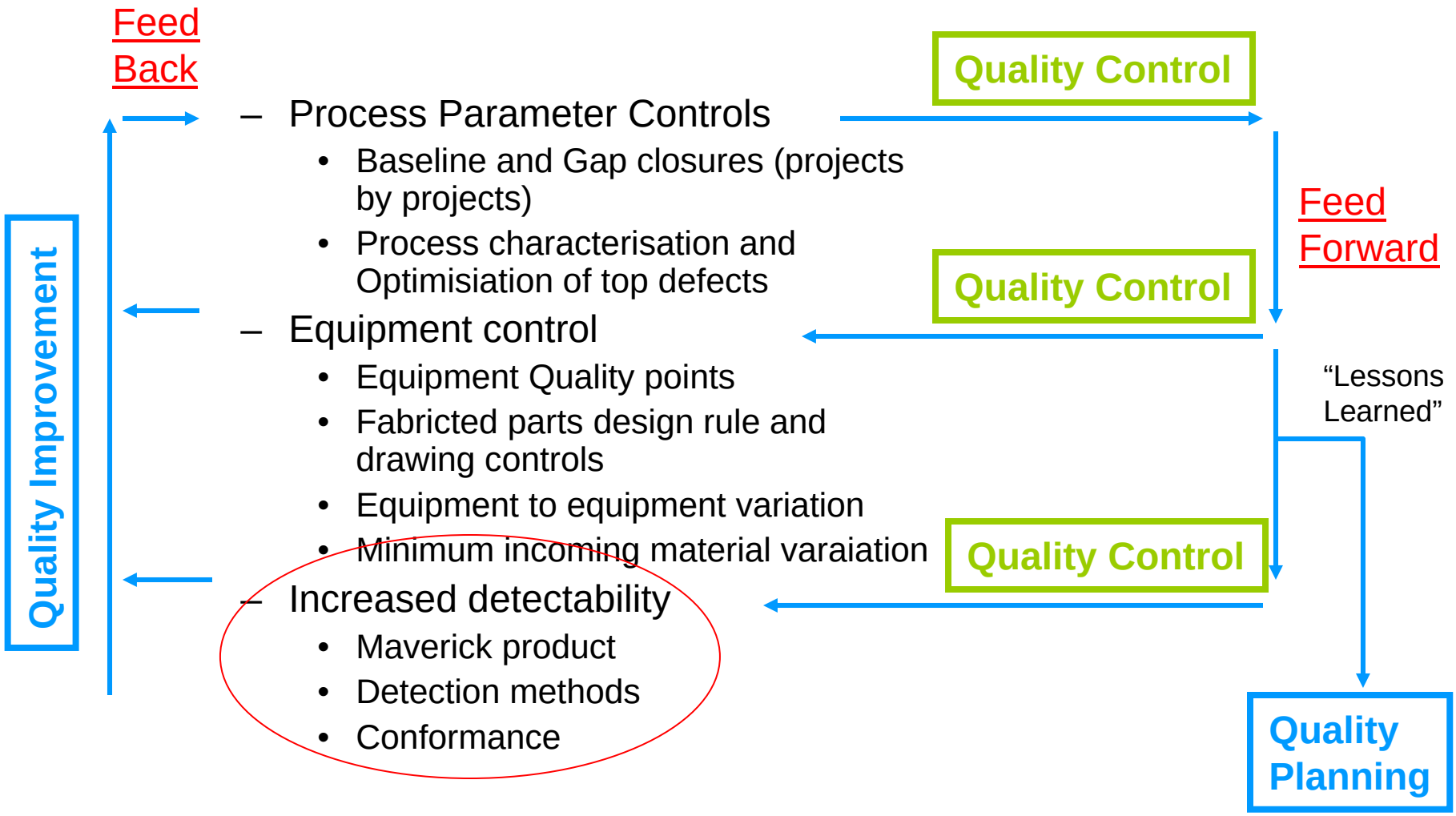
4 Pillars

Manufacturing Quality

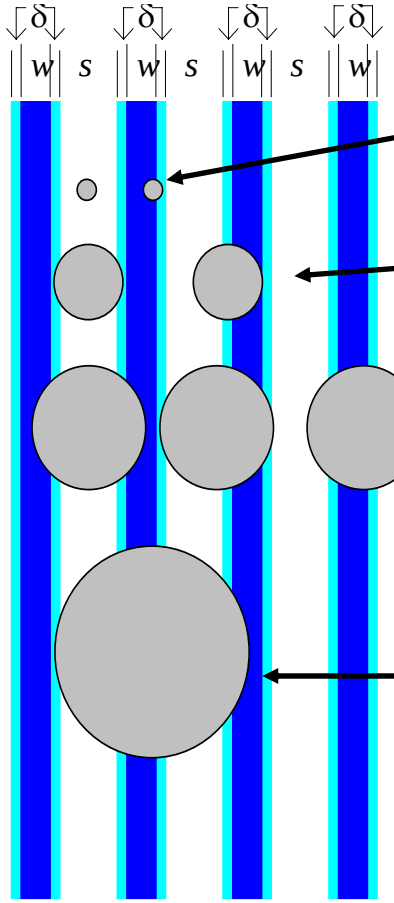
Manufacturing Organization Objectives

- Implement systems & methodologies to continuously produce product of highest quality that will meet customer requirements – Ultimate goal: ZERO Defect & Zero Spill
- Develop & maintain systems and processes to ensure responsiveness to customer needs and quality issue resolution.
- Support manufacturing in achieving lower manufacturing cost with no impact to product performance or transparent to customers in their application.

Manufacturing Quality (Effective prevention)



Early Failure Detection : Latent reliability defects vs. Yield Defects



Not a yield or reliability issue.

Sometimes a latent reliability defect.

Sometimes a yield defect ;
Very often a latent reliability defect.

Always a yield defect.

Reliability defects are proportional to yield defects (typically 1 % - 2 %).

IPRS 2002

Defect Oriented Electrical Screening methods for early reliability improvement

- Standard implemented test methods :
  - Dynamic Voltage Stress (digital & analog)
  - Current based testing :
    - IDDQ testing
    - Delta (IDD) testing
  - Statistical Post Processing :
    - Part Average testing (PAT)
    - Statistical Bin/Yield Analysis (SBA)

- Investigation / introduction of novel test methods :
  - Bridging fault ATPG
  - Transitional fault ATPG
  - Block-to-block interconnect testing
  - Ultra low VDD

Defect Oriented Electrical Screening :

Dynamic Voltage Stress (1)

- Dynamic V-Stress (DVS) :
  - IC production test technique on ATE for screening-out devices with latent process defects in MOS gate oxides, capacitors and interlayer oxides, which might otherwise end-up as (early) field failures.
  - Method : based upon AEC-Q001 (par. 2.1) ;
    - forcing of significantly higher supply (& input) voltages than maximum operational values in order to activate the latent defects :
      - 1.5x nominal voltage for Low Voltage supplies/inputs
      - absolute maximum ratings voltage for High Voltage supplies/inputs
  - DVS improves failure rates with at least a factor 10.
  - Properly implemented DVS does not result in early product wear-out.

Defect Oriented Electric Screening :
Dynamic Voltage Stress (2)

	Product code	Sample size	1000h HTOL drop-out	FIT rate @ Tj= 55°C (CL= 60% ; Ea= 0.7eV)
No DVS applied	P1	-	-	-
	P2	338	3	-
	P3	315	5	-
	Total (no DVS)	**653**	**8**	**2.3 FIT/mm²**
DVS applied	P3	890	0	-
	P4	120	0	-
	P5	75	0	-
	P6	210	0	-
	P7	535	0	-
	Total (DVS)	**1830**	**0**	**0.10 FIT/mm²**

Defect Oriented Electric Screening :

Statistical Post-Processing – PAT (1)

- Part Average Testing :
  - Statistical Post-Processing technique at wafersort for screening-out devices with parametric test results not belonging to the main part of the distribution.
  - Method : Based upon AEC Q001 guidelines ;

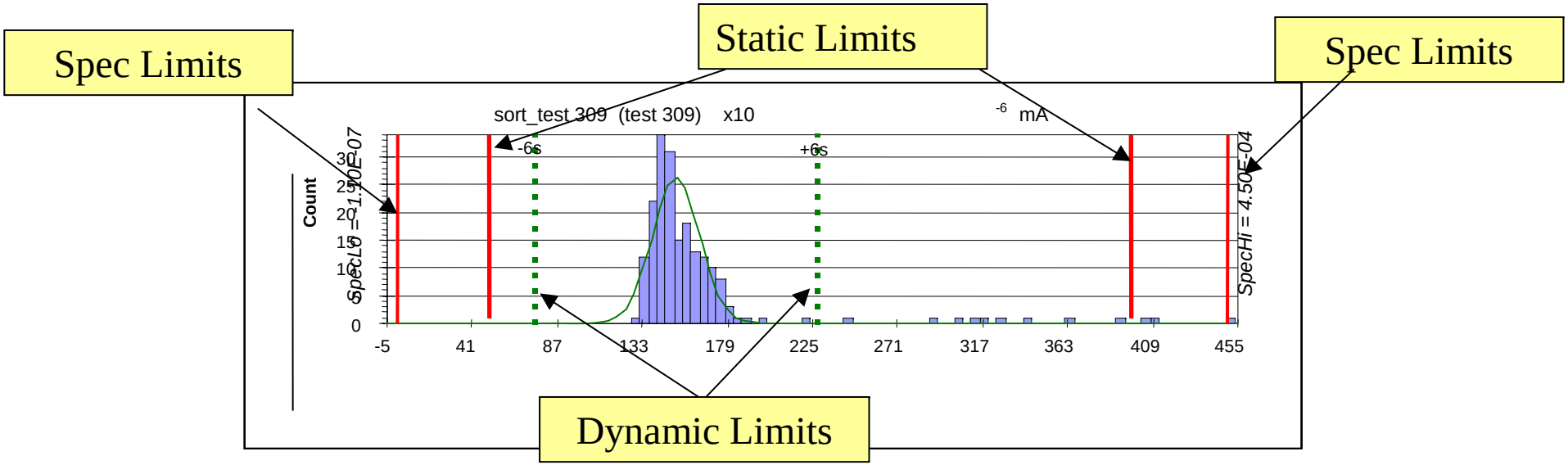
    For every wafer separately, 6 sigma limits are calculated.
    - These dynamic limits are applied after testing, during “pass4”.
    - Selection of parameters : minimum 5 per product which

      (1) exhibit a genuine Gaussian distribution

      (2) cover the critical parameters of the chip
  - Implementation : custom made tool

Defect Oriented Electric Screening：
Statistical Post-Processing – PAT (2)

- PAT example :
  - Device specification limits normally do not changed during the manufacturing life of a device.
  - Dynamic limits are generated automatically for **each wafer and each parameter**



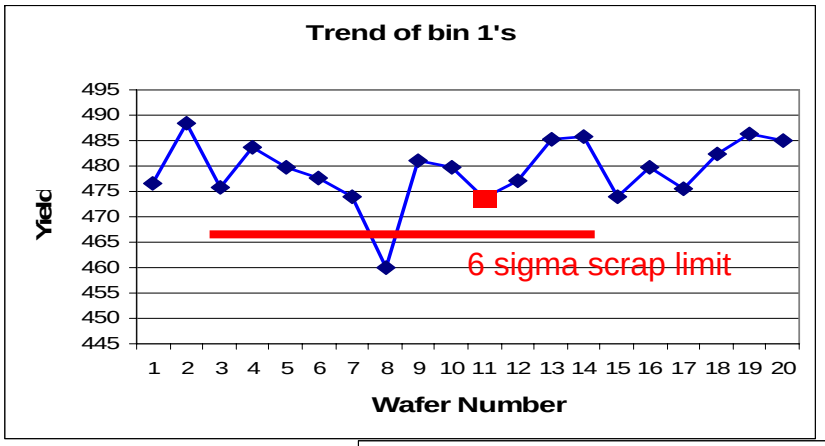
Defect Oriented Electric Screening :
Statistical Post-Processing – SBA (1)

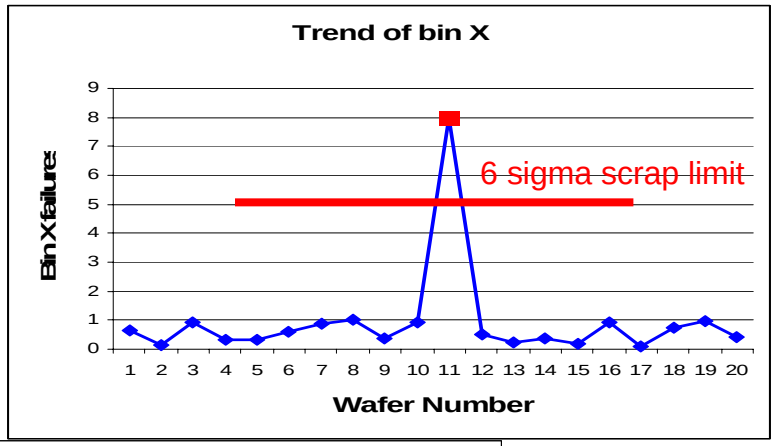
- Statistical Bin Analysis :
  - Statistical Post-Processing technique for identifying wafers or (sub)lots with lower yield or exceptional drop-out for certain binnings.
  - Method : Based upon AEC Q002 guidelines ;

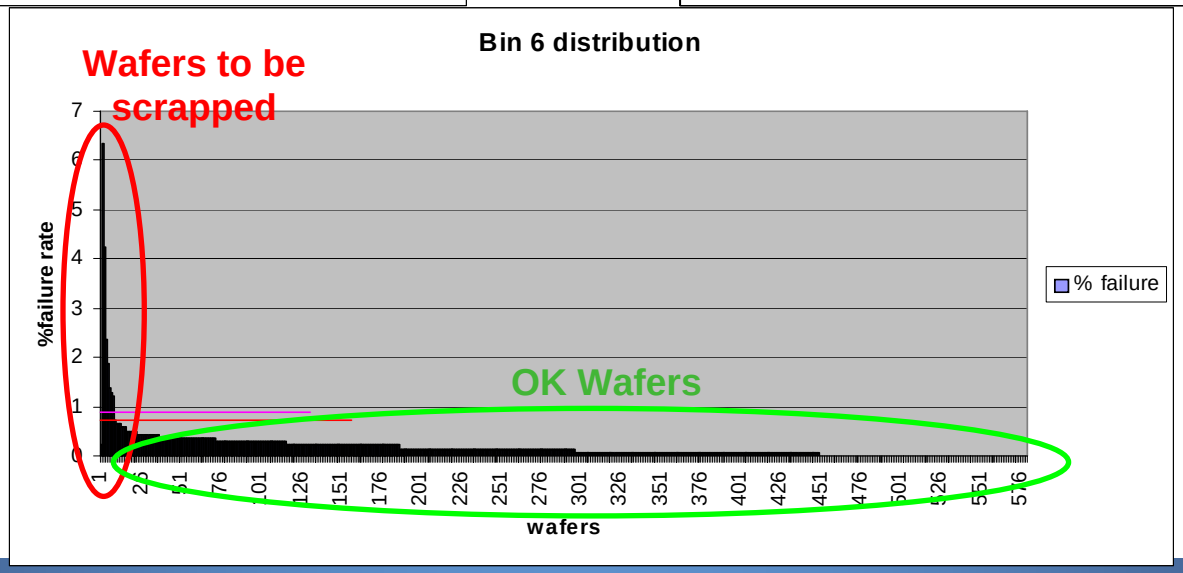
    Hold limits (at 4 sigma) and scrap limit (at 6 sigma) are calculated based on the first 100 wafers tested.
    - Statistical Yield Limits (bin 1) are applied on all test insertions.
    - Statistical Bin Limits are applied at wafersort.
  - Implementation : custom made tool

Defect Oriented Electric Screening : Statistical Post-Processing – SBA (2)

- Statistical Bin Analysis : example

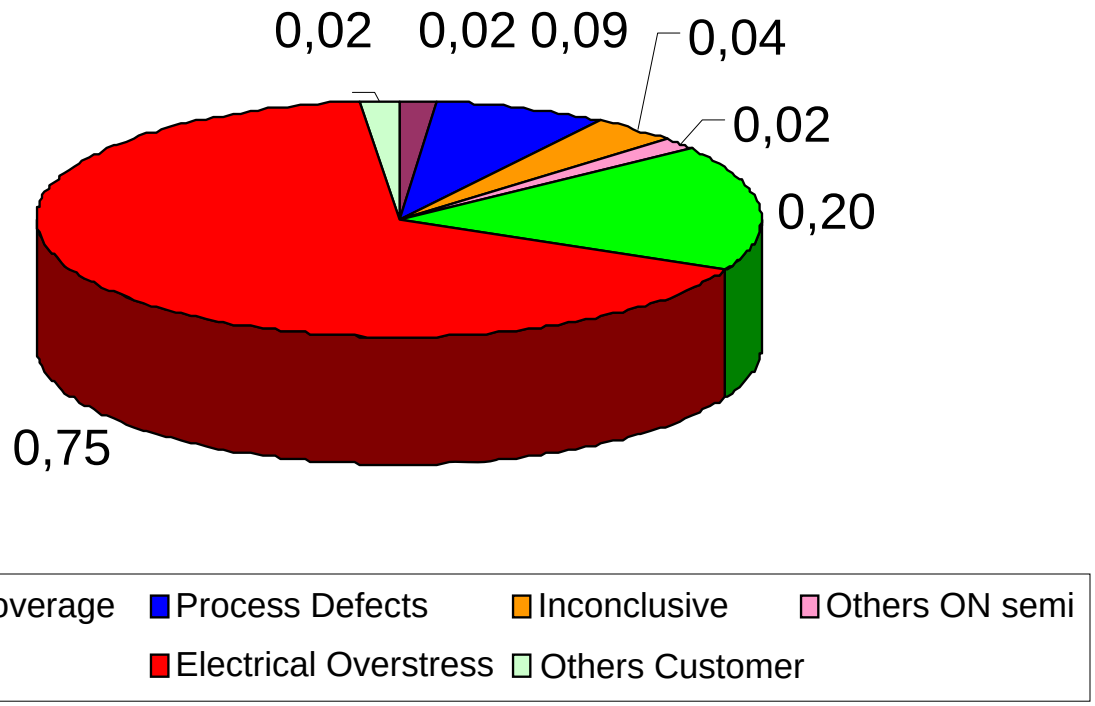






Defect Oriented Electric Screening :
Effectiveness

PPM Pareto (Field) - 2005-2007 - in ppm



Reported Field Failure Rate due to process defects is less than 100 ppb

Defect Oriented Electrical Screening :
Advantages

- High coverage of latent defects, due to implementation in ATE test program / flow. (coverage of dynamic burn-in is usually lower due to limitations in equipment capabilities)
- No additional material manipulations required :
  - Reduces risk for quality issues (e.g. coplanarity, solderability)
  - Reduces risk for reliability issues due to latent EOS/ESD damage
  - No significant impact on production lead-time.

Defect Oriented Electrical Screening :

Conclusions

- Implementation of Defect Oriented Electrical Screening techniques brings a significant reduction of Field Failure rate :
  - Dynamic Voltage Stress improves the Field Failure Rate with at least a factor 10. Introduced in former AMIS in 1996.
  - According to literature, Statistical Post-Processing techniques such as PAT improve the Field Failure Rate with at least a factor 2. Introduced in ON Semiconductor in 2005.

- ON Semiconductor considers Defect Oriented Electrical Screening as the preferred Field Failure screening method compared to production Burn-In.

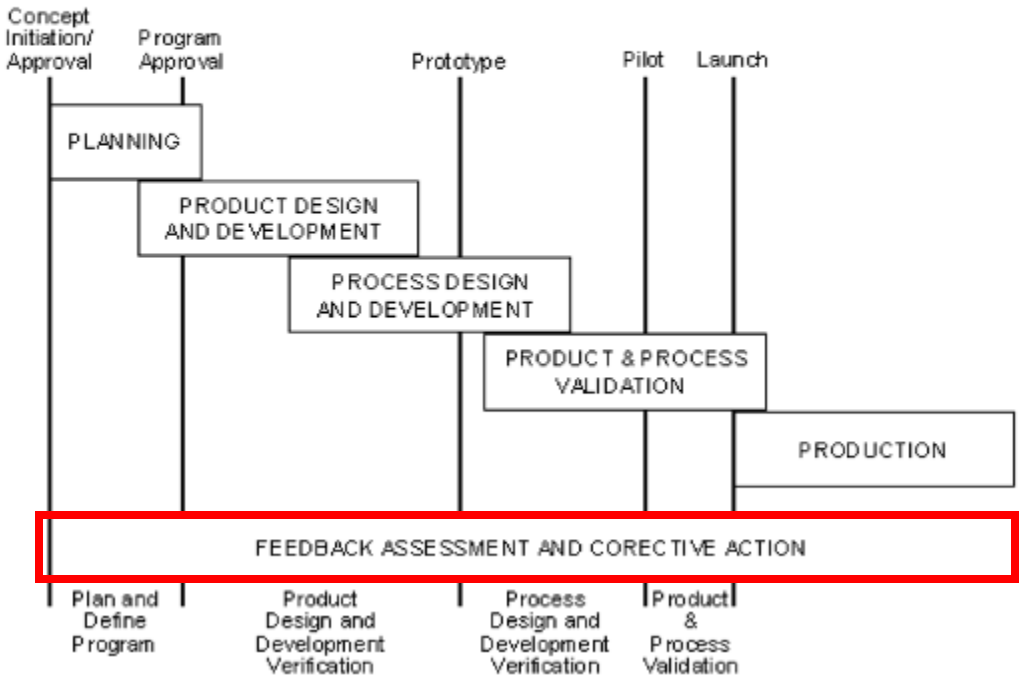
4 Pillars


D·O·M·SVB·INVOC·S·M·MAGDALENAE
Prevent
Promote
Produce
Progress

APQP : Advanced Planning Quality Process

- Improvement in product development : file and update development specifications to avoid issue and improve overall quality going forward

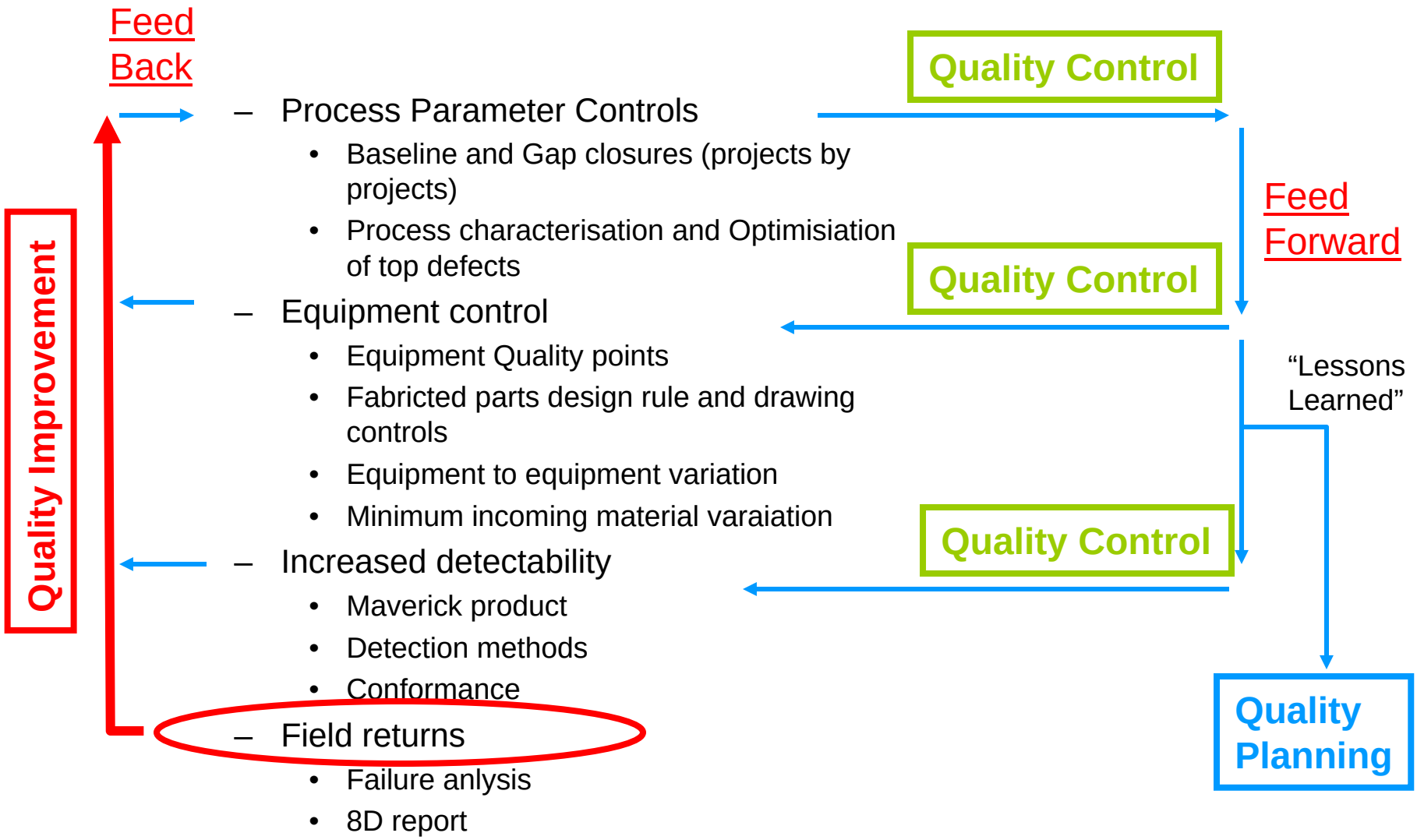
Typical Block flow:



Manufacturing : Quality Improvement Approach

- Review top devices in Pareto for improvement opportunities in each BU which can be extended across the portfolio
  - Team of Quality/Reliability, BU Product engineers, design (as needed), Mfg. engineering
  - Why do top products exhibit much higher return rate than most of portfolio?
    - Device Robustness
    - Manufacturing variability
    - Test coverage
    - Customer application stresses
    - etc.
  - What would it take (technically) to drive return rate to Zero?
    - Is it feasible (first technically then economically)?
    - Does it require joint task force with customer?
  - How do we extend the solution across the rest of the portfolio
    - Existing products
    - New Products

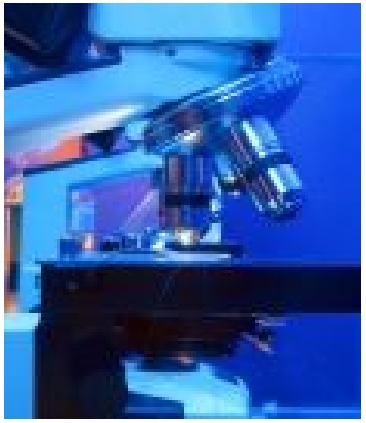
Manufacturing Quality (Effective prevention)

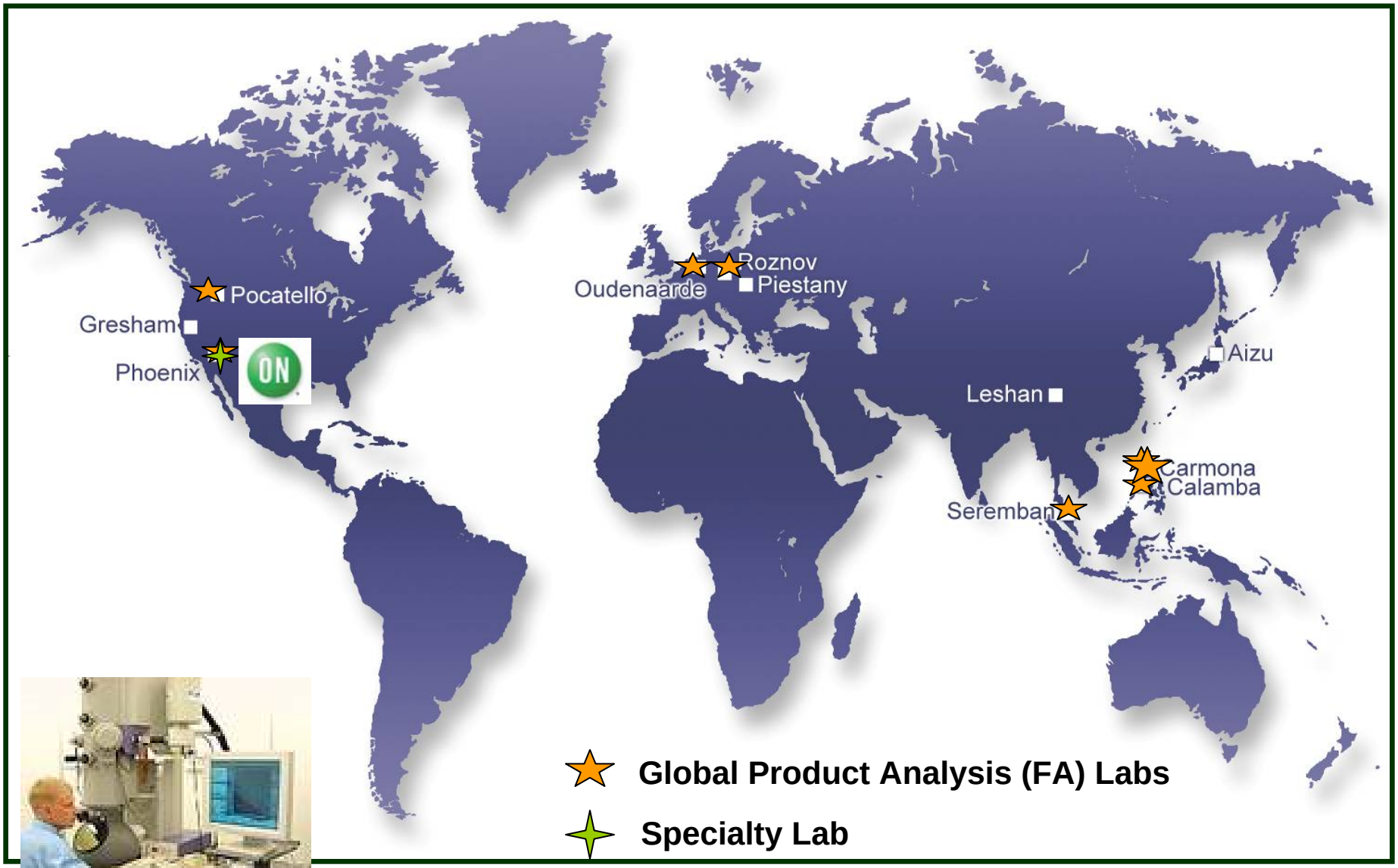


Failure Analysis and Reliability owned labs

High Level Objectives for Global Analytical Labs

- Standardization – Increase Efficiency
  - Toolsets, Data Base, Priority Scheme, Report Format, Procedures
- Site development – Capability and Capacity
  - Support Demand for Customer FA, Consolidation Projects
  - Readiness for New Products
- Responsiveness
  - Decrease Cycle time
  - On Time to CRD




Pocatello
Gresham
Phoenix
Oudenaarde
Roznov
Piestany
Aizu
Leshan
Carmona
Calamba
Seremban
Global Product Analysis (FA) Labs
Specialty Lab

Product Reliability Labs

Intrinsic Reliability Labs

4 Pillars


Quality
D·O·M·SVB·INVOC·S·M·MAGDALENAE
Prevent
Promote
Produce
Progress

Quality, Reliability, EHS

- Customer Quality
  - Responsiveness, Incident Reduction, Change Management
- Global Analytical Labs
  - Responsiveness, Capacity, Capability, Standardization
- Reliability
  - Capacity, Capability, Risk Reduction
- Quality Systems
  - Integration
- Manufacturing Quality
  - Control, Improve, Best Practice - LSS

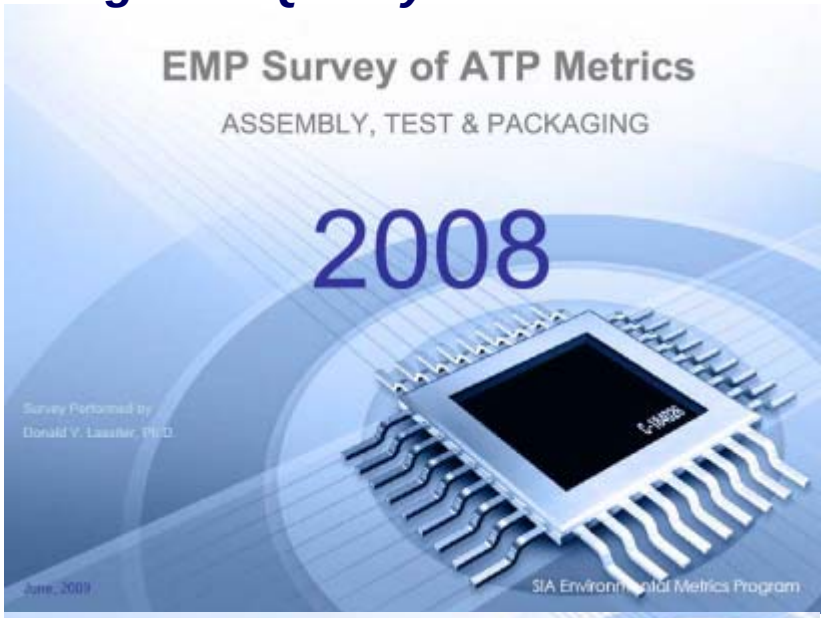
- Supplier Quality
  - Reduce Supplier Base, Drive Quality Improvement
- EHS
  - Compliance, Risk Management, Sustainability

Quality Key Takeaways

- Proactive Customer Engagement
  - Reduce Incident Rate and Eliminate Non-value added FA
- Continuous Improvement in Responsiveness
  - Measured as On Time Delivery to Customer Expectation
- World Class Product Quality Levels
  - Attack the top offenders and fan out best practice
- + Resource Conservation (not covered in this presentation)
  - Monitor Cost Savings & Publicize Results

Integrated Quality/EHS Metrics

Quality/EHS



Annual SIA Environmental Metrics Survey
Published June 2009

ON Semiconductor LPS ranks #1 in 4/5 Categories surveyed !

ON Semiconductor LPS Ranking out of 15 facilities surveyed

Water Usage per Package	#1 *(2)**
UPW Usage per package	#1 *(1)*
RCRA Waste per package	#2 *(7)*
Electricity kWH per package	#1 *(1)*
Total Waste per package	#1 *(1)*

** Numbers in parentheses are normalized to compensate for process time*

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting automotive applications at www.onsemi.com/automotive