安森美半导体
ON Semiconductor®

设计高能效ATX解决方案

Designing High-Efficiency ATX Solutions

实用设计考虑要点及255 W ATX电源参考设计测试结果

Practical Design Considerations & Results from a 255 W Reference Design

议程 Agenda

- 规范标准和市场要求 Regulation and Market Requirements
- 255 W ATX参考设计的目标规范 Target Specification for the Reference Design
- 架构考虑 Architectural Considerations
- 设计途径及每个电源段的关键考虑点 Design Approach & Key considerations for each stage
  - 功率因数校正(PFC)段 PFC Stage
  - 主开关电源(SMPS)段 Main SMPS Stage
  - 次级段 Secondary Stage
- 测试结果 Results
- 总结 Summary

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推动能效提升的因素
Drivers for Efficiency Improvements

- 降低能源消耗已经成为全球众多国家的政府和消费者的一项主要目标 Reducing Energy consumption has become a major goal for governments and consumers across the globe
- 业界需要适应这些对更高能效与日俱增的需求 Businesses need to adapt to these ever increasing demands for higher efficiency
- “绿色环保”团体持续不断地扩大节能环保界线 “Green” groups are continuing to constantly push the boundaries
- 终端产品更高集成度和更小形状系数也推动更高能效的需求 Higher integration into end-products and smaller form factors are also pushing the need for higher efficiency
- 提升能效的早期支持者如今正获得广泛关注，并收获更多的回报 Early enablers of increased efficiency are gaining lot of attention and garnering increased rewards
- 计算产业气候拯救行动(CSCI)是一个有影响力的团体，这团体正大力推动计算机产业的高能效要求 The Climate Savers Computing Initiative (CSCI) is an influential group that is pushing high efficiency requirements in computing
  - 在全球主要类似团体或规范机构中，这团体的能效目标最为激进 This group has the most aggressive efficiency targets of any major group or regulation agency world-wide
  - 他们的规范被其他团体迅速采纳，其中就包括美国的80 PLUS Their specifications were quickly adopted by other groups, including 80 PLUS in the US

计算产业气候拯救行动(CSCU)能效要求

CSCI Efficiency Requirements

	Year 1	Year 2	Year 3	Year 4
Time Table	July '07-June '08	July '08 - June '09	July '09 - June '10	July '10 - June '11
Minimum Efficiency Targets (@ 20%, 50%, 100% of rated o/p)	Energy Star 4.0 80%, 80%, 80% PF=0.9	82%, 85%, 82%	85%, 88%, 85%	87%, 90%, 87%
Equivalent to	80 PLUS	80 PLUS BRONZE	80 PLUS SILVER	80 PLUS GOLD
Purchase Commitment				
Most recent EnergyStar Compliant PC	100%	100%	100%	100%
85% PSU		>=20%	>=80%	100%
88% PSU			>=20%	>=80%
90% PSU				>=20%

- 由于英特尔、微软、Google、惠普、戴尔和联想等业界领先企业积极参与，这团体极具影响力 With active involvement from Intel, Microsoft, Google, HP, Dell & Lenovo this is a very influential group
- 此外，CSCI成员被要求作出每年最少采购多少符合上述能效要求的计算机产品的承诺 In addition, CSCI members are asked to have minimum purchase commitments listed above every year

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参考设计
Reference Design

- 介绍符合计算产业气候拯救行动(CSCI)第三年(2009年7月至2010年6月)目标(与80 PLUS的Silver目标类似)的参考设计ATX reference design that meets Climate Savers Year 3 targets (similar to 80 PLUS Silver targets) is presented
- 这255 W参考设计针对现实世界的规范而构造 The 255 W design was built to real-world specs
  - 整合了3家主要OEM的规范 Specifications from 3 major OEMs were incorporated
  - 标准ATX尺寸和输出 Standard ATX dimensions and outputs
  - 标准保护特性 Standard protection features
  - 成品采用严格方式进行完整测试 The finished unit was fully tested in a rigorous manner
- 系统总成本在每个设计阶段都是一项关键考虑点 Overall cost of the system was a key consideration during every design step
- 这参考设计采用双电感加单电容半桥(LLC-HB)谐振拓扑结构 LLC-HB Resonant Topology adopted for this design

参考设计-目标规范

Reference Design – Target Specifications

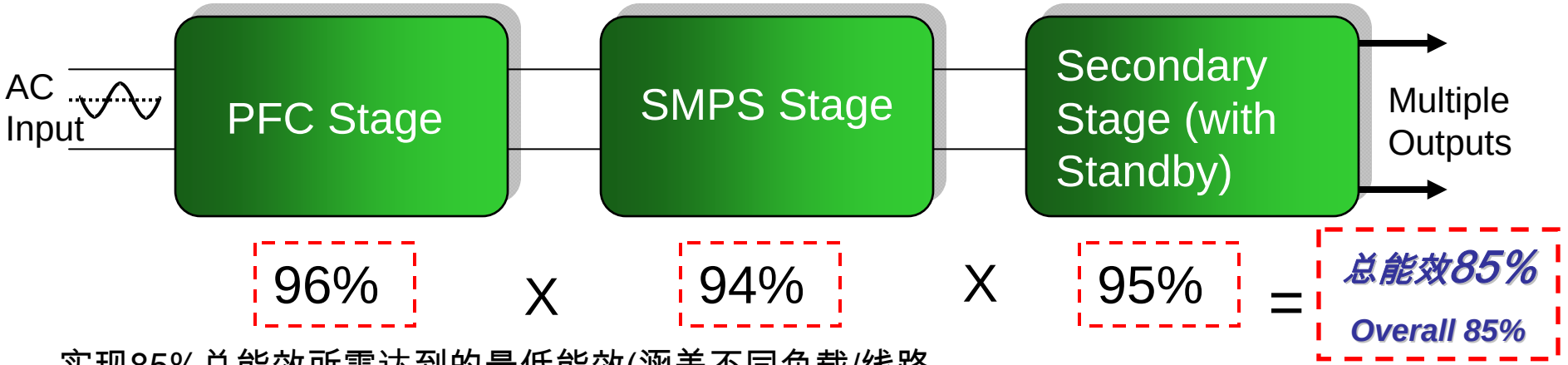
- 输入范围：90 Vac至264 Vac(100 Vac、115 Vac、230 Vac和240 Vac为标牌电压) Input range: 90 Vac to 264 Vac (100 Vac, 115 Vac, 230 Vac, and 240 Vac as the label voltage)
- 输出功率：255 W Output power: 255 W
- 输出电压： 12 V_A、12 V_B、-12 V、3.3 V、5 V和5 V_{sb} Output voltage: 12 V_A, 12 V_B, -12 V, 3.3 V, 5 V, and 5 V_{sb}
- 能效要求 Efficiency requirement:
  - 20%负载和满载时高于85% Above 85% at 20 % and full load
  - 50%负载时高于88% Above 88% at 50 % load
- 功率因数(PF)：230 Vac、50%负载时高于0.9 Power factor: > 0.9 at 230 Vac, 50 % load
- 待机能耗要求(FEMP)：低于1 W Standby power requirement (FEMP): < 1W

参考设计-输出负载
Reference Design – Output Loading

输出 Output	最大电流 (A) Max Current	满载电流(A) Full Load	50%负载电流 (A) 50% Load	20%负载电流 (A) 20% Load
12 V_A	13.0	9.5	4.75	1.90
12 V_B	7.0	5.12	2.56	1.02
-12 V	0.4	0.32	0.16	0.06
3.3 V	8.0	5.03	2.52	1.01
5 V	15.0	9.44	4.72	1.89
5 V_{sb}	3.0	2.39	1.20	0.48
总功率(W) Total Power	361.2	255	128	51
能效要求 Efficiency Requirement		> 85 %	> 88 %	> 85 %

各电源段能效目标 Efficiency Targets by Stage

- 为了满足85%的总能效目标，每个电源段都必须满足最低的能效要求 To meet the overall efficiency target of 85%, each stage has to meet a minimum efficiency



实现85%总能效所需达到的最低能效(涵盖不同负载/线路

Min. efficiency needed to achieve **85% overall efficiency** (across load/line)

- 为满足各段最低能效目标要求，电源架构、关键元件和总体设计都必须仔细考虑 In order to meet the minimum efficiency targets, the architecture, key components, and overall design has to be carefully considered
- 安森美半导体的参考设计已实现这些目标要求，同时仍然保持较低的总成本！ ON Semiconductor's reference design has achieved theis objective while still keeping the overall cost down!!

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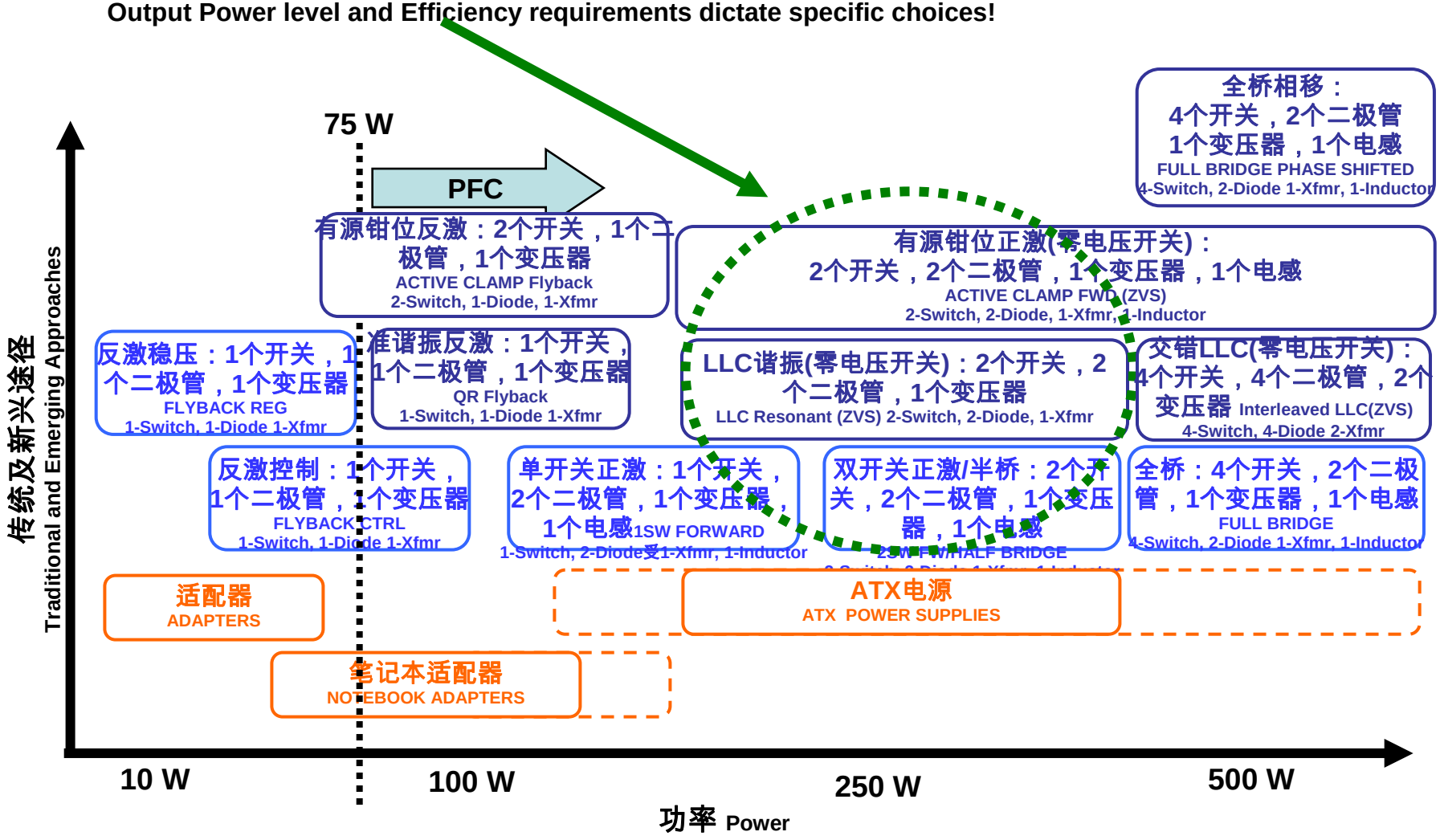
拓扑结构比较
Topology Comparison

	双开关正激 Dual switch Forward	LLC半桥谐振 LLC HB Resonant	有源钳位正激 Active Clamp Forward
变压器 Transformer	易于设计 Easy to design 对泄漏敏感 Leakage sensitive 第1象限操作 1Q operation 较低爬电距离Lower creepage	最难设计 Hardest to design 受控泄漏 Controlled $L_{leakage}$ 第2象限操作 2Q operation 较低爬电距离Lower creepage	最难设计 Hardest to design 对泄漏不敏感 No leakage sensitive 第2象限操作 2Q operation 较高爬电距离Higher creepage
MOSFET MOSFET	500 V (600 V) 2颗大电流器件 2pcs high current	500 V (600 V) 2颗大电流器件 2pcs high current	800 V 1颗大电流，1颗低电流 1pcs high current, 1pcs low current
输出扼流圈 Output Choke	传统设计 Conventional design	不需要 No needed	传统设计(小15%) Conventional design (smaller by 15%)
输出电容 Output Capacitor	传统设计 Conventional design	需较高纹波能力(损耗更高) Needs higher ripple capability (more losses)	传统设计 Conventional design
交叉稳压 Cross regulation	采用耦合扼流圈较好 Good with coupled choke	不太好 Not Very Good	采用耦合扼流圈较好 Good with coupled choke
开关方式 Switching	硬开关 Hard Switching	软开关 Soft Switching	软开关 Soft Switching
能效 Efficiency	中等 Mid	高 High	高 High

主转换器拓扑结构选择 Topology Options for Main Converter

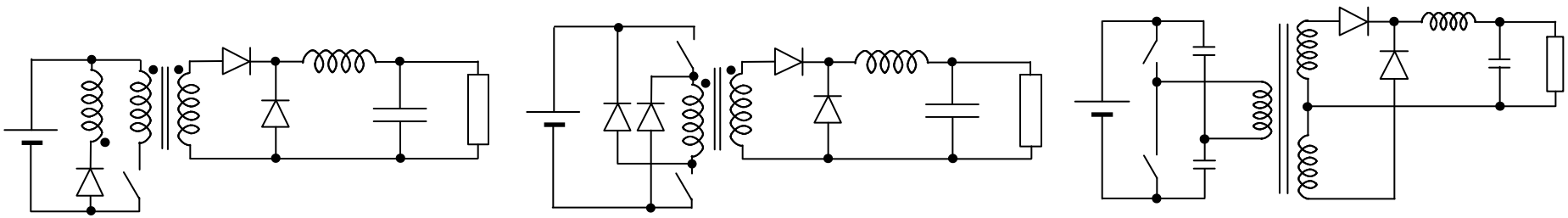
- **输出功率电平和能效要求决定着具体选择！**
  Output Power level and Efficiency requirements dictate specific choices!



拓扑结构总结
Topology Summary

双开关正激或其它硬开关拓扑结构 2-SW Forward or other Hard Switching topology:

- 不方便采用软开关 Does not facilitate soft switching
- 不方便采用同步整流 Does not facilitate sync rectification
- 能效较低 Lower Efficiency
- 双开关正激的MOSFET性能指数(Vds*Irms)低30% 2-sw forward has 30% worse MOSFET figure of merit (Vds*Irms)
- 磁性元件成本较高(变压器+输出扼流圈) Higher cost in Magnetic components (Transformer + Output choke)
- 需要2个大电流/电压二极管 2 high current/voltage diodes required
- 两个功率MOSFET都需要散热片 Heatsink required for both power MOSFETs



LLC串联谐振转换器优势

Benefits of LLC Series Resonant Converter

- 与其它谐振拓扑结构相比，串联谐振类的转换器允许工作在相对较宽的输入电压和输出负载范围 Type of serial resonant converter that allows operation in relatively wide input voltage and output load range when compared to other resonant topologies
- 元器件数量有限：谐振储能(tank)元件能够被集成至单个变压器中——只需要一个磁性元件 Limited number of components: resonant tank elements can be integrated to a single transformer – only one magnetic component needed
- 初级开关管在所有额定负载条件下都零电压开关(ZVS) Zero Voltage Switching (ZVS) condition for the primary switches under all normal load conditions
- 零电流开关(ZCS)用于次级二极管 Zero Current Switching (ZCS) for secondary diodes
- 软开关和电磁干扰(EMI)较低是另外优势 Soft-switching and lower EMI are additional benefits

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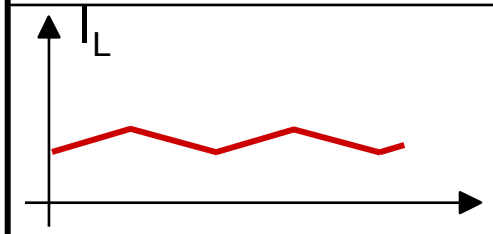
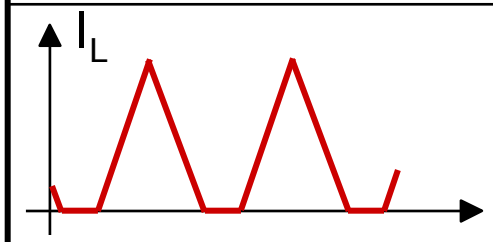
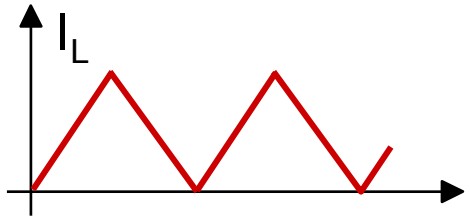
PFC段能效提升

PFC Efficiency Improvements

- 首先选择工作模式(CCM或DCM/CrM) First, select the mode of operation (CCM or DCM/CrM)
- 在CrM和CCM应用方面，安森美半导体都提供能效高于94%的解决方案
  ON Semiconductor has >94% efficient solutions for both CrM and CCM applications

	工作模式 Operating Mode	主要特点 Main Feature
	连续导电模式 (CCM) Continuous Conduction Mode	总是硬开关 Always hard-switching 电感值最大 Inductor value is largest 均方根电流最小 Minimized rms current
	非连续导电模式 (DCM) Discontinuous Conduction Mode	均方概电流最大 Highest rms current 线圈电感降低 Reduced coil inductance 稳定性最佳 Best Stability
	临界导电模式 (CrM) Critical conduction Mode	性价比佳 Good performance to cost 均方根电流较大 Large rms current 开关频率不固定-EMI更难处理 Switching frequency not fixed – EMI becomes harder

不同工作模式考虑
Considerations for Different Operation Mode

- 对CCM而言，能够这样实现高能效： For CCM, high efficiency can be achieved by:
  - 优化开关选择(轻载时开关损耗占损耗的主导，因此，牺牲导通阻抗来提升开关频率较为明智) Optimal switch selection (at light load, switching losses dominate, so it is more advisable to sacrifice Rds-on for faster switching)
  - 使用软恢复升压二极管 Soft recovery boost diode
  - 选择合适大小的电感，减少铜损耗 (磁芯损耗较低) Inductor sized for copper loss reduction (Core losses are low)
- 对DCM/CrM而言，能够这样实现高能效： For DCM/CrM, high efficiency can be achieved by:
  - 优化电感磁芯，降低磁芯损耗和高频绕组损耗 Optimizing the inductor core for low core loss and low high-frequency winding losses
  - 选择导通阻抗较低的开关 Selecting a lower Rds-on switch
  - 只需较少注意升压二极管的选择 Less attention to be paid to boost diode selection

PFC – 输出功率定位

PFC – Output Power Positioning

器件型号 Part number	75-150 W	150-250 W	250-500 W	>500 W
NCP1601				
NCP1606				
NCP1653				
NCP1654/55				
NCP1650				
推荐 Recommended	有更适合器件 Better fit exists			

固定频率非连续导电及临界导电模式 Fixed Freq. DCM & CrM
临界导电模式 Critical Conduction Mode
连续导电模式 Continuous conduction Mode

- 就250 W应用而言，工作模式中有一种灰色区域可以选择 There is a grey area in the mode of operation to be chosen for a 250 W application
- 这参考设计选择了CCM PFC，使用的是安森美半导体的NCP1654 For this reference design, a CCM mode PFC was chosen using ON Semiconductor's NCP1654

PFC – 连续导电模式MOSFET选择

PFC – CCM MOSFETs Choice

	20N60C3 导通阻抗 Rds(on) = 0.19 W 输出电容 Coss = 780 pF		15N60C3 导通阻抗 Rds(on) = 0.28 W 输出电容 Coss = 540 pF	
	开关损耗(Coss) Switching losses	导电损耗 Conduction losses	开关损耗(Coss) Switching losses	导电损耗 Conduction losses
100%负载Load 270 W	1.28 W	1.34 W	0.88 W	1.98 W
	小计 Sub-total: **2.62 W**		小计 Sub-total: **2.86 W**	
50%负载load 135 W	1.28 W	0.34 W	0.88 W	0.5 W
	小计 Sub-total: **1.61 W**		小计 Sub-total: **1.38 W**	
20%负载load 54 W	1.28 W	0.05 W	1.28 W	0.08 W
	小计 Sub-total: **1.33 W**		小计 Sub-total: **0.96 W**	

导电损耗 Conduction losses:

$$P_{on,\max} = R_{DS(on)} \cdot \left(\frac{P_{in,\max}}{V_{acLL}} \right)^2 \cdot \left(1 - \frac{8\sqrt{2}V_{acLL}}{3\pi V_{out}} \right)$$

由Coss导致的开关损耗
Switching losses caused by Coss:

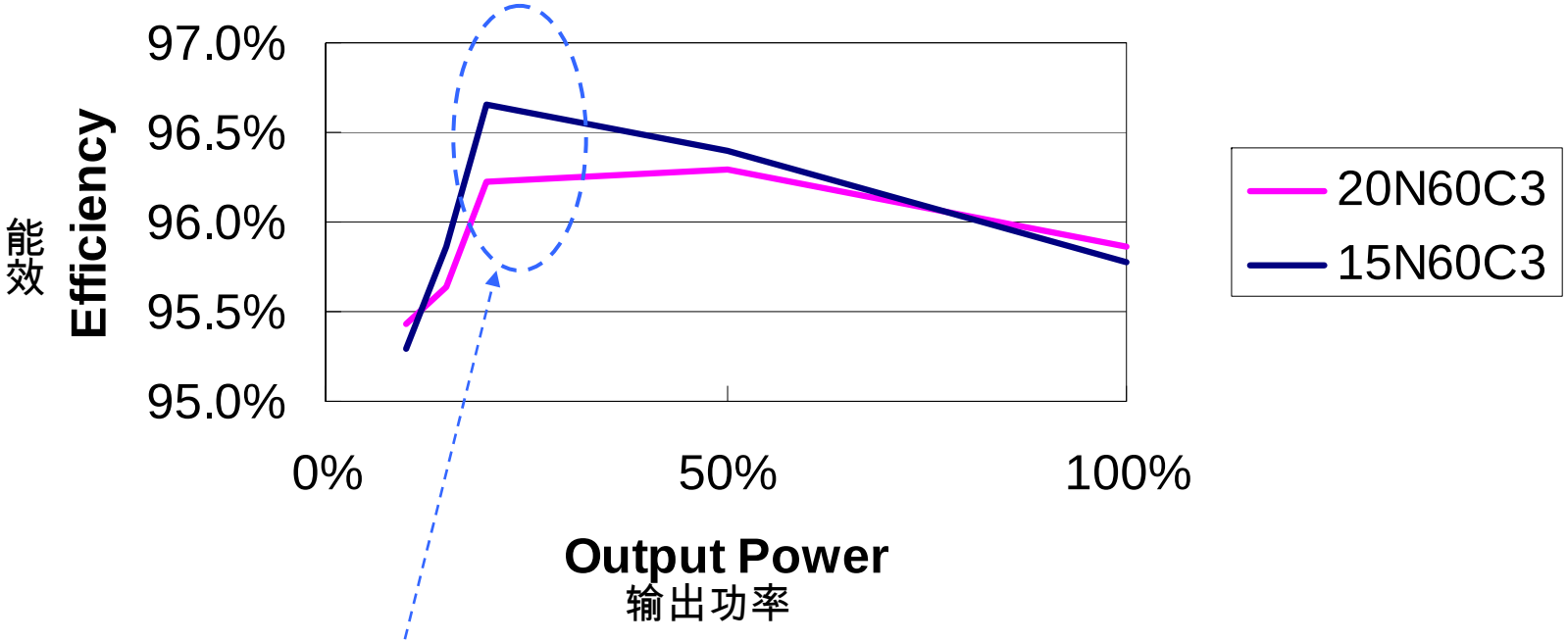
$$\int_0^{V_{end}} CV^2 dv = \frac{2}{3} C_{25} \sqrt{25} \cdot V^{1.5} \cdot f$$

PFC – 连续导电模式MOSFET选择(续)

PFC – CCM MOSFETs Choice (Cont'd)

Efficiency of 270 W CCM PFC based on NCP1654 (Vin = 115 Vac)

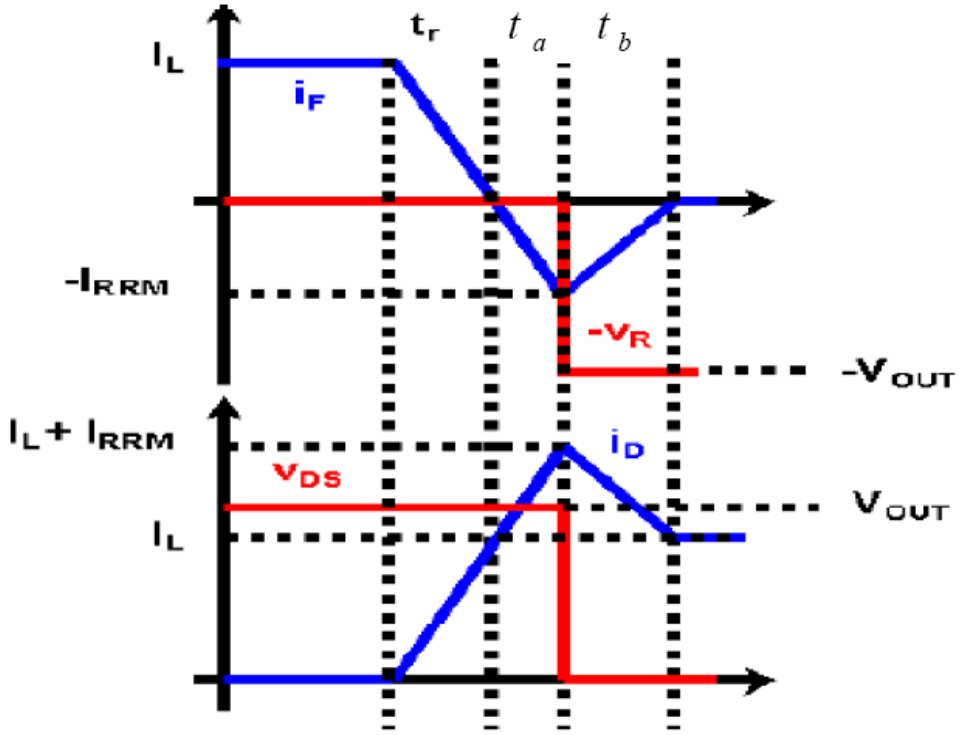
基于NCP1654的270 W CCM PFC的能效(输入电压=交流115 V)



- 轻载时，开关损耗占损耗的主导。某些条件下，额定值较低的MOSFET提供更佳能效。 At light load, switching losses dominate. In some conditions, MOSFETs with lower rating provide better efficiency

PFC – 连续导电模式升压二极管选择

PFC – CCM Boost Diode Choice



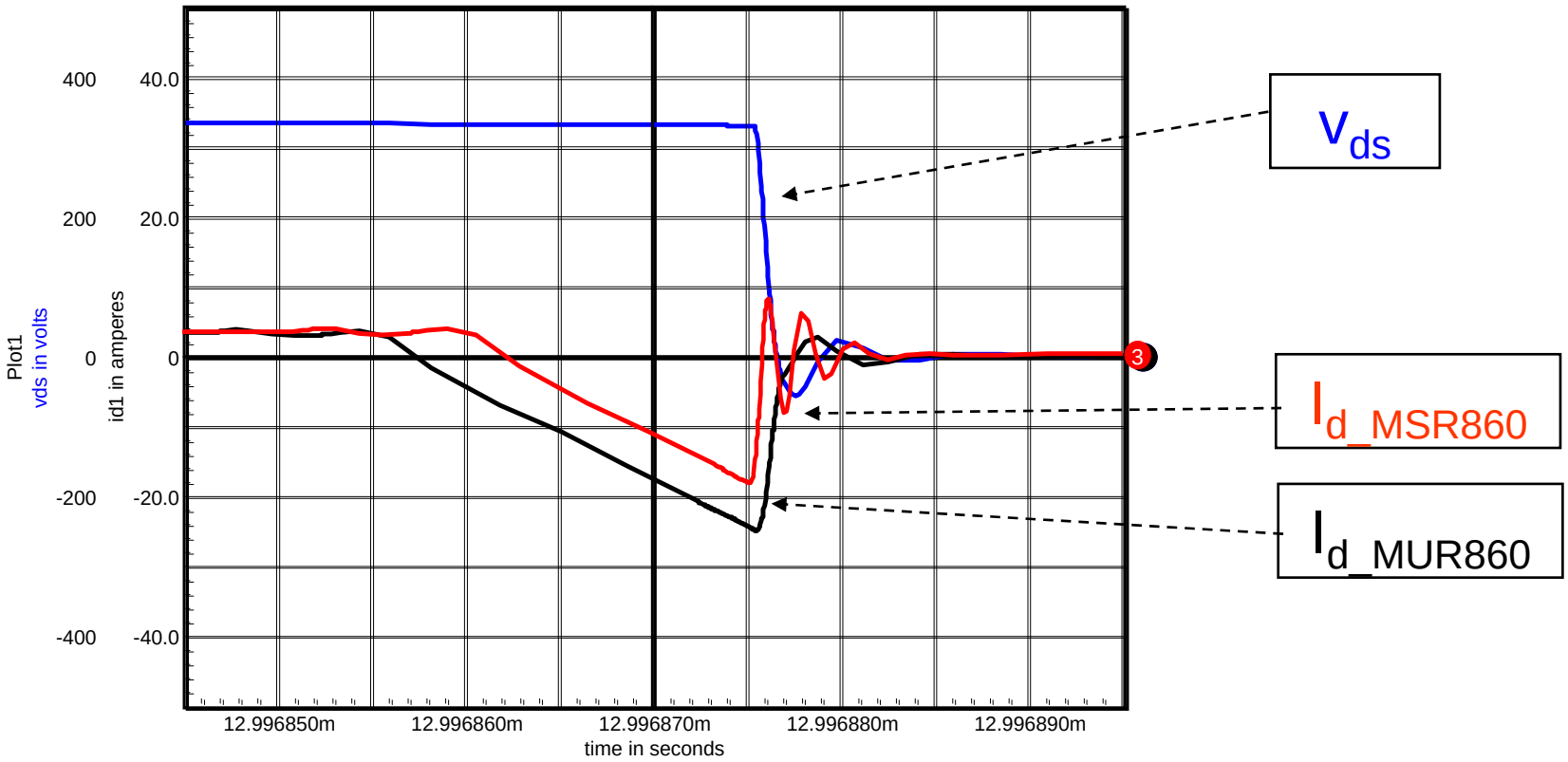
升压二极管
Boost diode

MOSFET
MOSFETs

- 在连续导电模式(CCM)操作中，升压二极管的I_{RRM} (Q_{rr})和(t_r + t_a + t_b)极大地影响MOSFET和升压二极管的开关损耗 In CCM operation, the I_{RRM} (Q_{rr}), and (t_r + t_a + t_b) of boost diode impact the switching losses of MOSFETs and boost diodes significantly

PFC – 连续导电模式升压二极管选择(续)

PFC – CCM Boost Diode Choice (Cont'd)



- 诸如MSR860这样的软恢复二极管(软恢复能力s=tb/ta=3，反向恢复电荷Qrr=700 nC)可以降低开关损耗 A soft recovery diode, e.g. MSR860, with s = tb/ta = 3 and Qrr = 700 nC, reduces the switching losses

PFC – 连续导电模式升压二极管选择(续)

PFC – CCM Boost Diode Choice (Cont'd)

- 为了进一步提升能效，这里列出几种选择：

  To further improve the efficiency, here come several choices:

  – 碳化硅(SiC)肖特基二极管 – 零恢复二极管

  Silicon Carbide Schottky Diode – zero recovery diode

  - 这类二极管提供更高性能，但会增加成本

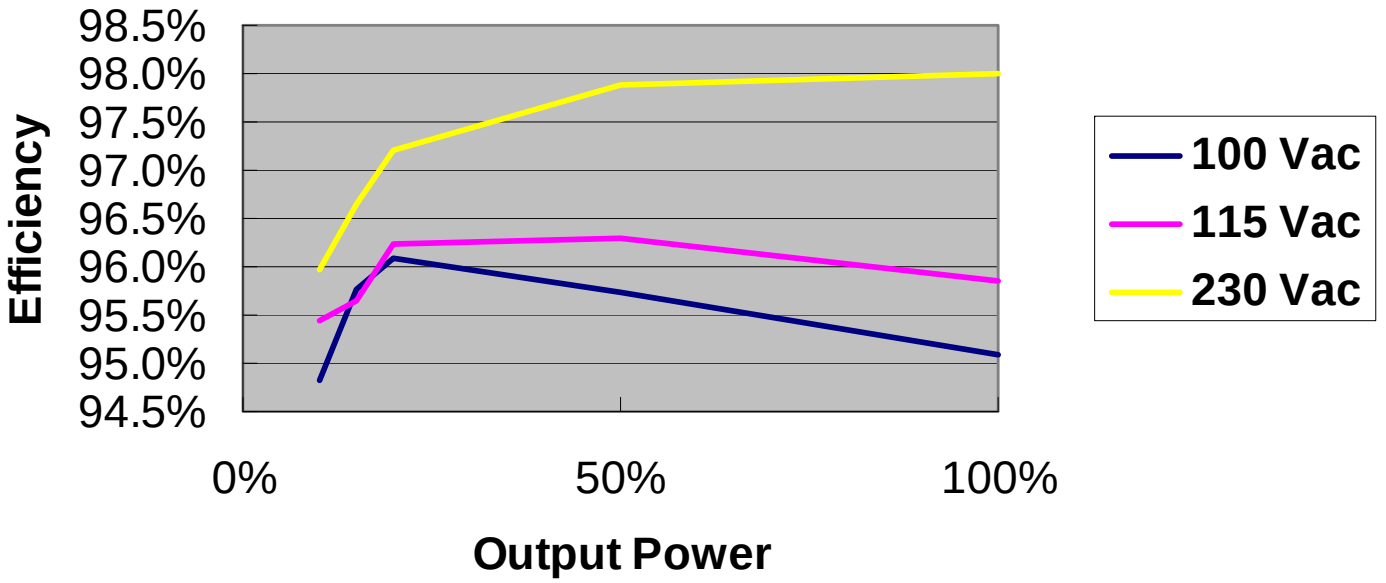
    This provides better performance at added cost

  – Qspeed Q系列PFC整流器 – 软恢复二极管(软恢复能力s=tb/ta=1.3，反向恢复电荷Qrr=35 nC)

  Qspeed Q-series PFC rectifier – soft recovery diode with s = tb / ta =1.3 and Qrr = 35 nC

NCP1654连续导电模式(CCM)PFC 270 W应用

NCP1654 CCM PFC 270 W Application



PFC MOSFET Q1 = 20N60C3

PFC二极管D1 PFC Diode D1=Qspeed LQA08TC600

PFC扼流圈电感 PFC choke = 650 mH

100 Vac时能效高于95%
Efficiency > 95 % at 100 Vac

- 通过选择适合元件，能效得到优化 By selecting suitable components, efficiency is optimized
- 但有些人可能会认为升压二极管较贵，那能够采用其它什么解决方案呢？ But some people might think the boost diode costs more, what other solutions can be used?

PFC段考虑点总结
Summary of PFC Stage Considerations

- 在250 W左右的功率范围，连续导电模式(CCM)和临界导电模式(CrM)/非连续导电模式(DCM)都能提供良好的能效 Both CCM and CrM/DCM PFC can provide good efficiency at power range around 250 W
- 每种拓扑结构的设计考虑点各不相同 The design considerations for each topology are different
- 对于CCM而言，可以这样实现高能效 For CCM, high efficiency can be achieved by:
  - 优化开关选择 Optimal switch selection
  - 使用软恢复升压二极管 Soft recovery boost diode
  - 选择合适大小的电感，减少铜损耗 (磁芯损耗较低) Inductor sized for copper loss reduction (Core losses are low)
- 对于DCM/CrM而言，可以这样实现高能效 For DCM/CrM, high efficiency can be achieved by
  - 优化电感磁芯，降低磁芯损耗和高频绕组损耗 Optimizing the inductor core for low core loss and low high-frequency winding losses
  - 选择导通阻抗较低的开关 Selecting a lower Rds-on switch
  - 只需较少注意升压二极管的选拔 Less attention to be paid to boost diode selection

参考设计中PFC所用关键元件
Key Components used in PFC Stage for Reference Design

- NCP1654，采用SO-8封装的65 kHz CCM PFC控制器
  NCP1654, 65 kHz CCM PFC controller in SO-8
- PFC扼流圈 PFC choke
  - PQ3319 PQ3319
  - 电感值为650 µH Inductance is 650 µH
  - 0.1 * 50规格的绞合线 0.1 * 50 Litz wire
- PFC MOSFET PFC MOSFET
  - SPP15N60C3, 15 A, 650 V, 0.19 Ω $R_{ds(on)}$
- PFC二极管 PFC Diode
  - Qspeed LQA08T600, 8 A, 600 V

议程 Agenda

- 规范标准和市场要求 Regulation and Market Requirements
- 255 W ATX参考设计的目标规范 Target Specification for the Reference Design
- 架构考虑 Architectural Considerations
- 设计途径及每个电源段的关键考虑点 Design Approach & Key considerations for each stage
  - 功率因数校正(PFC)段 PFC Stage
  - 主开关电源(SMPS)段 Main SMPS Stage
  - 次级段 Secondary Stage
- 测试结果 Results
- 总结 Summary

主转换器拓扑结构选择(续)
Topology Options for Main Convertor (Cont'd)

安森美半导体软开关解决方案的优势 Advantage with Soft Switching solutions:

- 软开关带来高性价比、高能效和较低电磁干扰(EMI) Cost effective, highly efficient and lower EMI due to soft switching
- 有源钳位正激(ACF)和双电感加单电容(LLC)拓扑结构正被用于80 PLUS和85 PLUS解决方案 ACF and LLC are being used for 80 PLUS and 85 PLUS solutions
- 在ACF拓扑结构中提供自驱动同步整流 Self-driven Sync Rectification in ACF
- 方便LLC拓扑结构中的同步整流 Facilitates Synchronous Rectification in LLC
- 在ACF拓扑结构中输出电感小15%或者在LLC拓扑结构中无需输出扼流圈 15% lower output inductor in ACF or No output choke required in LLC
- 更好地利用变压器磁芯(第2象限操作) Better Transformer core utilization (2Q operation)
- 允许以更高频率工作，从而尺寸更小 Allows operation at higher frequency, thus smaller size

过去的第一代80 PLUS参考设计中采用有源钳位(ACF)。为显示另一个案例，这85 PLUS高能效参考设计中选择了双电感加单电容(LLC)。 Active clamp was used in 1st 80 PLUS ref design in past. In order to show another example, LLC was chosen in this 85 PLUS efficiency design

提升轻载能效的设计诀窍

Design Tips for Light Load Efficiency

- 通过选择电容较低的场效应管(FET)(在与较低导通阻抗之间进行折衷)，采用软开关操作来降低开关损耗 Reduce switching losses with soft-switching operation by selecting FETs with low capacitance (trade-off with low Rds-on)

	双开关正激 Dual switch Forward	LLC半桥谐振 LLC HB Resonant	有源钳位正激 Active Clamp Forward
FET总输出电容 Total FET Coss	1560 pF	1560 pF	930 pF
导通电压 Turn-on voltage	400 V	0 V	200 V
导通损耗 Turn-on losses(100 kHz)	4.8 W	0 W 	1.1 W
关闭电流 Turn-off current	2.5 A	1.6 A	2.0 A
关闭损耗Turn-off losses (25 ns, 100 kHz)	0.8 W	0.4 W 	0.6 W

提升轻载能效的设计诀窍
Design Tips for Light Load Efficiency

- 轻载时，哪怕是节省0.1 W的能耗都有意义！

  At light load, every 0.1 W counts!

  – 以250 W输出系统为例，20%轻载时减少0.6 W损耗就能提升能效1.2%

    For a 250 W output system, 0.6 W loss reduction leads to 1.2% efficiency improvement at 20% load

- 在240至300 W的大批量ATX应用领域中，双电感加单电容(LLC)半桥(HB)谐振拓扑结构是一种较好的解决方案，凭借初级MOSFET所采用的零电压开关(ZVS)技术，能够在轻载时实现更高能效

  Within the high-volume ATX application space of 240 – 300 W, LLC HB Resonant topology is a good solution to achieve higher efficiency at light load due to ZVS on primary MOSFETs

优化工作点
The Optimized Operating Point

- 增益特性曲线和所需的工作频率范围由这些参数来确定

  Gain characteristics shape and needed operating frequency range is given by these parameters:
  - 励磁电感(Lm)/串联谐振电感(Ls)比 Lm/Ls ratio
  - 谐振储能元件的特征阻抗 Characteristic impedance of the resonant tank
  - 负载值 Load value
  - 变压器匝数比 Transformer turns ratio
- 工作频率范围(fop)的工作点等于谐振频率(fs)时最具吸引力

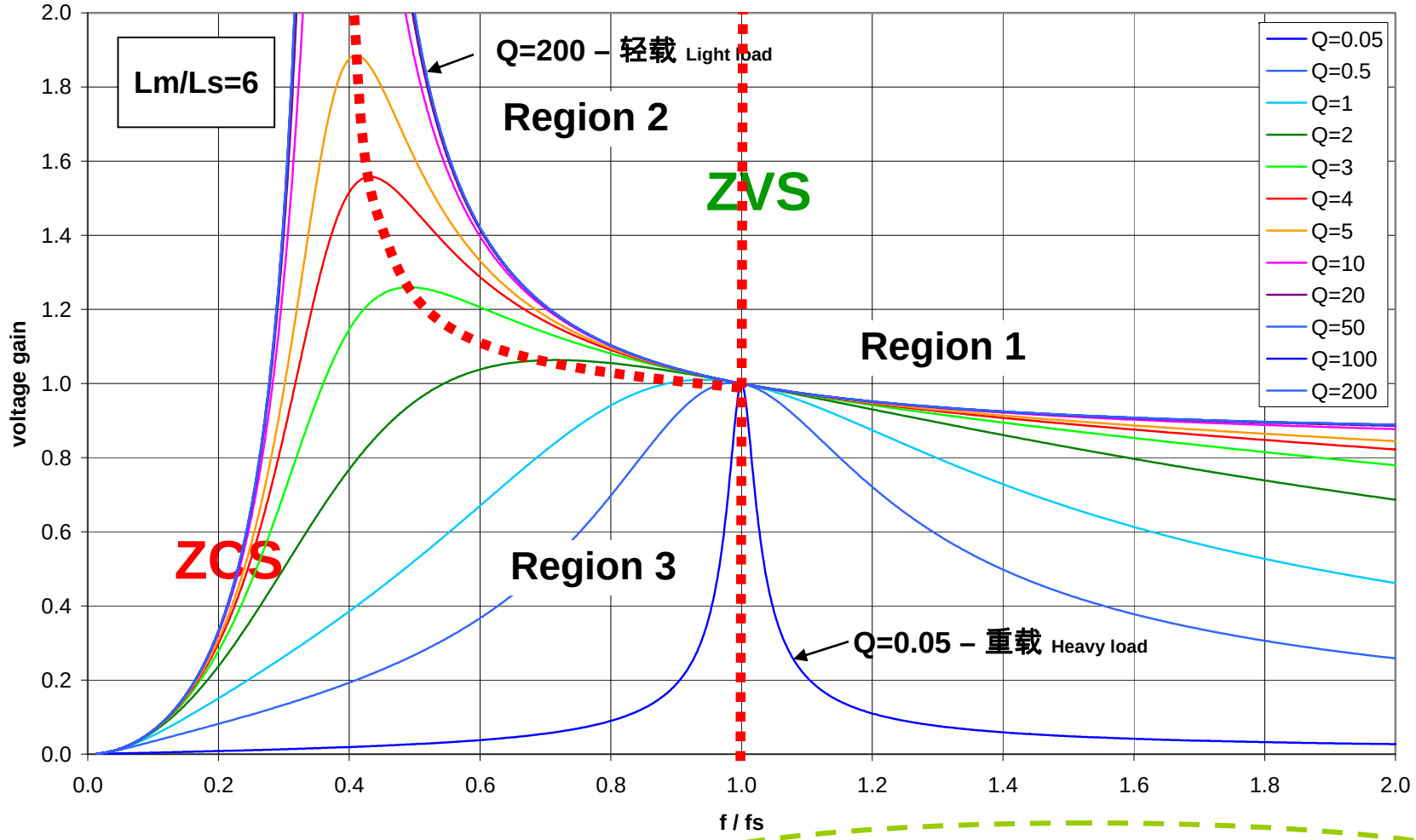
  fop = fs The operating point of fop = fs is the most attractive
  - 正弦初级电流 Sinusoidal primary current
  - MOSFET和次级整流器得到优化使用

    MOSFETs and secondary rectifiers optimally used
  - 只有特定输入电压和负载(通常是满载和额定大电容电压Vbulk)才能达到这个工作点

    This operating point can be reached only for specific input voltage and load (usually full load and nominal Vbulk)

规格化的增益特性曲线

Normalized Gain Characteristic

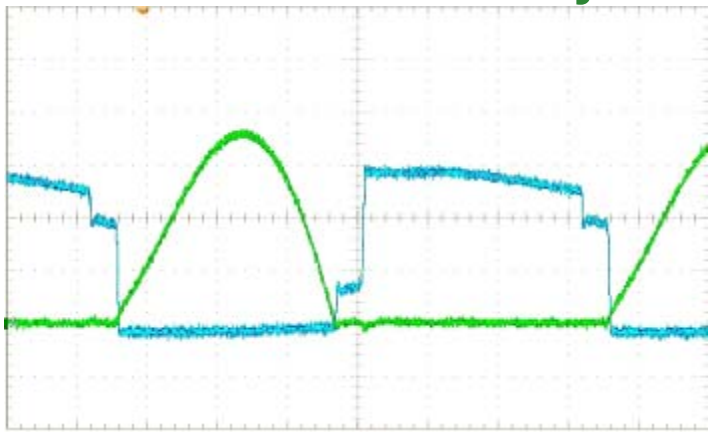


3区：ZCS区域 Region3: ZCS region

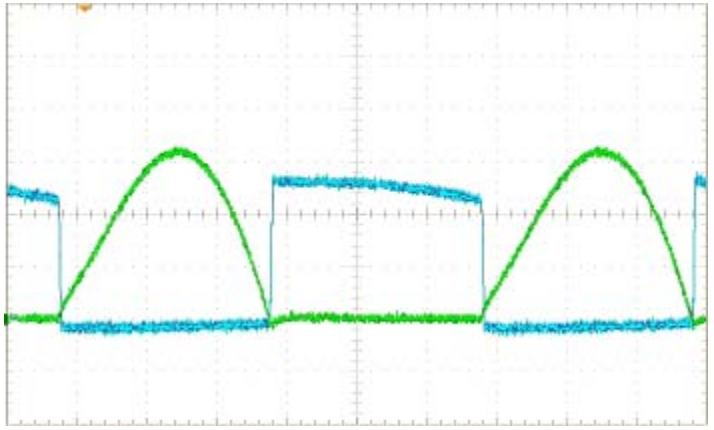
1区和2区：ZVS工作区 Region 1 and 2: ZVS operating regions

带二极管的LLC次级波形

Secondary Waveforms of LLC with Diode

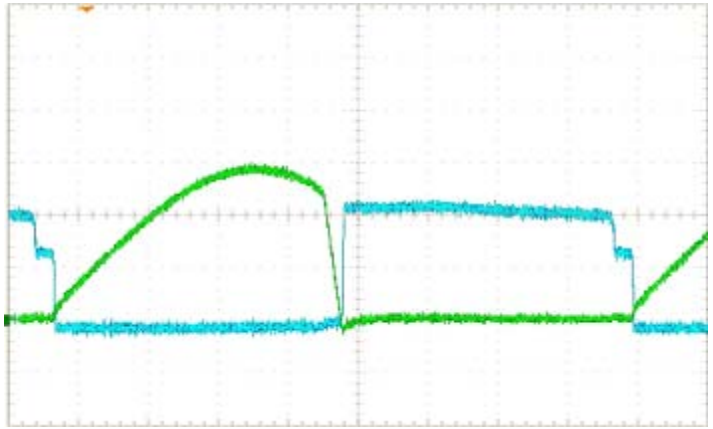


a) $F_{op} < F_s$



b) $F_{op} = F_s$

- 整流器电流 rectifier current
- 整流器电压 rectifier voltage



c)$F_{op} > F_s$

假定 Assumptions:

1. 次级电流是正弦波 Secondary current is sinusoidal
2. 工作状态是在谐振频率F_s Operating state is in resonant frequency F_s.

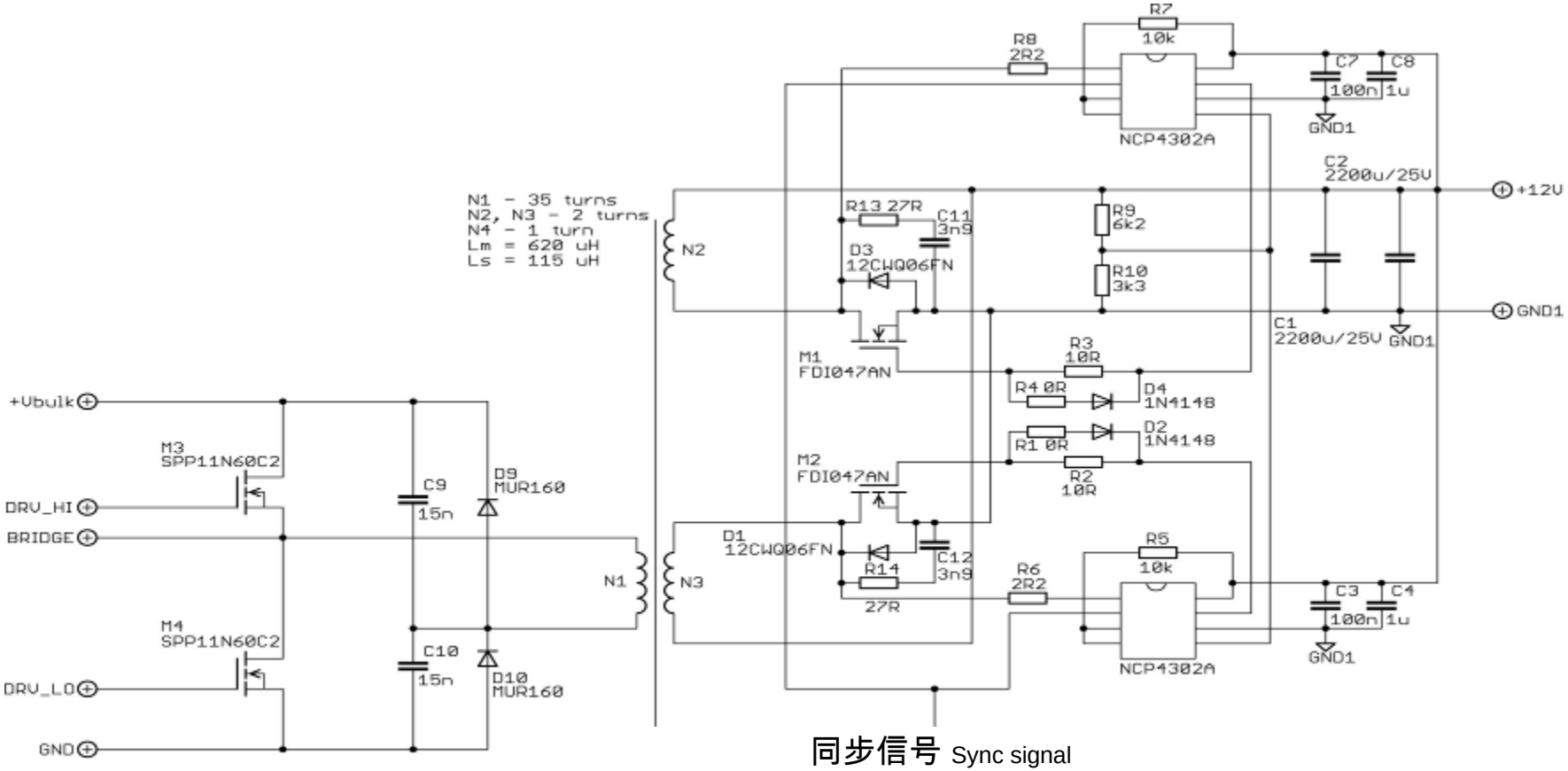
次级电流计算
Secondary Current Calculations

等式 Equations	24 V/ 10 A输出 24 V/10 A output	12 V/20 A输出 12 V/20 A output
均方根二极管电流 RMS diode current $I_{D\_RMS} = I_{out} \cdot \frac{\pi}{4}$	$I_{D\_RMS} = 7.85A$	$I_{D\_RMS} = 15.7A$
平均二极管电流 AVG diode current $I_{D\_AVG} = \frac{I_{out}}{2}$	$I_{D\_AVG} = 5A$	$I_{D\_AVG} = 10A$
峰值二极管电流 Peak diode current $I_{D\_PK} = I_{out} \cdot \frac{\pi}{2}$	$I_{D\_PK} = 15.7A$	$I_{D\_PK} = 31.4A$

- 即便在12 V电压，LLC拓扑结构的均方根电流仍在可接受范围
  Even at 12 V, the RMS current is still in the acceptable range for LLC topology

使用2颗NCP4302的同步整流解决方案

Synchronous Rectification Solution using 2 x NCP4302

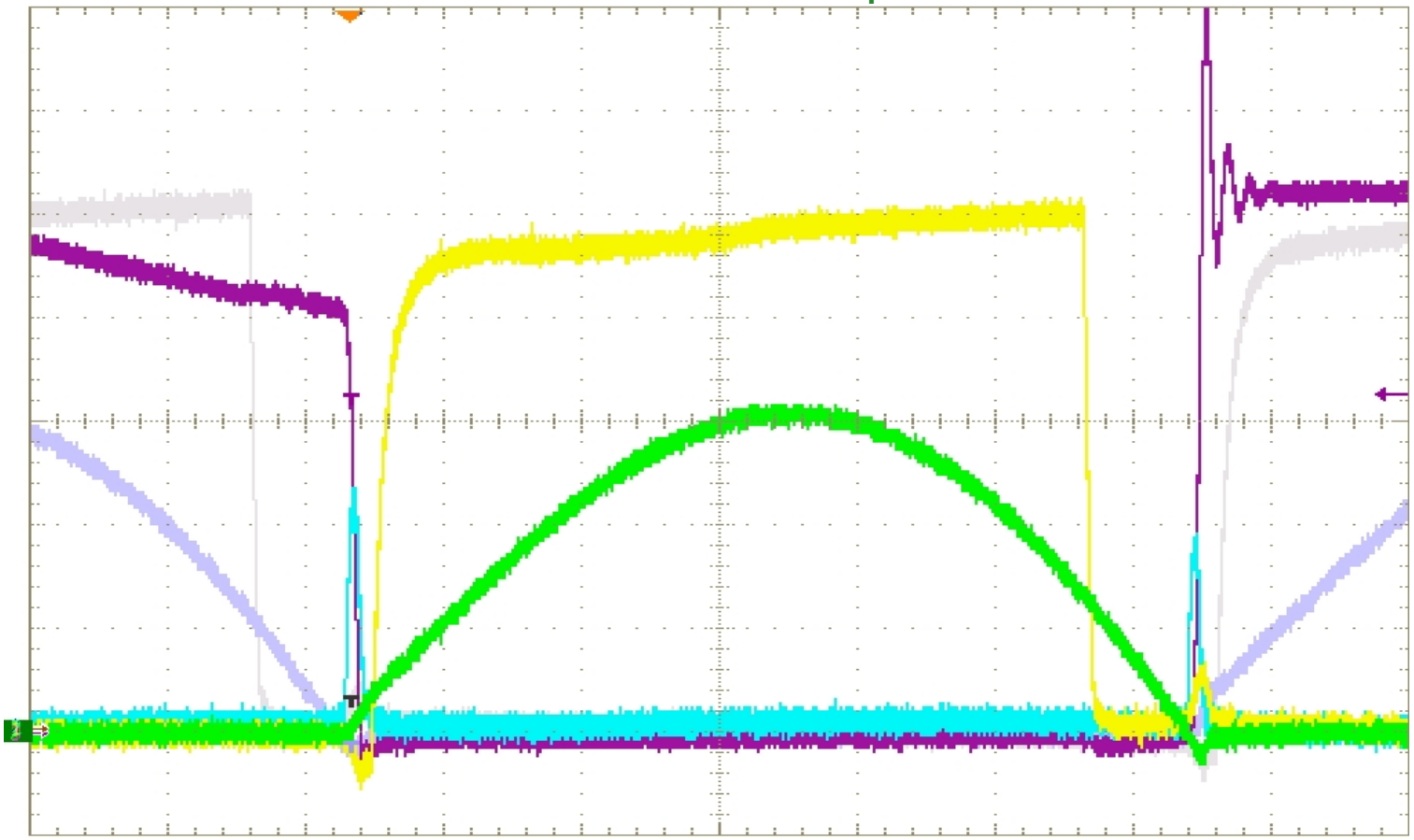


同步信号 Sync signal

正在申请专利 (patent pending)

F_{op}= F_s时的同步整流操作

SR Operation for F_{op}= F_s



C1 2.0V
C2 2.0V
C3 5.0V
C4 10.0A Ω

R1 2.0V 1.0µs
R2 10.0A 1.0µs

- 同步整流MOSFET门信号 SR MOSFET gate signal
- 整流器电流 Rectifier current
- 同步整流MOSFET漏电压 SR MOSFET drain voltage
- 触发器输入 Trigger input

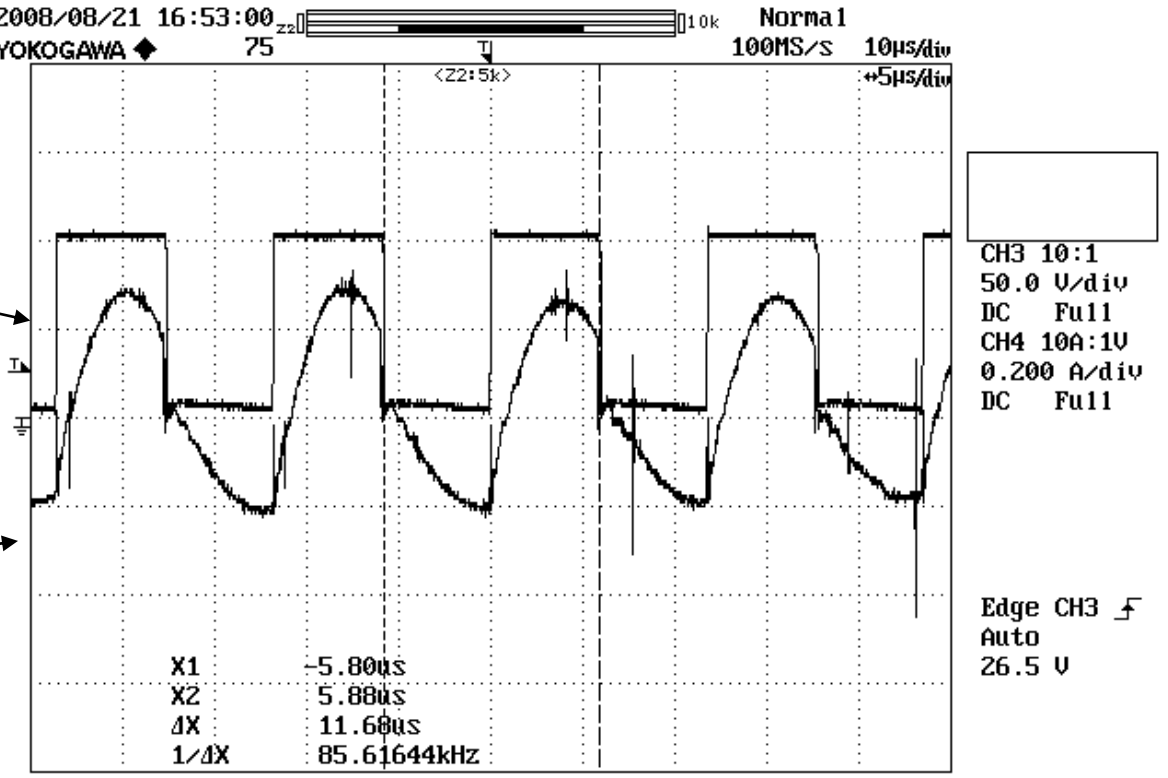
1.0µs/div
5.0GS/s 200ps/pt
A C3 16.3V

LLC半桥拓扑结构的工作点

The Operation Point of LLC HB

初级MOSFET的漏-源电压Vds
Vds of primary MOSFET

谐振储能元件中的电流 Current in resonant tank



- 谐振频率f_s为77 kHz The resonant frequency, f_s, is 77 kHz
- 满载时的工作频率为85 kHz The operating frequency at full load is 85 kHz
- 初级MOSFET工作在零电压开关(ZVS) Primary MOSFETs operate at ZVS

参考设计中主开关电源初级端的关键元件

Key Components of Main SMPS Stage in Reference Design–Primary Side

- NCP1396，具有高压驱动器的LLC控制器
  NCP1396, LLC controller featuring high voltage driver

- 集成谐振储能解决方案，如变压器的泄漏电感充当谐振电感
  Integrated resonant tank solution, i.e. the leakage inductance of transformer acts as resonant inductance.
  - EE35线轴 EE35 bobbin
  - 励磁电感为Lm=630 µH
  - 谐振电感为Ls=80 µH
  - 初级匝数为33匝，0.08*80绞合线 Np = 33 Turns, 0.08 * 80 Litz wires
  - 次级匝数为2匝，0.2*25绞合线 Ns = 2 Turns, 0.2 *25 Litz wires

- 初级侧MOSFET MOSFETs at primary side
  - STP12NM50, 12 A 500 V, 0.35 Ω $R_{ds(on)}$

参考设计中主开关电源次级端关键元件

Key Components of Main SMPS Stage in Ref. Design – Secondary Side

- 采用2颗同步整流器控制器NCP4302来控制同步整流MOSFET

  2 pcs of NCP4302, the synchronous rectifier controller, to control SR MOSFETs

- MOSFET用作整流器

  MOSFETs as rectifiers

  – STP80NF55, 80 A, 55 V, 5 mΩ $R_{ds(on)}$

- 二极管与同步整流MOSFET并联，以减小死区时间损耗

  Diodes in parallel the SR MOSFETs to reduce dead time losses

  – MBR20L45CTG, 20 A, 45 V

议程 Agenda

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  - 功率因数校正(PFC)段 PFC Stage
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次级转换器拓扑结构选择

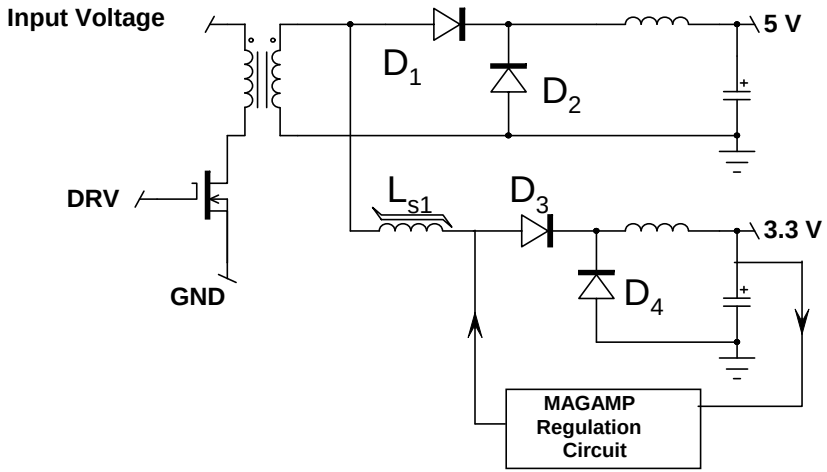
Topology Options for Secondary Convertor

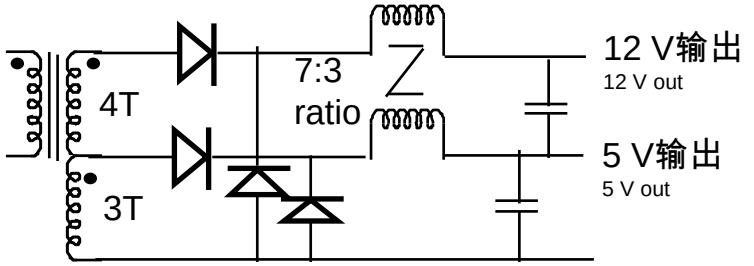
- 对交叉稳压的新的严格要求需要+3.3 V和+5 V输出零负载操作

  New stringent requirements for cross regulation require zero load operation on +3.3 V and +5 V outputs

- 堆叠变压器绕组、耦合输出扼流圈、磁放大途径难以满足新要求

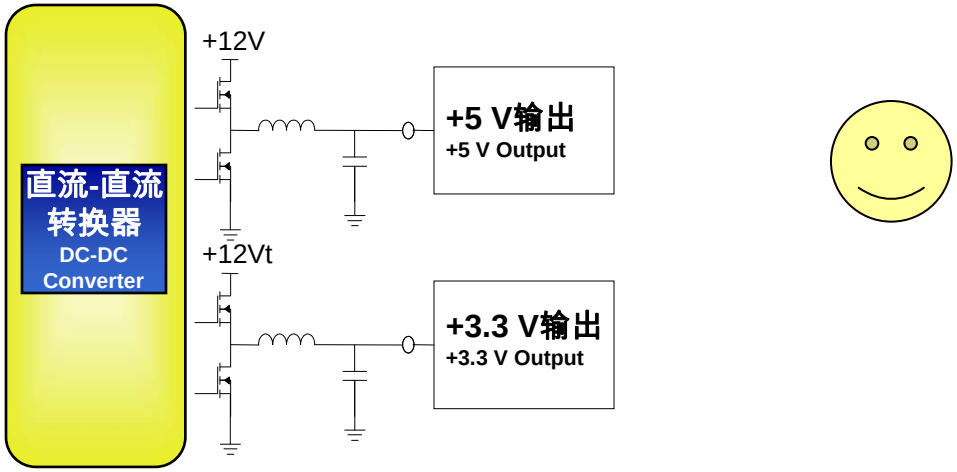
  Stacking transformer windings, coupling the output chokes, Mag-amp approach is hard to meet new requirements



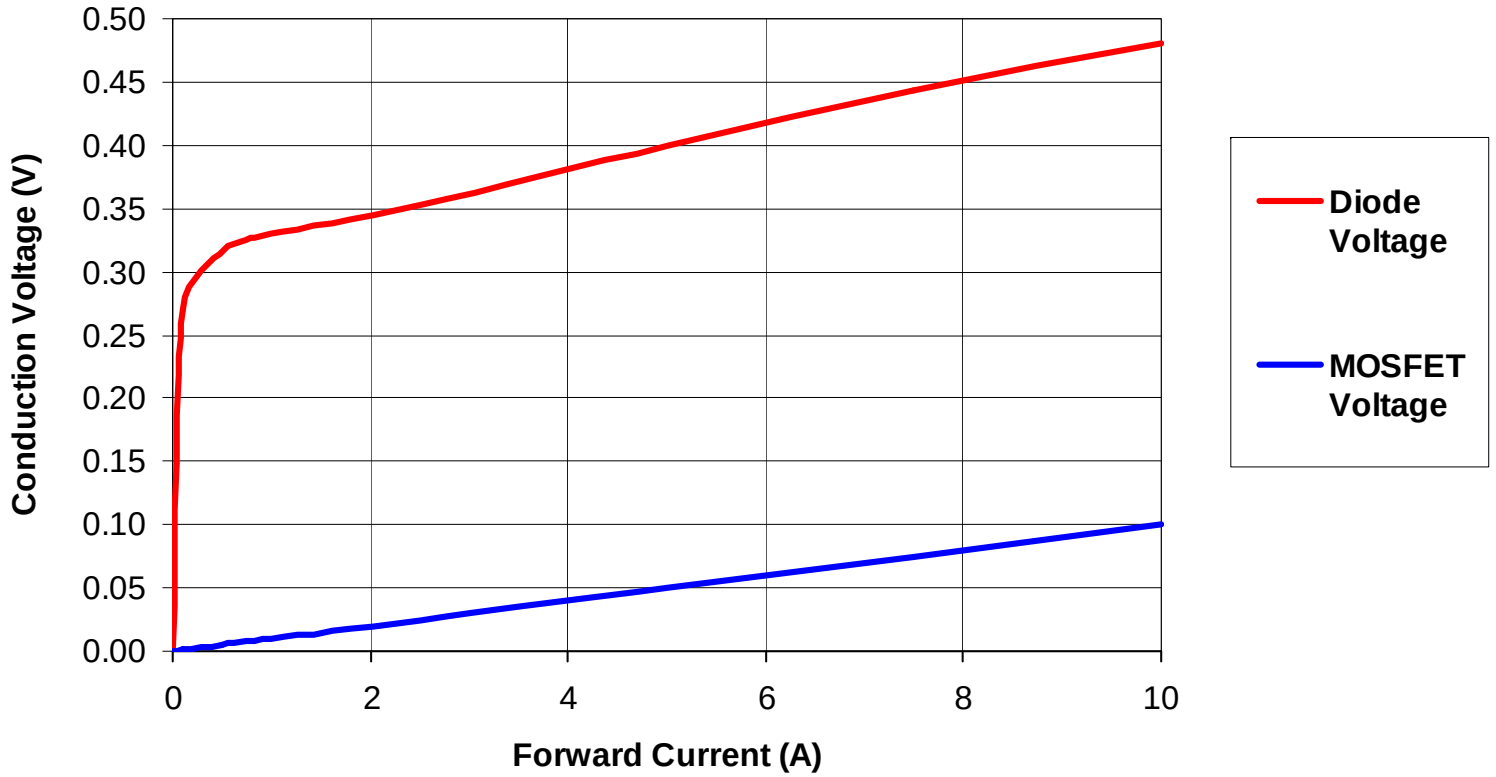


次级转换器拓扑结构选择
Topology Options for Secondary Convertor

- LLC半桥拓扑结构没有输出扼流圈 LLC HB does not have an output choke
  - 因此，它使其转向单路+12 V输出，其后跟随着产生+5 V和+3.3 V输出的直流-直流段 So, it lends itself to moving to a single +12 V output followed by a dc-dc stage to generate the +5 V and +3.3 V outputs
  - 这结构提供更好的交叉稳压性能 This provides better cross-regulation
  - 然而，由于增加额外功率处理段(+12 V至+5 V和+3.3 V)，能效是一项挑战 However, the efficiency is a challenge due to additional power processing stages (+12 V → +5 V and +3.3 V)



为什么在直流-直流中采用同步整流？
Why Synchronous Rectification in DC-DC?



- 二极管正向压降(0.35 V至0.45 V)将能效限制为3.3/(3.3+0.45)=88%

  Diode forward drop (0.35 V to 0.45 V) limits efficiency to 3.3/(3.3+0.45)=88%

同步整流降压转换中的设计考虑
Design Consideration in SR Buck

能够做些什么来降低功率损耗？
What can be done to Reduce Power Loss?

- 升级MOSFET，降低导通阻抗，选择低门极电荷
  Upgrade MOSFET, Reduce Rdson and chose low Qg
- 肖特基二极管并联在低端FET，以减小死区时间损耗
  Add Schottky diode in parallel low side FET to reduce dead time loss
- 使用直流电阻(DCR)较低的电感
  Use inductor with Low DCR
- 由于开关损耗原因，尽量使用高频(200 kHz至400 kHz)
  Use reasonably high frequency (200 kHz ~ 400 kHz) due to the switching lost
- 增加印制电路板(PCB)层数和铜厚度
  Increase PCB layers and copper thickness

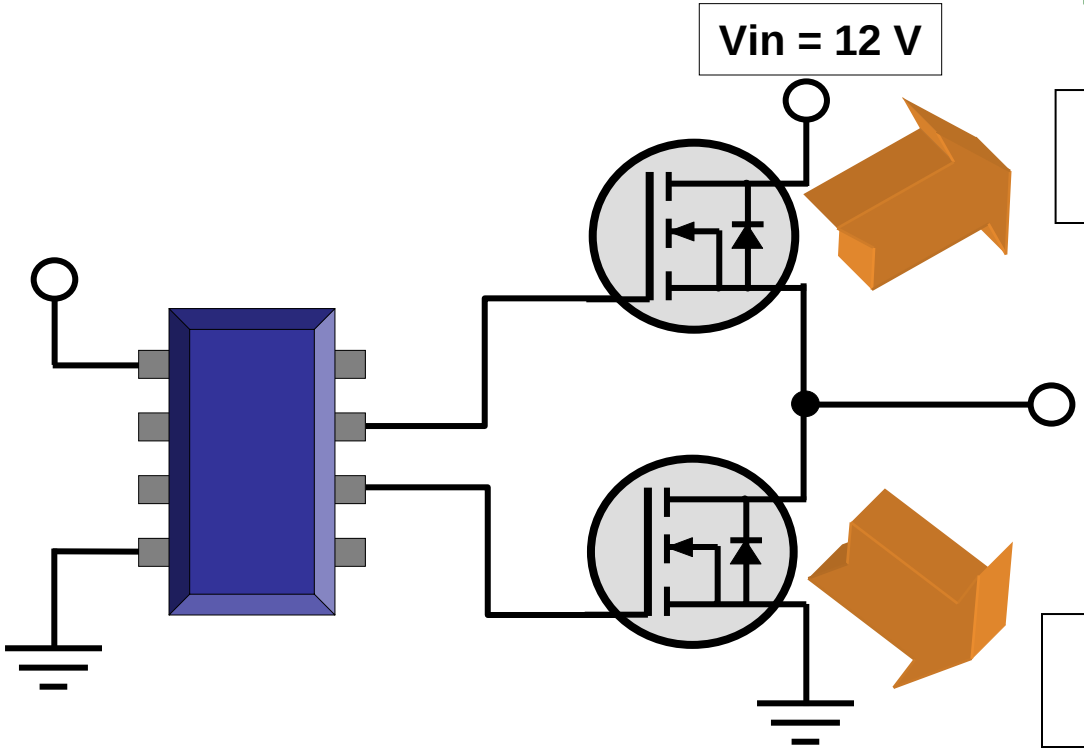
同步整流降压转换中的设计考虑(续)
Design Consideration in SR buck (Cont'd)

布线考虑 Layout Consideration:

- 敏感信号应该避开高dV/dT铜线，如门驱动(最少距离5 mm或0.2英寸) Sensitive signals should be kept away from the high dV/dT trace such as gate drive (minimum 5 mm or 0.2 in)
- 某些实际设计中，噪声隔离技术对紧凑型PCB板也是一种可选解决方案 In some practical design, noise isolation technique is also an alternative solution for compact PCB board
- 连接至IC的MOSFET门迹线必须短而直，并尽可能地宽 The MOSFET gate traces to the IC must be short, straight, and as wide as possible
- 门迹线上的"星形"或"T"形迹线长度保持最短化 Minimize the "Star" or "T" trace length on gate traces
- VCC旁路电容(0.1 F或更大)应当布设在离IC尽可能近的区域，对地连接必须尽可能地短 The VCC bypass capacitor (0.1 F or greater) should be located as close as possible to the IC and connection to GND must be as short as possible

同步降压应用中的MOSFET选择

MOSFETs selection for SR Buck Application



高端 HIGH SIDE

低门电荷 Low Gate charge

导通阻抗要求一般Fair Rdson

低端 LOW SIDE

门电荷较适宜 Fair Gate charge

低导通阻抗 Low Rdson

- 低端FET损耗中导电损耗占主导 The losses in the Low side FET is dominated by conduction losses
  - 因此，导通阻抗最重要 Therefore Rdson is the most important
- 高端FET影响开关速度 High side FET affects the switching speed
  - 因此，重要的是将开关电荷Qsw和门电阻Rg最小化，同时将导通阻抗Rdson维持在适宜水平 Therefore, it is important to minimize the switching charge Qsw and gate resistance Rg, while maintaining a reasonable on-resistance Rdson

参考设计中采用的关键直流-直流降压转换器元件
Key DC to DC Buck Converter Components used in Reference Design

- 2颗降压转换器控制器NCP1586，用于5 V和3.3 V输出
  2 pcs of NCP1586, the buck converter controller, for 5 V and 3.3 V outputs
  - NCP1586内置不交叠时序控制功能，用于防止整流MOSFET交叉导电
    NCP1586 built in non overlap timing control prevents cross conduction of rectification MOSFETs

- 电源扼流圈 Power chokes
  - 电感值μH 5.7 5.7 μH

- MOSFET
  NTD4809N, 58 A, 30 V, 14 mΩ $R_{ds(on)}$

参考设计中待机转换器采用的关键元件

Key components for Standby Converter in Reference Design

- NCP1027，带有700 V MOSFET的65 kHz PWM控制器
  NCP1027, 65 kHz PWM controller featuring 700 V MOSFET
  - 满载能效得到优化，因为得益于其可调节斜坡补偿特性，它允许深度的CCM工作 The efficiency at full load is optimized because it allows deep CCM operation thanks to the adjustable ramp compensation feature
  - 轻载能效得到优化，得益于跳周期工作模式The light load efficiency is optimized thanks to the skip mode operation

- 待机变压器 The Stby transformer
  - 采用EEL19线轴 EEL19 bobbin
  - 初级匝数为105匝，电感1.4 mH Np = 105 T, 1.4 mH
  - 次级匝数为6匝 Ns = 6 T
  - 辅助匝数为20匝 Naux = 20 T

- 二极管 Diode
  - MBR20L45CTG, 20 A, 45 V

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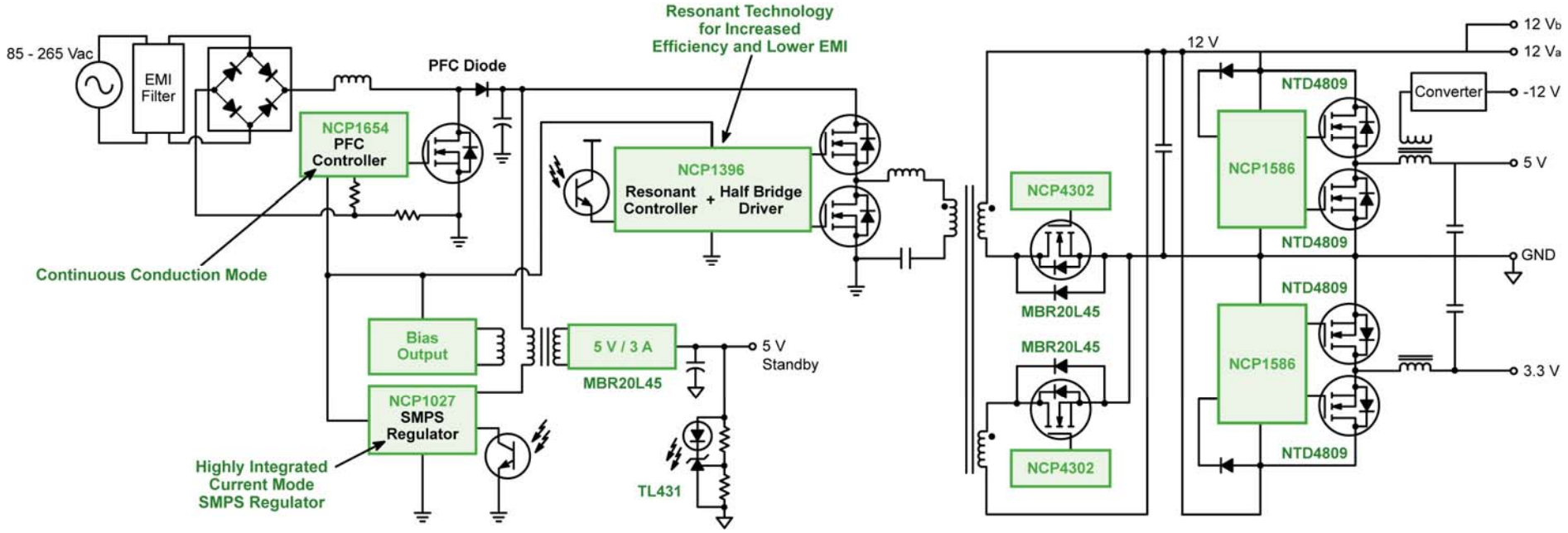
255 W 85 PLUS ATX电源参考设计

255 W, 85 PLUS ATX Power Supply Reference Design



Specification	20% load	50% load	100% load
• Multiple-Output • Non-Redundant • PFC 0.9 at 50%	85%	88%	85%

80 PLUS SILVER
Climate Savers 3

GreenPoint™ From ON Semiconductor

230 Vac、50%负载时的输入电流

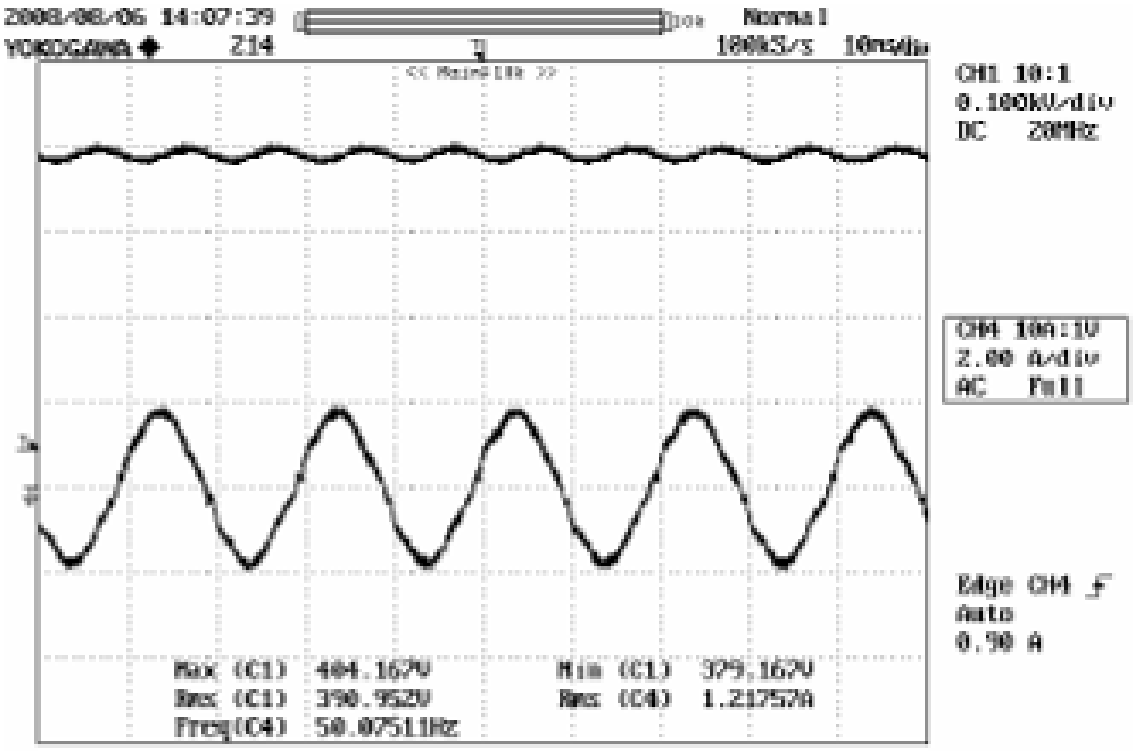
The Input Current at 230 Vac, 50 % Load

大电容电压

Vbulk

输入电流

Input Current



- 230 Vac输入、满载时功率因数为0.991 PF = 0.991 at 230 Vac input, full load
- 230 Vac输入、50%负载时功率因数为0.952 PF = 0.952 at 230 Vac, input, 50 % load

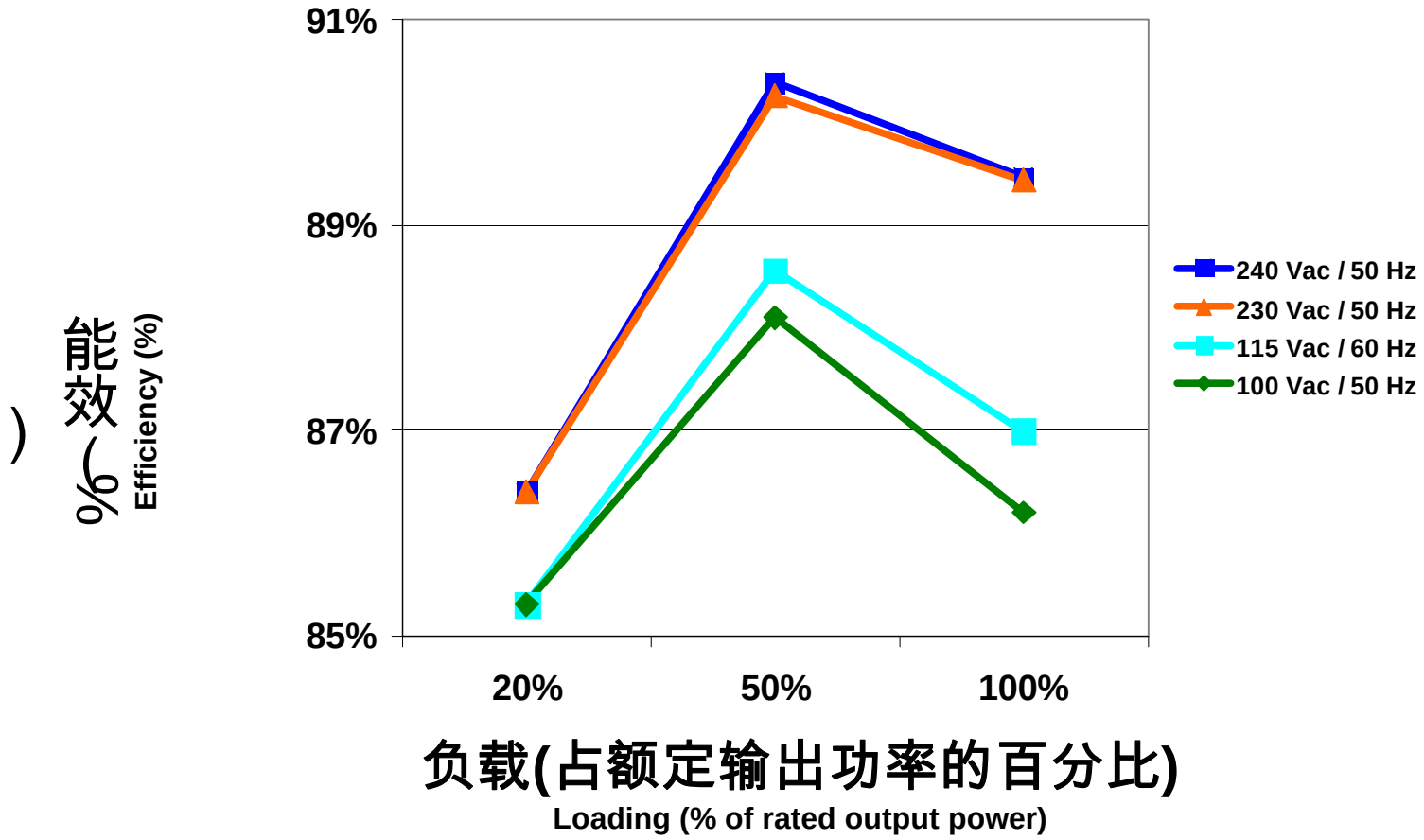
能效测试结果
Efficiency Results

输入 Input	20% Load	50% Load	100% Load
100 Vac	85.35%	88.61%	86.78%
115 Vac	85.57%	89.12%	87.59%
230 Vac	86.25%	90.69%	89.73%
240 Vac	86.69%	90.93%	89.86%
115 Vac时要求 **Requirement @ 115 Vac**	**85%**	**88%**	**85%**

能效测试结果
Efficiency Results

4条线路电压和3路负载时能效高于85%

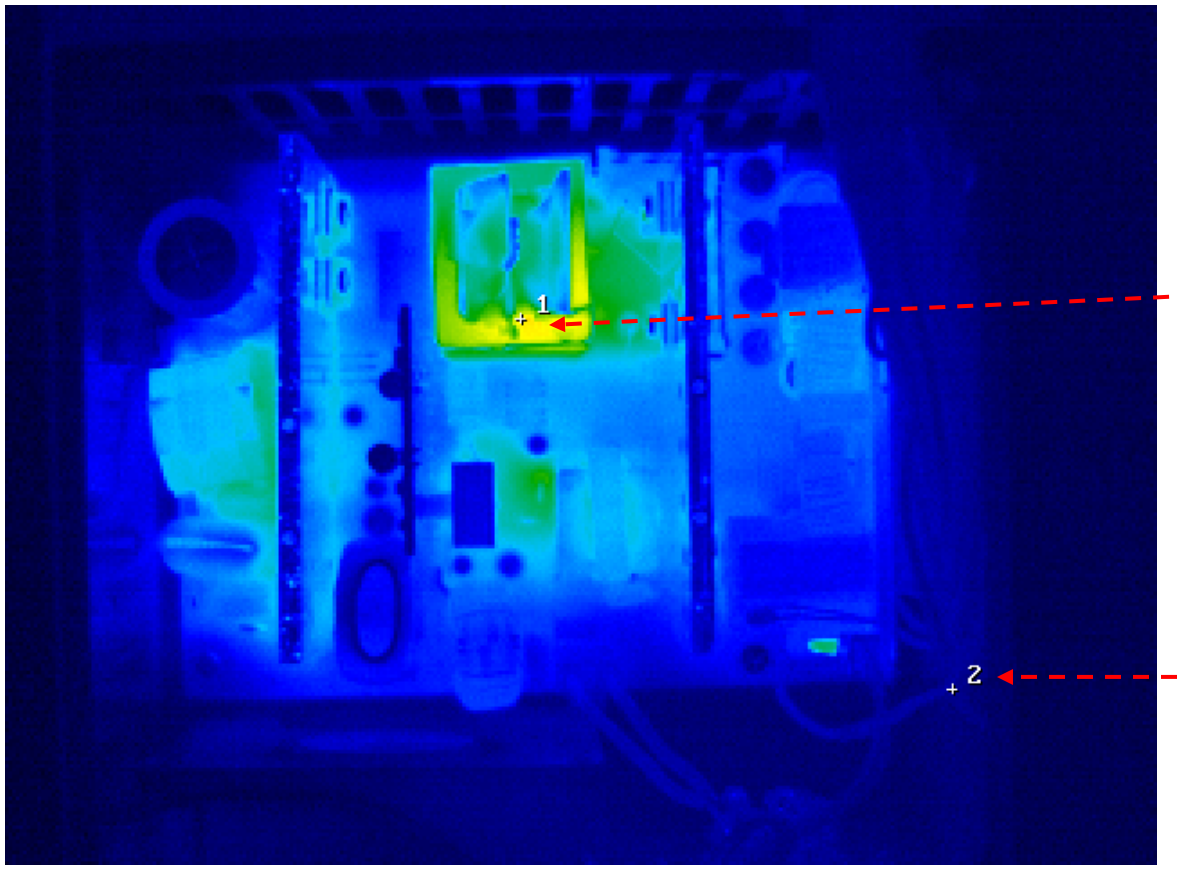
Efficiency > 85% @ 4 line voltages and 3 loads



输出电压稳压 The Output Voltage Regulation

Load	DC Terminal Voltage (V) & DC Load Current (A)											
	$12V_A$		$12V_B$		5V		3.3V		5Vsb		-12V	
(%)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)	(V)	(A)
20	12.01	1.90	12.02	1.03	5.01	1.89	3.25	1.01	4.99	0.48	-12.78	0.06
50	11.97	4.75	11.97	2.56	4.98	4.71	3.22	2.52	4.96	1.20	-12.37	0.16
100	11.86	9.50	11.87	5.12	4.93	9.43	3.18	5.02	4.91	2.39	-11.95	0.32

满载时的热测试结果 The Thermal Result @ 100 Vac, Full load



LLC半桥转换器为

85℃ LLC-HB transformer is 85℃

机壳外的环境温度约为

33℃ The ambient temperature outside the case is around 33 ℃

- **热性能得到优化** The thermal performance is optimized.

议程 Agenda

- 规范标准和市场要求 Regulation and Market Requirements
- 255 W ATX参考设计的目标规范 Target Specification for the Reference Design
- 架构考虑 Architectural Considerations
- 设计途径及每个电源段的关键考虑点 Design Approach & Key considerations for each stage
  - 功率因数校正(PFC)段 PFC Stage
  - 主开关电源(SMPS)段 Main SMPS Stage
  - 次级段 Secondary Stage
- 测试结果 Results
- 总结 Summary

总结
Summary

- 为了获得较高的电源总能效，直接的架构考虑和每一段的元器件选择至关重要

  In order to obtain high overall efficiency for the power supply, up-front architectural considerations and component selection for each stage are critical

- 需要采用软开关拓扑结构，配以高能效的PFC段和输出段，才能实现OEM新的能效要求

  A soft-switching topology, coupled with highly efficient PFC stage and output stage are required to meet the new efficiency requirements of the OEMs

- 安森美半导体的85% PLUS提供的参考设计经过完全测试、强固和高性价比的解决方案

  ON Semiconductor's 85% PLUS reference design offers a fully tested, robust and cost-effective solution

  – 这解决方案还能够进行优化，提供更高能效，用于其它额定输出功率

    This solution can be optimized for higher efficiencies and other output power ratings

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies