Failsafe™ 2.5V/ 3.3V Zero Delay Buffer

Features

- **Internal DCXO for continuous glitch-free operation**
- **Zero input-output propagation delay**
- **100ps typical output cycle-to-cycle jitter**
- **110 ps typical Output-output skew**
- **1 MHz–200 MHz reference input**
- **Supports industry standard input crystals**
- **200 MHz (commercial), 166 MHz (industrial) outputs**
- **5V-tolerant inputs**
- **Phase-locked loop (PLL) Bypass Mode**
- **Dual Reference Inputs**
- **28-pin SSOP**
- **Split 2.5V or 3.3V output power supplies**
- **3.3V core power supply**
- **Industrial temperature available**

Functional Description

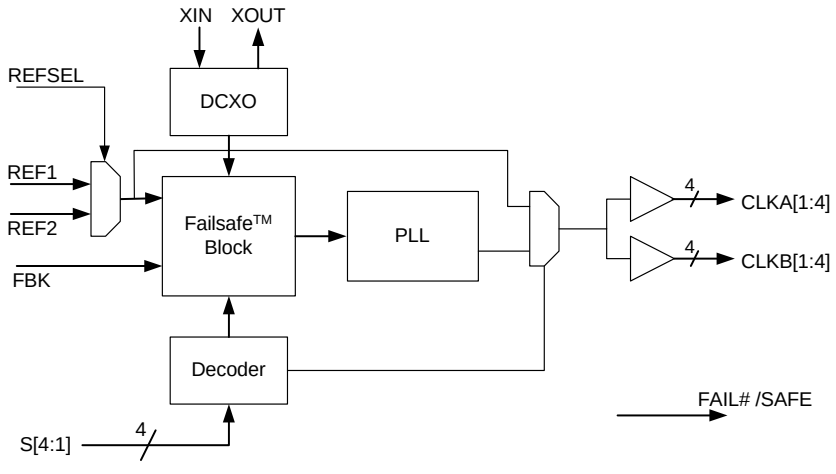
The CY23FS08 is a FailSafe™ Zero Delay Buffer with two reference clock inputs and eight phase-aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

Continuous, glitch-free operation is achieved by using a DCXO, which serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

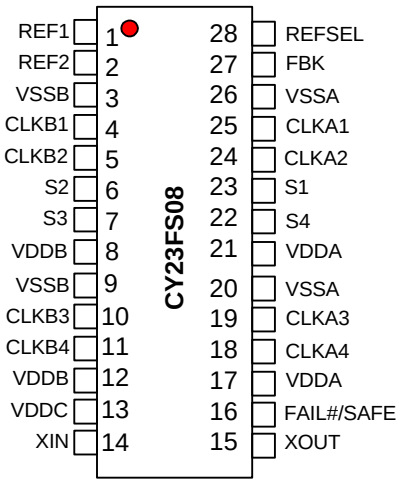
The unique feature of the CY23FS08 is that the DCXO is in fact the primary clocking source, which is synchronized (phase-aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal, which will be connected to the DCXO must be chosen to be an integer factor of the frequency of the reference clock. This factor is set by four select lines: S[4:1]. please see *Table 1*. The CY23FS08 has three split power supplies; one for core, another for Bank A outputs and the third for Bank B outputs. Each output power supply, except VDDC can be connected to either 2.5V or 3.3V. VDDC is the power supply pin for internal circuits and must be connected to 3.3V.

Block Diagram



Pin Configuration



28-pin SSOP

Pin Definitions

Pin Number	Pin Name	Description
1,2	REF1,REF2	**5V-tolerant, reference clock inputs**[4].
4,5,10,11	CLKB[1:4]	**Bank B clock outputs**.[1, 2]
25,24,19,18	CLKA[1:4]	**Bank A clock outputs.**[1, 2]
27	FBK	**Feedback input to the PLL**.[1,]
23,6,7,22	S[1:4]	**Frequency select pins/PLL and DCXO bypass**.[3]
14	XIN	**Reference crystal input**.
15	XOUT	**Reference crystal output**.
16	FAIL#/SAFE	**Valid reference indicator**. A high level indicates a valid reference input.
13	VDDC	**3.3V power supply for the internal circuitry**.
8,12	VDDB	**2.5V or 3.3V power supply for Bank B outputs**.
3,9	VSSB	**Ground**.
17,21	VDDA	**2.5V or 3.3V power supply for Bank A outputs**.
20,26	VSSA	**Ground**.
28	REFSEL	**Reference select**. Selects the active reference clock from either REF1 or REF2. REFSEL = 1, REF1 is selected, REFSEL = 0, REF2 is selected.

Table 1. Configuration Table

S[4:1]	XTAL (MHz)		REF(MHz)		OUT(MHz)		REF:OUT ratio	REF:XTAL ratio	Out:XTAL ratio
	Min.	Max.	Min.	Max.	Min.	Max.			
0000			PLL and DCXO Bypass mode						
1000	8.33	30	16.67	60.00	8.33	30.00	÷2	2	1
1110	9.50	30	57.00	180.00	28.50	90.00	÷2	6	3
0101	8.50	30	6.80	24.00	1.70	6.00	÷4	4/5	1/5
1011	8.33	30	25.00	90.00	6.25	22.50	÷4	3	3/4
0011	8.33	30	2.78	10.00	2.78	10.00	x1	1/3	1/3
1001	8.33	30	8.33	30.00	8.33	30.00	x1	1	1
1111	8.00	25	32.00	100.00	32.00	100.00	x1	4	4
1100	8.00	25	64.00	200.00	64.00	200.00	x1	8	8
0001	8.33	30	1.04	3.75	2.08	7.50	x2	1/8	1/4
0110	8.33	30	4.17	15.00	8.33	30.00	x2	1/2	1
1101	8.33	30	16.67	60.00	33.33	120.00	x2	2	4
0100	8.33	30	4.17	15.00	16.67	60.00	x4	1/2	2
1010	8.33	30	12.50	45.00	50.00	180.00	x4	3/2	6
0010	8.33	30	1.39	5.00	11.11	40.00	x8	1/6	4/3
0111	8.33	30	6.25	22.50	50.00	180.00	x8	3/4	6

Notes:
1. For normal operation, connect either one of the eight clock outputs to the FBK input.
2. Weak pull-downs on all outputs.
3. Weak pull-ups on these inputs.
4. Weak pull-downs on these inputs.

FailSafe Function

The CY23FS08 is targeted at clock distribution applications that could or which currently require continued operation should the main reference clock fail. Existing approaches to this requirement have utilized multiple reference clocks with either internal or external methods for switching between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another, often requiring complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL, greatly simplifying system design.

The CY23FS08 PLL is driven by the crystal oscillator, which is phase-aligned to an external reference clock so that the output of the device is effectively phase-aligned to reference via the external feedback loop. This is accomplished by utilizing a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±300 ppm from its nominal frequency.

In this mode, should the reference frequency fail (i.e., stop or disappear), the DCXO maintains its last setting and a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS08 provides four select bits, S1 through S4 to control the reference to crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag will be set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag will be cleared, indicating to the system that the selected reference is valid.

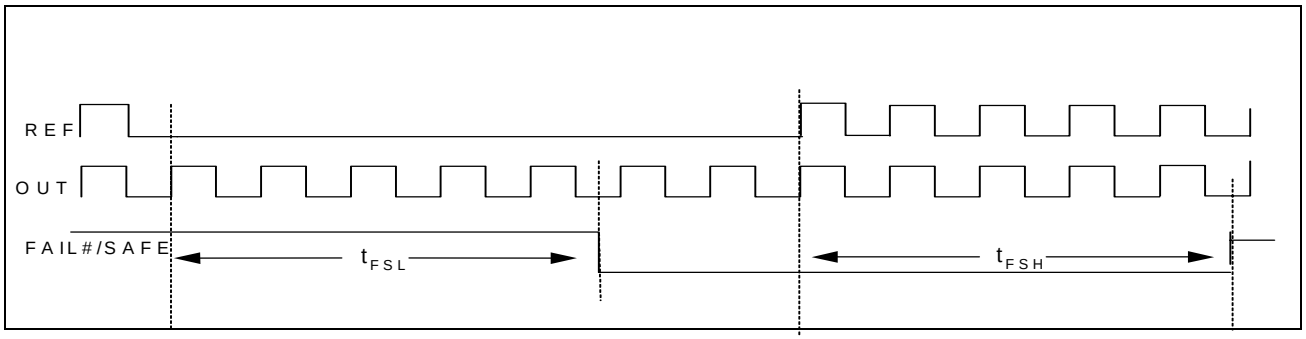


Figure 1. Fail#/Safe Timing for Input Reference Failing Catastrophically

$$t_{FSL(max)} = 2 (t_{REF} \times n) + 25ns$$

$$n = \frac{F_{REF}}{F_{XTAL}} = 4 \text{ (in above example)}$$

$$t_{FSH(min)} = 12 (t_{REF} \times n) + 25ns$$

Figure 2. Fail#/Safe Timing Formula

Table 2. FailSafe Timing Table

Parameter	Description	Conditions	Min.	Max.	Unit
t_{FSL}	Fail#/Safe Assert Delay	Measured at 80% to 20%, Load = 15 pF		See *Figure 2*	ns
t_{FSH}	Fail#/Safe Deassert Delay	Measured at 80% to 20%, Load = 15 pF	See *Figure 2*		ns

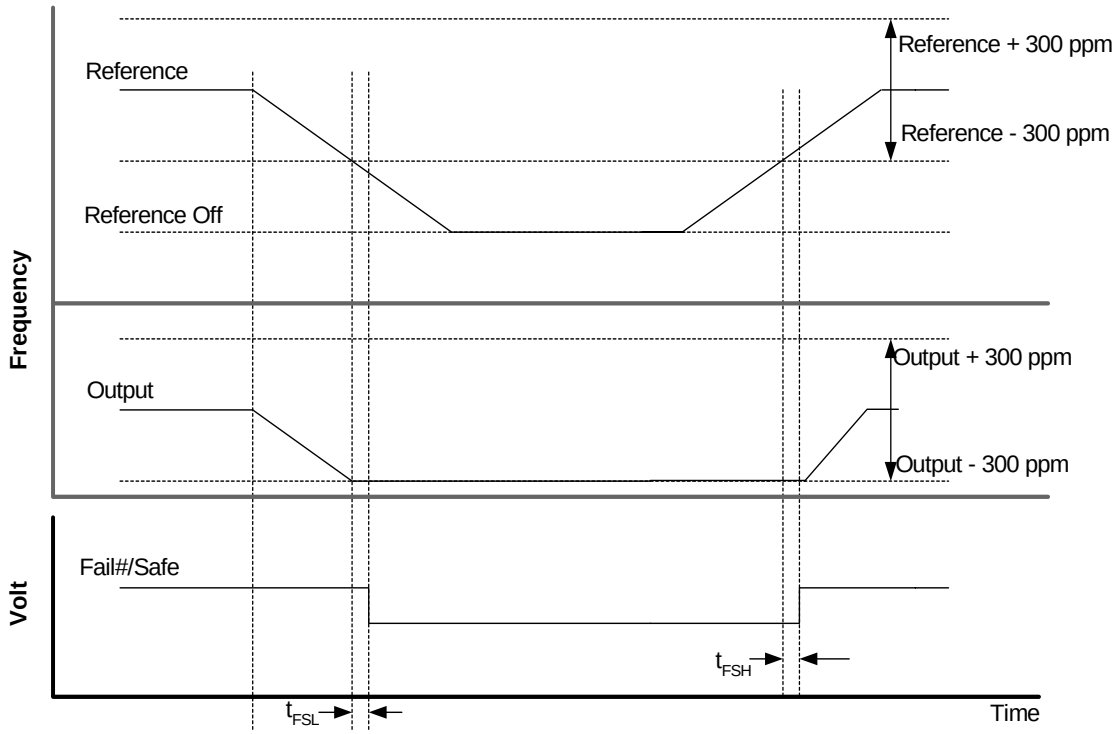


Figure 3. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range

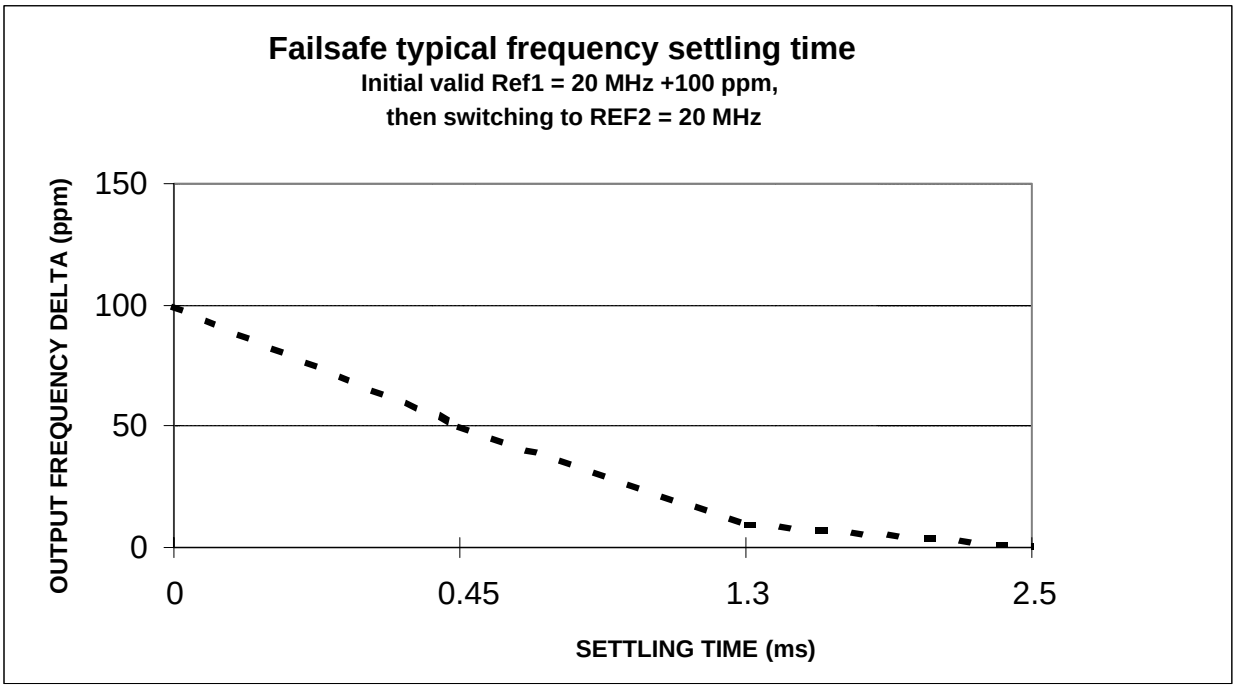


Figure 4. FailSafe Reference Switching Behavior

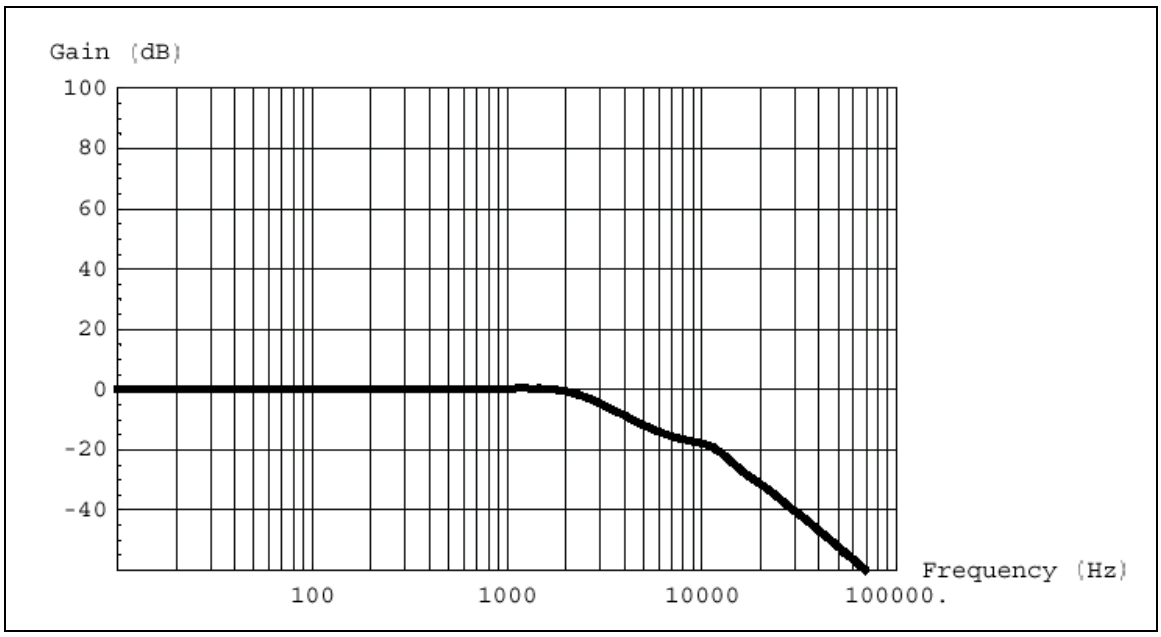


Figure 5. FailSafe Effective Loop Bandwidth (min)

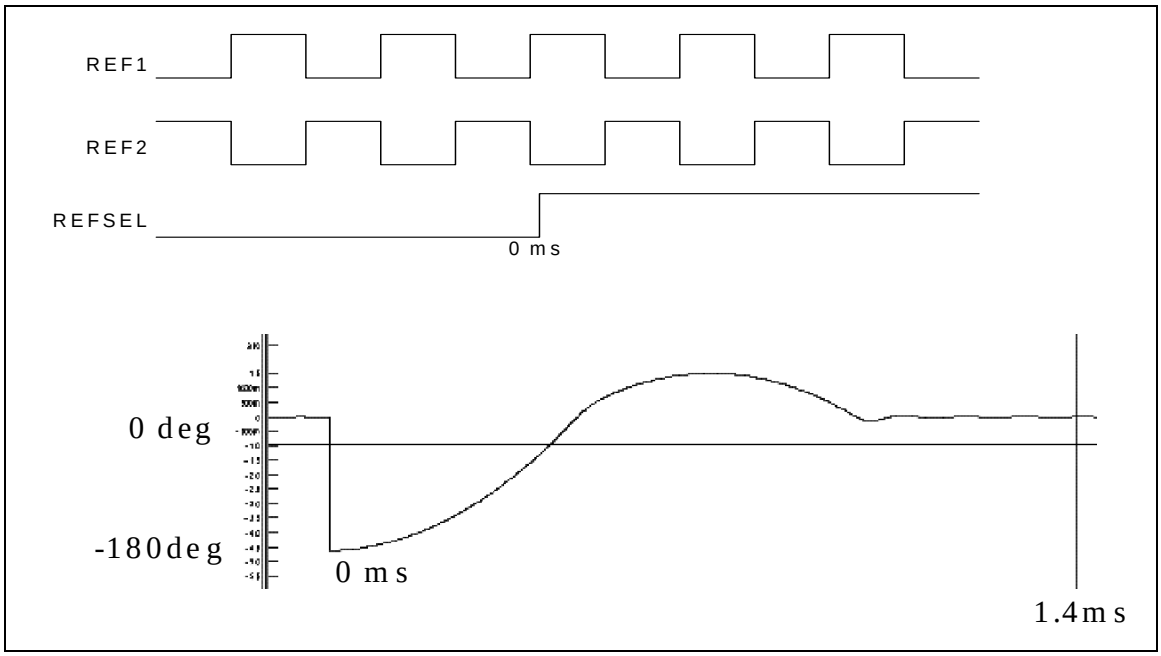


Figure 6. Sample Timing of Muxing Between Two Reference Clocks 180°C Out of Phase and Resulting Output Phase Offset Typical Settling Time (105 MHz)

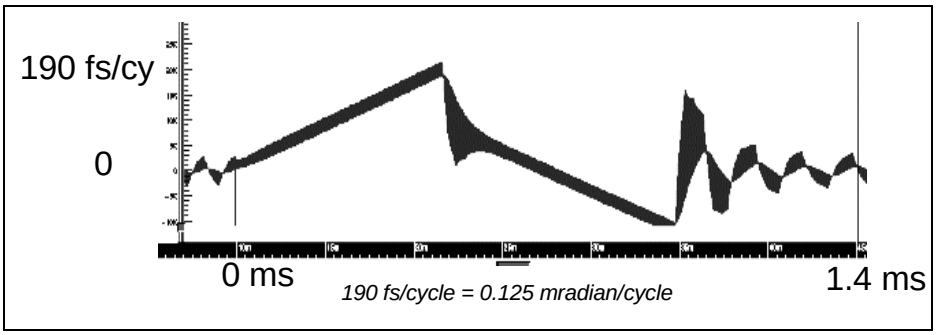
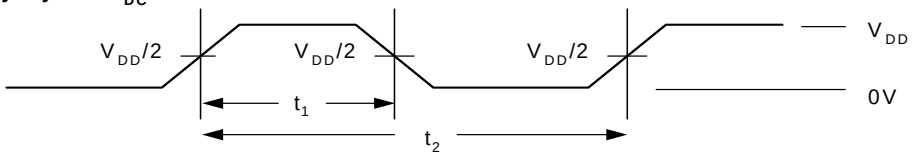
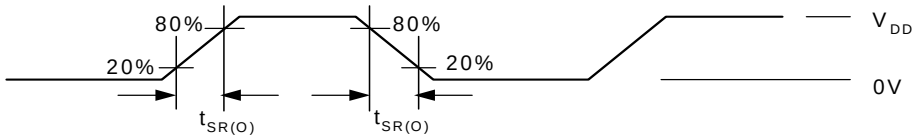


Figure 7. Resulting Output Dphase/Cycle Typical Rate of Change (105 MHz)

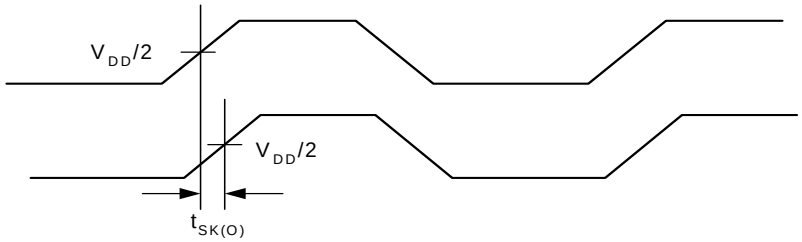
Duty Cycle - t_{DC}



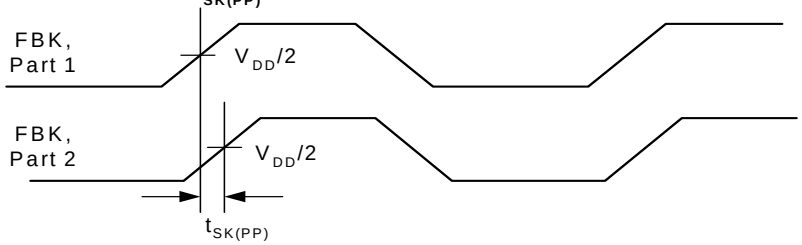
Slew Rate - $t_{(SR)}$



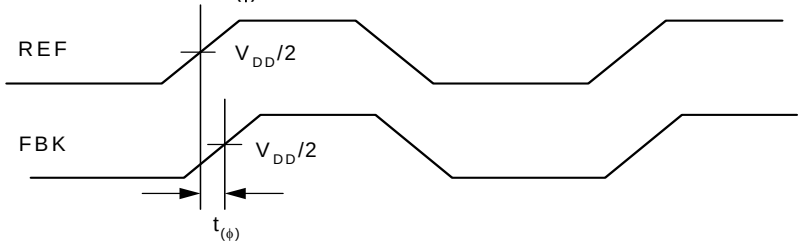
Output-Output Skew - $t_{SK(O)}$



Part to Part Skew - $t_{SK(PP)}$



Static Phase Offset - $t_{(\phi)}$



XTAL Selection Criteria and Application Example

Choosing the appropriate XTAL will ensure the FailSafe device will be able to span an appropriate frequency of operation. Also, the XTAL parameters will determine the holdover frequency stability. Critical parameters are as follows. Our recommendation is to choose:

- Low C0/C1 ratio (240 or less) so that the XTAL has enough range of pullability.
- Low temperature frequency variation
- Low manufacturing frequency tolerance
- Low aging.

C0 is the XTAL shunt capacitance (3 pF–7 pF typ.).

C1 is the XTAL motional capacitance (10 fF–30 fF typ).

The capacitive load as “seen” by the XTAL is across its terminals. It is named Clmin (for minimum value), and Clmax (for maximum value).These are used for calculating the pull range.

Please note that the Cl range “center” is approximately 20 pF, but we may not want a XTAL calibrated to that load. This is because the pullability is not linear, as represented in the equation above. Plotting the pullability of the XTAL shows this expected behavior as shown in *Figure 8*. In this example, specifying a XTAL calibrated to 14 pF load provides a balanced ppm pullability range around the nominal frequency.

Example:[5]

Clmin = (12 pF IC input cap + 0 pF pulling cap+ 6 pF trace cap on board)/2 = 9 pF

Clmax = (12 pF IC input cap + 48 pF pulling cap+ 6 pF trace cap on board)/2 = 33 pF

Pull Range =(fClmin–fClmax)/fClmin = ((C1)/2)[(1/(C0+Clmin))–(1/(C0+Clmax))]

Pull Range in ppm = ((C1)/2)[(1/(C0+Clmin))–(1/(C0+Clmax))] × 10^6

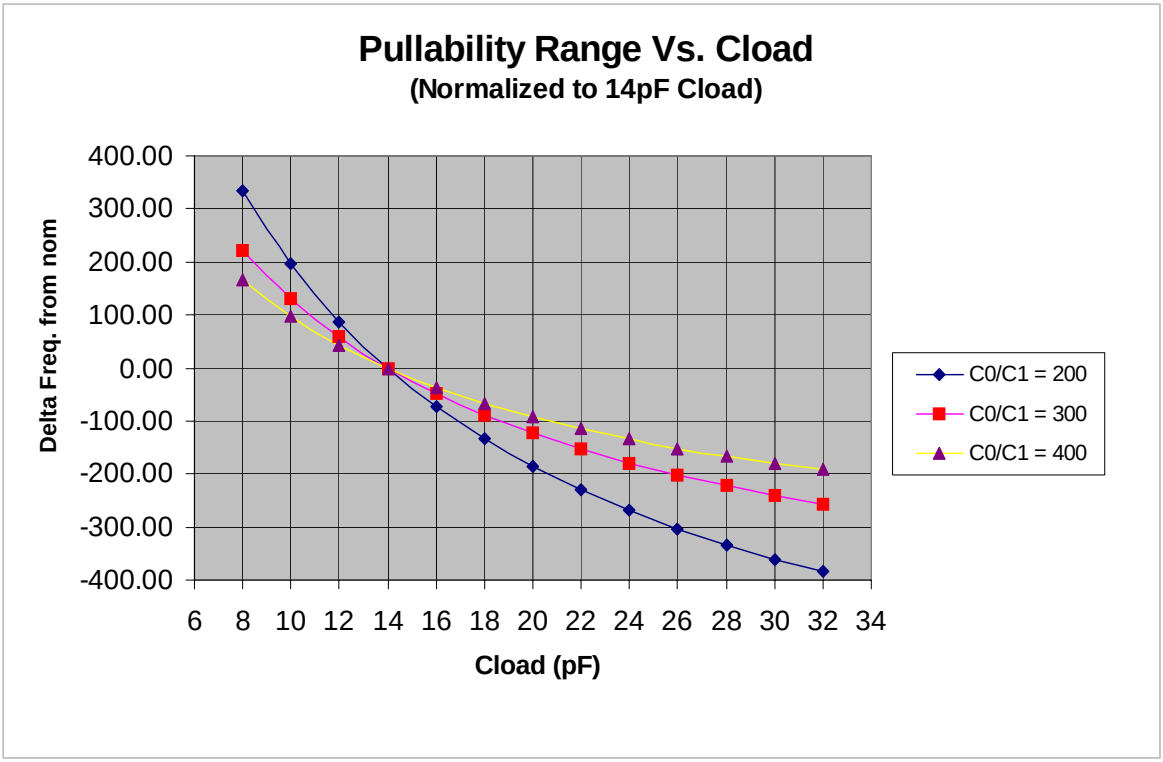


Figure 8. Frequency vs. Cload Behavior for Example XTAL

Note:

5. The above example shows the maximum range the FailSafe internal capacitor array is capable of (0 to 48.6 pF).Cypress recommends the min./max capacitor array values be programmed to a narrower range such as 6 pF–30 pF, or 7.5 pF–27 pF. This ensures the XTAL operates between series resonance and anti-resonance. Please contact Cypress for choosing these range settings.

Table 3. Pullability Range from XTAL with Different C0/C1 Ratio

C0/C1 Ratio	Cload(min.)	Cload(max.)	Pullability Range	
200	8.0	32.0	–385	333
300	8.0	32.0	–256	222
400	8.0	32.0	–192	166

Calculated value of the pullability range for the XTAL with C0/C1 ratio of 200, 300 and 400 are shown in *Table 3*. For this calculation Cl(min) = 8pF and Cl(max)= 32pF has been used. Using a XTAL that has a nominal frequency specified at load capacitance of 14pF, almost symmetrical pullability range has been obtained.

Next, it is important to calculate the pullability range including error tolerances. This would be the **capture range** of the input reference frequency that the FailSafe device and XTAL combination would reliably span.

Calculating the **capture range** involves subtracting error tolerances as follows:

Parameter ..... f error (ppm)

Manufacturing frequency tolerance 15

Temperature stability 30

Aging 3

Board/trace variation 5

Total 53

Example: Capture Range for XTAL with C0/C1 Ratio of 200

Negative Capture Range= –385 ppm + 53 ppm = –332 ppm

Positive Capture Range = 333 ppm – 53 ppm = +280 ppm

It is important to note that the XTAL with lower C0/C1 ratio has wider **pullability/capture range** as compared to the higher C0/C1 ratio. This will help the user in selecting the appropriate XTAL for use in the FailSafe application.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD}+0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Commercial Grade	0	70	°C
		Industrial Grade	–40	85	°C
T_J	Temperature, Junction	Functional		125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000		V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	36.17		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	100.6		°C/W
UL–94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Recommended Pullable Crystal Specifications[6]

Parameter	Name	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8.00	–	30.00	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPLI}	Third overtone separation from 3*F_{NOM}	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from 3*F_{NOM}	Low side	–	–	–150	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Table 4. Operating Conditions for FailSafe Commercial/Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DDC}	3.3V Supply Voltage	3.135	3.465	V
V_{DDA}, V_{DDB}	2.5V Supply Voltage Range	2.375	2.625	V
	3.3V Supply Voltage Range	3.135	3.465	V
T_A	Ambient Operating Temperature, Commercial	0	70	°C
	Ambient Operating Temperature, Industrial	–40	85	°C
C_L	Output Load Capacitance (Fout ≤ 100 MHz)		30	pF
	Output Load Capacitance (Fout > 100 MHz)		15	pF
C_{IN}	Input Capacitance (except XIN)		7	pF
C_{XIN}	Crystal Input Capacitance (all internal caps off)	10	13	pF
T_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

Note:

6. Ecliptek ECX-5788-13.500M, ECX-5807-19.440M, ECX-5872-19.53125M, ECX-5806-18.432M, ECX-5808-27.000M, ECX-5884-17.664M, ECX-5883-16.384M,ECX-5882-19.200M,ECX-5880-24.576M meet these specifications.

Table 5. Electrical Characteristics for FailSafe Commercial/Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS Levels, 30% of V_{DD}			0.3xV_{DD}	V
V_{IH}	Input High Voltage	CMOS Levels, 70% of V_{DD}	0.7xV_{DD}			V
I_{IL}	Input Low Current	V_{IN} = V_{SS} (100k pull-up only)			50	µA
I_{IH}	Input High Current	V_{IN} = V_{DD} (100k pull-down only)			50	µA
I_{OL}	Output Low Current	V_{OL} = 0.5V, V_{DD} = 2.5V		18		mA
		V_{OL} = 0.5V, V_{DD} = 3.3V		20		mA
I_{OH}	Output High Current	V_{OH} = V_{DD} – 0.5V, V_{DD} = 2.5V		18		mA
		V_{OH} = V_{DD} – 0.5V, V_{DD} = 3.3V		20		mA
I_{DDQ}	Quiescent Current	All Inputs grounded, PLL and DCXO in bypass mode, Reference Input = 0			250	µA

Table 6. Switching Characteristics for FailSafe Commercial/Industrial Temperature Devices

Parameter[8]	Description	Test Conditions	Min.	Typ.	Max.	Unit
f_{REF}	Reference Frequency	Commercial Grade	1.04	–	200	MHz
		Industrial Grade	1.04	–	166.7	MHz
f_{OUT}	Output Frequency	15-pF Load, Commercial Grade	1.70	–	200	MHz
		15-pF Load, Industrial Grade	1.70	–	166.7	MHz
f_{XIN}	DCXO Frequency		8.0	–	30	MHz
t_{DC}	Duty Cycle	Measured at V_{DD}/2	47	–	53	%
$t_{SR(I)}$	Input Slew Rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	–	4.0	V/ns
$t_{SR(O)}$	Output Slew Rate	Measured from 20% to 80% of V_{DD} = 3.3V, 15 pF Load	0.8	–	4.0	V/ns
		Measured from 20% to 80% of V_{DD} =2.5V, 15 pF Load	0.4	–	3.0	V/ns
$t_{SK(O)}$	Output to Output Skew	All outputs equally loaded, measured at V_{DD}/2	–	110	200	ps
$t_{SK(IB)}$	Intrabank Skew	All outputs equally loaded, measured at V_{DD}/2	–	–	75	ps
$t_{SK(PP)}$	Part to Part Skew	Measured at V_{DD}/2	–	–	500	ps
$t_{(\phi)}$[7]	Static Phase Offset	Measured at V_{DD}/2	–	–	250	ps
$t_{D(\phi)}$[7]	Dynamic Phase Offset	Measured at V_{DD}/2	–	150	200	ps
$t_{J(CC)}$	Cycle-to-Cycle Jitter	Load = 15 pF, $f_{OUT} \geq$ 6.25 MHz	–	100	200	ps
			–	18	35	ps_{RMS}
t_{LOCK}	Lock Time	At room temperature with 18.432-MHz Crystal	–	70	–	ms

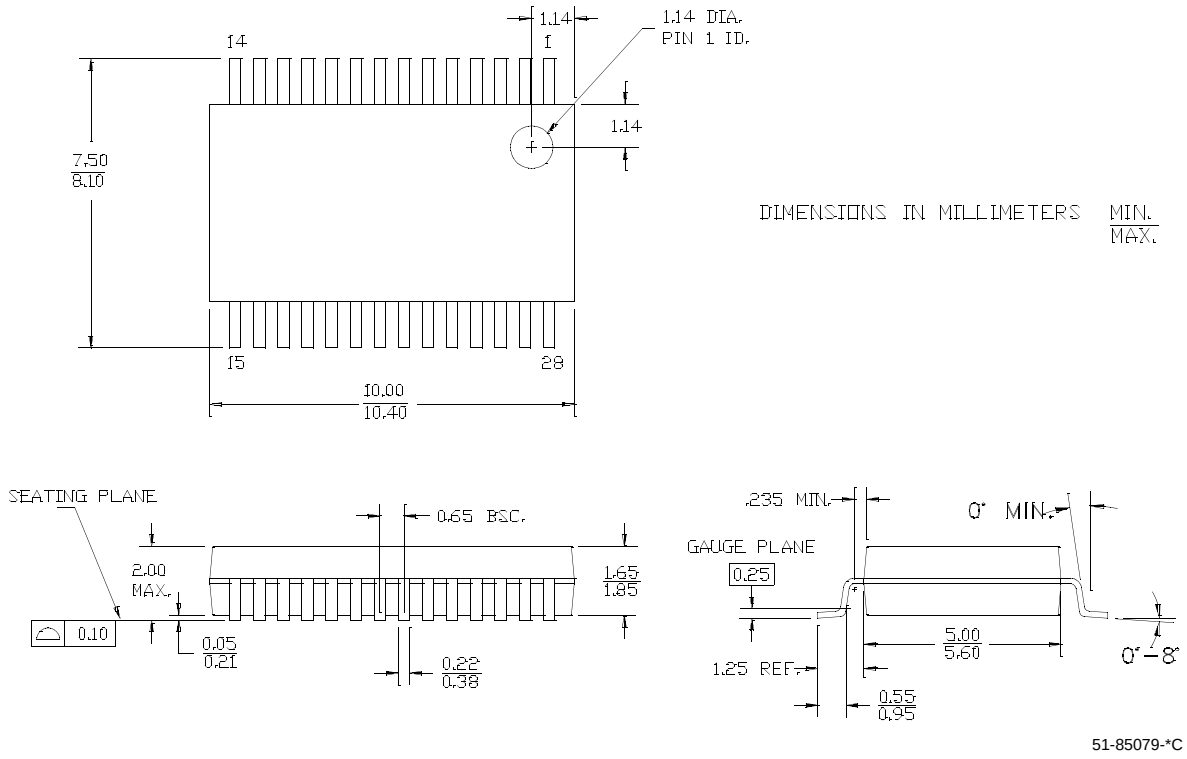
Ordering Information

Part Number	Package Type	Product Flow
CY23FS08OI	28-pin SSOP	Industrial, –40°C to 85°C
CY23FS08OIT	28-pin SSOP – Tape and Reel	Industrial, –40°C to 85°C
CY23FS08OC	28-pin SSOP	Commercial, 0°C to 70°C
CY23FS08OCT	28-pin SSOP – Tape and Reel	Commercial, 0°C to 70°C
Lead-free		
CY23FS08OXI	28-pin SSOP	Industrial, –40°C to 85°C
CY23FS08OXIT	28-pin SSOP – Tape and Reel	Industrial, –40°C to 85°C
CY23FS08OXC	28-pin SSOP	Commercial, 0°C to 70°C
CY23FS08OXCT	28-pin SSOP – Tape and Reel	Commercial, 0°C to 70°C

Notes:
7. The $t_{(\phi)}$ reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as $t_{SR(I)}$ is maintained.
8. Parameters guaranteed by design and characterization, not 100% tested in production.
9. Includes typical board trace capacitance of 6–7pF each XIN, XOUT.

Package Drawing and Dimensions

28-Lead (5.3 mm) Shrunk Small Outline Package O28



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Document History Page

Document Title: CY23FS08 Failsafe™ 2.5V/ 3.3V Zero Delay Buffer Document #: 38-07518 Rev. *C				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	123699	04/23/03	RGL	New Data Sheet
*A	224067	See ECN	RGL/ZJX	Changed the XTAL Specifications table.
*B	276749	See ECN	RGL	Removed (T_{LOCK}) Lock Time Specification.
*C	417645	See ECN	RGL	Added Lead-free devices Added typical nos. on jitters