

# XMC4400

Microcontroller Series  
for Industrial Applications

XMC4000 Family

ARM<sup>®</sup> Cortex<sup>™</sup>-M4  
32-bit processor core

Data Sheet

V0.6 2012-11

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**PRELIMINARY**

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**XMC4400 Data Sheet**

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## About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4400 series devices.

The document describes the characteristics of a superset of the XMC4400 series devices. For simplicity, the various device types are referred to by the collective term XMC4400 throughout this manual.

### XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  - describes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

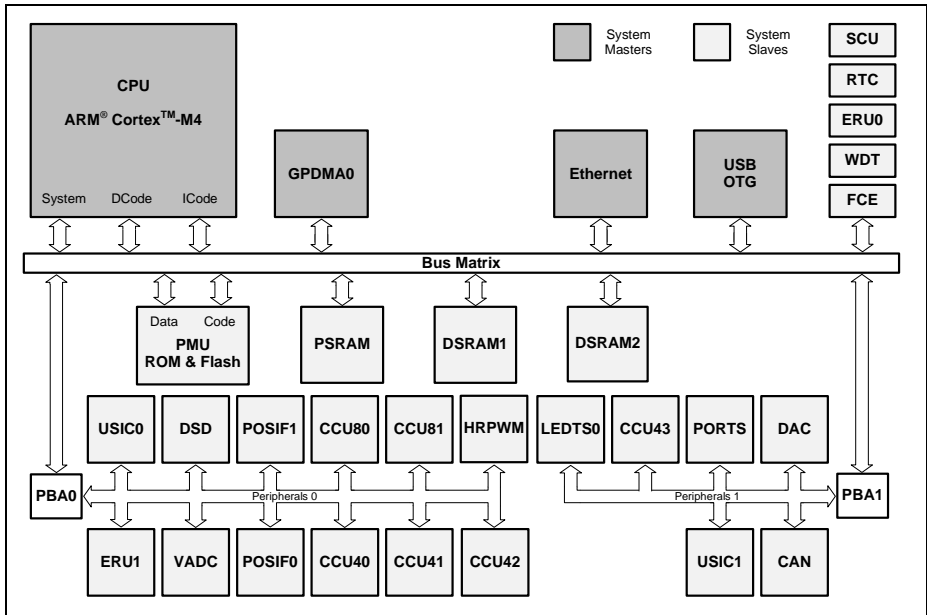
***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

# 1 Summary of Features

The XMC4400 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.



**Figure 1 System Block Diagram**

## CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- One General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection



**On-Chip Memories**

- 16 KB on-chip boot ROM
- 16 KB on-chip high-speed program memory
- 32 KB on-chip high speed data memory
- 32 KB on-chip high-speed communication memory
- 512 KB on-chip Flash Memory with 4 KB instruction cache

**Communication Peripherals**

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with two nodes, 64 message objects, data rate up to 1MBit/s
- Four Universal Serial Interface Channels (USIC), providing four serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface

**Analog Frontend Peripherals**

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analogue Converter (DAC) with two channels of 12-bit resolution

**Industrial Control Peripherals**

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Four High Resolution PWM (HRPWM) channels
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

**Input/Output Lines**

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

## On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC4<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4400 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4400 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC4400** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

**Table 1**      **Synopsis of XMC4400 Device Types**

Derivative <sup>1)</sup>	Package	Flash Kbytes	SRAM Kbytes
XMC4400-F100x512	PG-LQFP-100	512	80
XMC4400-F64x512	PG-LQFP-64	512	80
XMC4400-F100x256	PG-LQFP-100	256	80
XMC4400-F64x256	PG-LQFP-64	256	80
XMC4402-F100x256	PG-LQFP-100	256	80
XMC4402-F64x256	PG-LQFP-64	256	80

1) x is a placeholder for the supported temperature range.

### 1.3 Device Type Features

The following table lists the available features per device type.

**Table 2 Features of XMC4400 Device Types**

Derivative <sup>1)</sup>	LEDTS Intf.	ETH Intf.	USB Intf.	USIC Chan.	MultiCAN Nod./Msg.
XMC4400-F100x512	1	1	1	2 x 2	2 / 64
XMC4400-F64x512	1	1	1	2 x 2	2 / 64
XMC4400-F100x256	1	1	1	2 x 2	2 / 64
XMC4400-F64x256	1	1	1	2 x 2	2 / 64
XMC4402-F100x256	1	–	1	2 x 2	2 / 64
XMC4402-F64x256	1	–	1	2 x 2	2 / 64

1) x is a placeholder for the supported temperature range.

**Table 3 Features of XMC4400 Device Types**

Derivative <sup>1)</sup>	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.	HRPWM Intf.
XMC4400-F100x512	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x512	14	4	2	4 x 4	2 x 4	2	1
XMC4400-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4400-F64x256	14	4	2	4 x 4	2 x 4	2	1
XMC4402-F100x256	24	4	2	4 x 4	2 x 4	2	1
XMC4402-F64x256	14	4	2	4 x 4	2 x 4	2	1

1) x is a placeholder for the supported temperature range.

## 1.4 Definition of Feature Variants

The XMC4400 types are offered with several memory sizes and number of available VADC channels. [Table 4](#) describes the location of the available Flash memory, [Table 5](#) describes the location of the available SRAMs, [Table 6](#) the available VADC channels.

**Table 4 Flash Memory Ranges**

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	0800 0000 <sub>H</sub> – 0803 FFFF <sub>H</sub>	0C00 0000 <sub>H</sub> – 0C03 FFFF <sub>H</sub>
512 Kbytes	0800 0000 <sub>H</sub> – 0807 FFFF <sub>H</sub>	0C00 0000 <sub>H</sub> – 0C07 FFFF <sub>H</sub>

**Table 5 SRAM Memory Ranges**

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
80 Kbytes	1FFF C000 <sub>H</sub> – 1FFF FFFF <sub>H</sub>	2000 0000 <sub>H</sub> – 2000 7FFF <sub>H</sub>	2000 8000 <sub>H</sub> – 2000 FFFF <sub>H</sub>

**Table 6 AD Converter Channels<sup>1)</sup>**

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3
PG-LQFP-64	CH0, CH3..CH7	CH0, CH1, CH3, CH6	CH0, CH1	CH2, CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.5 Identification Registers

The identification registers allow software to identify the marking.

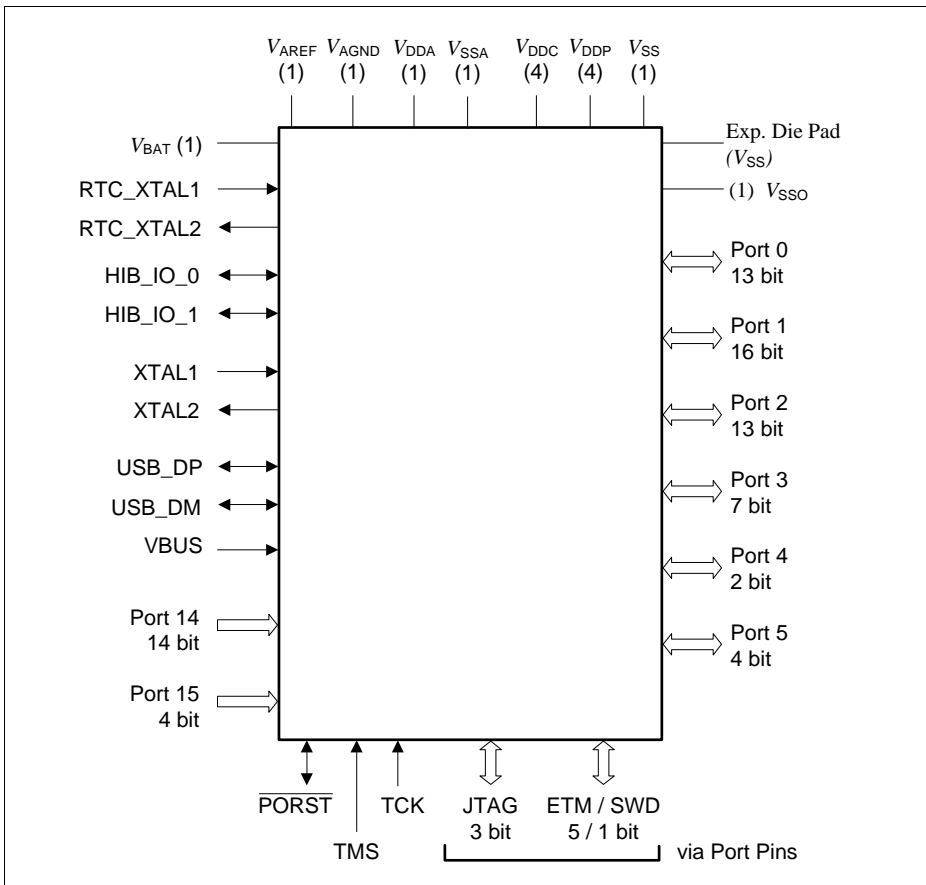
**Table 7 XMC4400 Identification Registers**

Register Name	Value	Marking
SCU_IDCHIP	0004 4001 <sub>H</sub>	EES
JTAG IDCODE	101D C083 <sub>H</sub>	EES

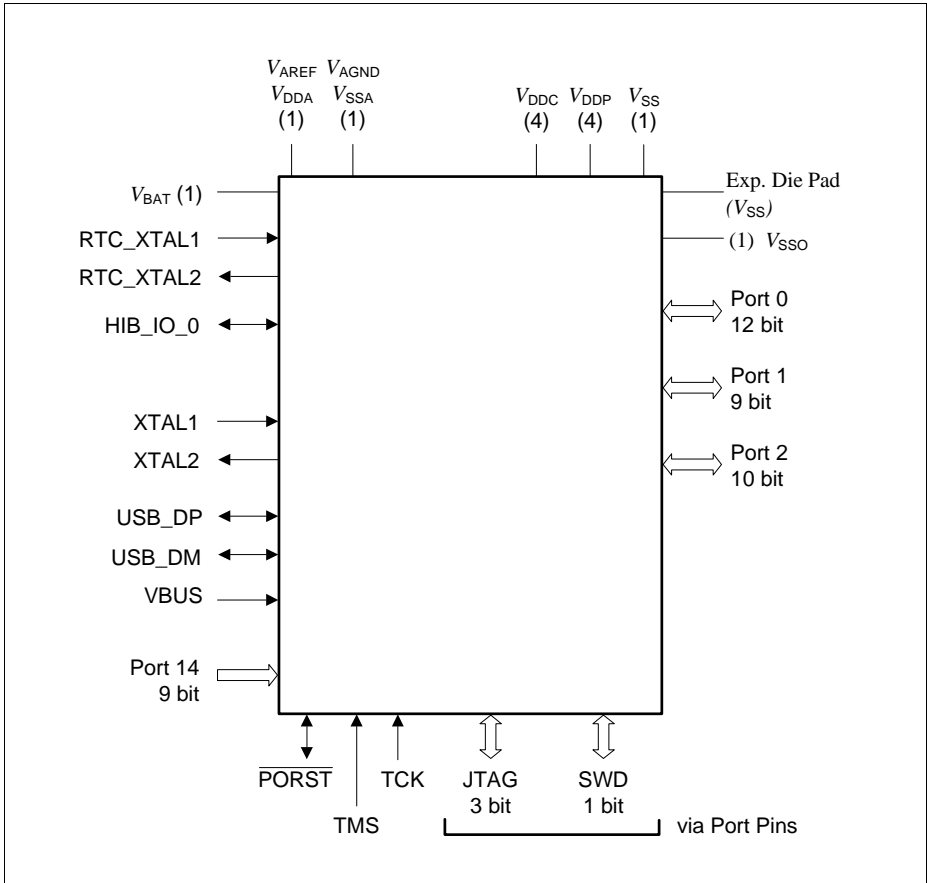
## 2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

### 2.1 Logic Symbols



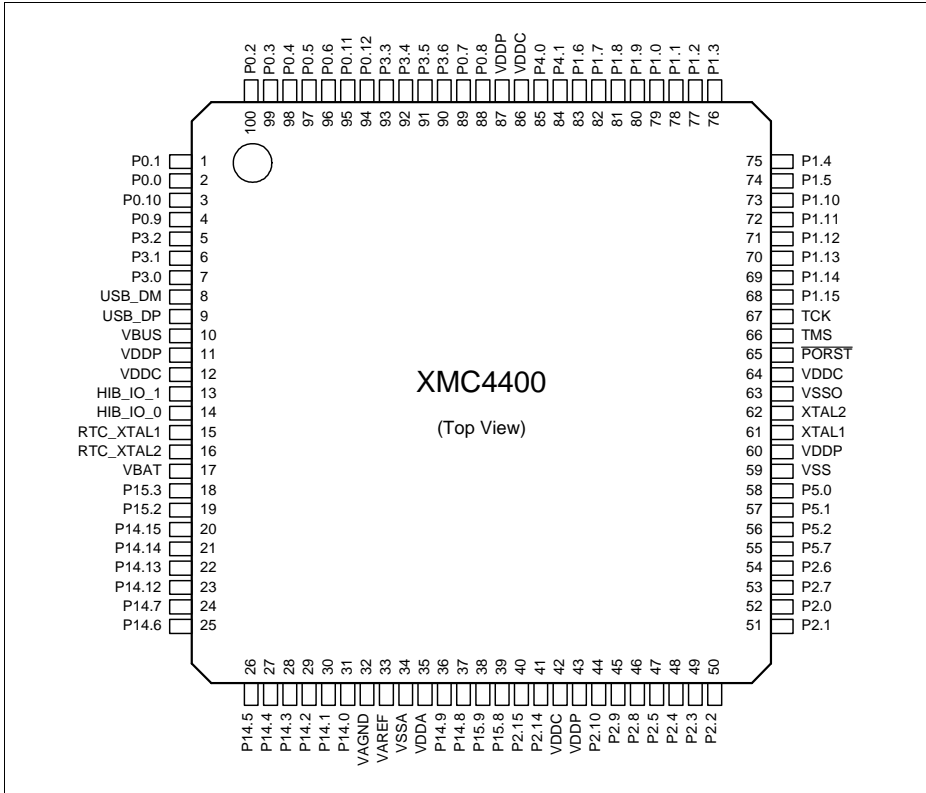
**Figure 2 XMC4400 Logic Symbol PG-LQFP-100**



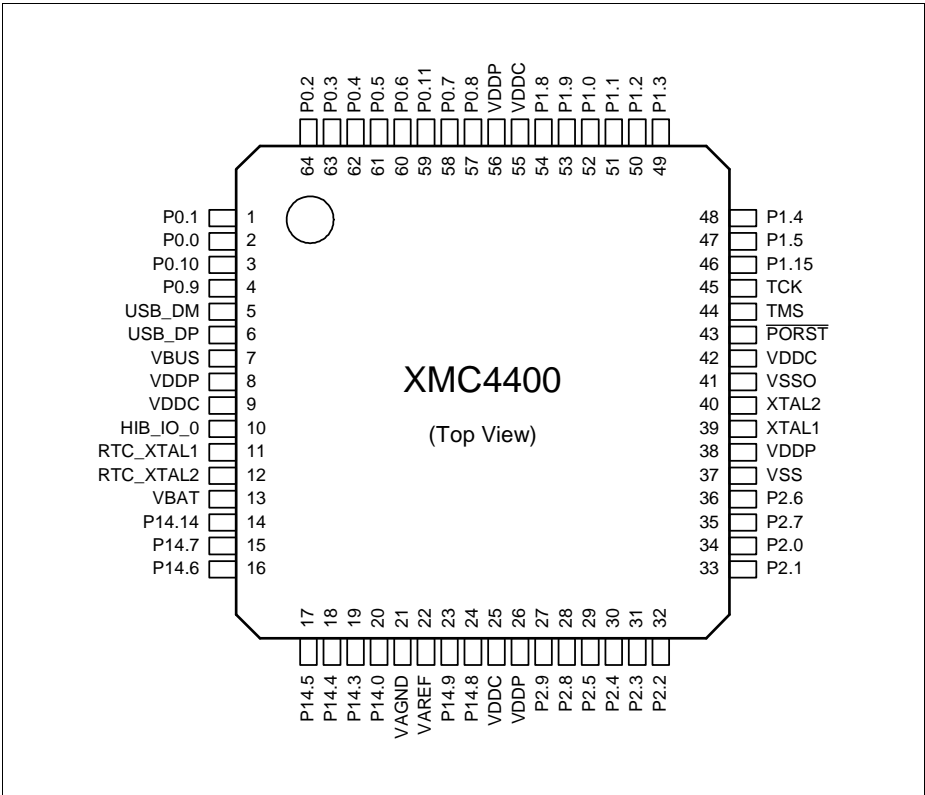
**Figure 3 XMC4400 Logic Symbol PG-LQFP-64**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.



**Figure 4 XMC4400 PG-LQFP-100 Pin Configuration (top view)**



**Figure 5 XMC4400 PG-LQFP-64 Pin Configuration (top view)**



## 2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

**Table 8 Package Pin Mapping Description**

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG\_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset.

**Table 9 Package Pin Mapping**

Function	LQFP-100	LQFP-64	Pad Type	Notes
P0.0	2	2	A1+	
P0.1	1	1	A1+	
P0.2	100	64	A2	
P0.3	99	63	A2	
P0.4	98	62	A2	
P0.5	97	61	A2	
P0.6	96	60	A2	
P0.7	89	58	A2	After a system reset, this pin selects HW0.
P0.8	88	57	A2	After a system reset, this pin selects HW0 with a weak pull-down active.
P0.9	4	4	A2	
P0.10	3	3	A1+	
P0.11	95	59	A1+	
P0.12	94	-	A1+	
P1.0	79	52	A1+	

**Table 9 Package Pin Mapping (cont'd)**

Function	LQFP-100	LQFP-64	Pad Type	Notes
P1.1	78	51	A1+	
P1.2	77	50	A2	
P1.3	76	49	A2	
P1.4	75	48	A1+	
P1.5	74	47	A1+	
P1.6	83	-	A2	
P1.7	82	-	A2	
P1.8	81	54	A2	
P1.9	80	53	A2	
P1.10	73	-	A1+	
P1.11	72	-	A1+	
P1.12	71	-	A2	
P1.13	70	-	A2	
P1.14	69	-	A2	
P1.15	68	46	A2	
P2.0	52	34	A2	
P2.1	51	33	A2	After a system reset, this pin selects HW0.
P2.2	50	32	A2	
P2.3	49	31	A2	
P2.4	48	30	A2	
P2.5	47	29	A2	
P2.6	54	36	A1+	
P2.7	53	35	A1+	
P2.8	46	28	A2	
P2.9	45	27	A2	
P2.10	44	-	A2	
P2.14	41	-	A2	
P2.15	40	-	A2	
P3.0	7	-	A2	
P3.1	6	-	A2	
P3.2	5	-	A2	
P3.3	93	-	A1+	

**Table 9 Package Pin Mapping (cont'd)**

Function	LQFP-100	LQFP-64	Pad Type	Notes
P3.4	92	-	A1+	
P3.5	91	-	A2	
P3.6	90	-	A2	
P4.0	85	-	A2	
P4.1	84	-	A2	
P5.0	58	-	A1+	
P5.1	57	-	A1+	
P5.2	56	-	A1+	
P5.7	55	-	A1+	
P14.0	31	20	AN/DIG_IN	
P14.1	30	-	AN/DIG_IN	
P14.2	29	-	AN/DIG_IN	
P14.3	28	19	AN/DIG_IN	
P14.4	27	18	AN/DIG_IN	
P14.5	26	17	AN/DIG_IN	
P14.6	25	16	AN/DIG_IN	
P14.7	24	15	AN/DIG_IN	
P14.8	37	24	AN/DAC/DIG_I N	
P14.9	36	23	AN/DAC/DIG_I N	
P14.12	23	-	AN/DIG_IN	
P14.13	22	-	AN/DIG_IN	
P14.14	21	14	AN/DIG_IN	
P14.15	20	-	AN/DIG_IN	
P15.2	19	-	AN/DIG_IN	
P15.3	18	-	AN/DIG_IN	
P15.8	39	-	AN/DIG_IN	
P15.9	38	-	AN/DIG_IN	
USB_DP	9	6	special	
USB_DM	8	5	special	

**Table 9 Package Pin Mapping (cont'd)**

Function	LQFP-100	LQFP-64	Pad Type	Notes
HIB_IO_0	14	10	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0".
HIB_IO_1	13	-	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active.
TCK	67	45	A1	Weak pull-down active.
TMS	66	44	A1+	Weak pull-up active.
PORST	65	43	special	Strong pull-down controlled by EVR. Weak pull-up active while strong pull-down is not active.
XTAL1	61	39	clock_IN	
XTAL2	62	40	clock_O	
RTC_XTAL1	15	11	clock_IN	
RTC_XTAL2	16	12	clock_O	
VBAT	17	13	Power	When $V_{DDP}$ is supplied $V_{BAT}$ has to be supplied as well.
VBUS	10	7	special	
VAREF	33	-	AN_Ref	
VAGND	32	-	AN_Ref	
VDDA	35	-	AN_Power	
VSSA	34	-	AN_Power	
VDDA/VAREF	-	22	AN_Power/AN_Ref	Shared analog supply and reference voltage pin.
VSSA/VAGND	-	21	AN_Power/AN_Ref	Shared analog supply and reference ground pin.
VDDC	12	9	Power	
VDDC	42	25	Power	
VDDC	64	42	Power	
VDDC	86	55	Power	
VDDP	11	8	Power	

**Table 9 Package Pin Mapping (cont'd)**

Function	LQFP-100	LQFP-64	Pad Type	Notes
VDDP	43	26	Power	
VDDP	60	38	Power	
VDDP	87	56	Power	
VSS	59	37	Power	
VSSO	63	41	Power	
VSS	Exp. Pad	Exp. Pad	Power	<p><b>Exposed Die Pad</b> The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</p>

### 2.2.2 Port I/O Functions

The following general scheme is used to describe each PORT pin:

**Table 10 Port I/O Function Description**

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn\_IN.y, Pn\_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn\_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn\_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

## 2.2.2.1 Port I/O Function Table

**Table 11 Port I/O Functions**

Function	Output					Input									
	ALT1	ALT2	ALT3	ALT4	HW00	HWI0	Input	Input	Input	Input	Input	Input	Input	Input	
P0.0		CAN. NO_TXD	CCU80. OUT21	LEDT50. COL2			U1C1. DX0D	ETH0. CLK_RMIIb	ERU0. 0B0			HRPWM0. C1INB		ETH0. CLKRXB	
P0.1	USB. DRIVEBUS	U1C1. DOU0	CCU80. OUT11	LEDT50. COL3				ETH0. CRS_DVB	ERU0. 0A0			HRPWM0. C2INB		ETH0. RXDVB	
P0.2		U1C1. SELO1	CCU80. OUT01	HRPWM0. HROUT01	U1C0. DOU03	U1C0. HWIN3	ETH0. RXDOB		ERU0. 3B3						
P0.3			CCU80. OUT20	HRPWM0. HROUT20	U1C0. DOU02	U1C0. HWIN2	ETH0. RXD1B			ERU1. 3B0					
P0.4	ETH0. TX_EN		CCU80. OUT10	HRPWM0. HROUT21	U1C0. DOU01	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3						
P0.5	ETH0. TXD0	U1C0. DOU0	CCU80. OUT00	HRPWM0. HROUT00	U1C0. DOU00	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0					
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30	HRPWM0. HROUT30				U1C0. DX2A	ERU0. 3B2			CCU80. IN2B			
P0.7	WWD0. SERVICE_OUT	U0C0. SELO0		HRPWM0. HROUT11		DB. TDI	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1			CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT		HRPWM0. HROUT10		DB. TRST	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1			CCU80. IN1B			
P0.9	HRPWM0. HROUT31	U1C1. SELO0	CCU80. OUT12	LEDT50. COL0	ETH0. MDO	ETH0. MDIA	U1C1. DX2A	USB. ID	ERU0. 1B0						
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDT50. COL1			U1C1. DX1A		ERU0. 1A0						
P0.11		U1C0. SCLKOUT	CCU80. OUT31				ETH0. RXERB	U1C0. DX1A	ERU0. 3A2						
P0.12		U1C1. SELO0	CCU40. OUT3					U1C1. DX2B	ERU0. 2B2						
P1.0	DSD. CGPWMN	U0C0. SELO0	CCU40. OUT3	ERU1. P0OUT3			U0C0. DX2A		ERU0. 3B0			CCU40. IN3A	HRPWM0. CO1NA		
P1.1	DSD. CGPWP	U0C0. SCLKOUT	CCU40. OUT2	ERU1. P0OUT2			U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0			CCU40. IN2A	HRPWM0. C1INA		
P1.2			CCU40. OUT1	ERU1. P0OUT1	U0C0. DOU03	U0C0. HWIN3		POSIF0. IN1A		ERU1. 2B0		CCU40. IN1A	HRPWM0. C2INA		
P1.3		U0C0. MCLKOUT	CCU40. OUT0	ERU1. P0OUT0	U0C0. DOU02	U0C0. HWIN2		POSIF0. IN0A		ERU1. 2A0		CCU40. IN0A	HRPWM0. CO1NB		
P1.4	WWD0. SERVICE_OUT	CAN. NO_TXD	CCU80. OUT33	CCU81. OUT20	U0C0. DOU01	U0C0. HWIN1	U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0			CCU41. IN0C	HRPWM0. BL0A		
P1.5	CAN. N1_TXD	U0C0. DOU0	CCU80. OUT23	CCU81. OUT10	U0C0. DOU00	U0C0. HWIN0	U0C0. DX0A	CAN. NO_RXDA	ERU0. 2A0	ERU1. 0A0		CCU41. IN1C	DSD. DIN2B		

**Table 11 Port I/O Functions (cont'd)**

Function	Output					Input									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input	
P1.6		U0C0. SCLKOUT					DSD. DIN2A								
P1.7		U0C0. DOUT0	DSD. MCLK2	U1C1. SELO2				DSD. MCLK2A			DSD. MCLK0C				
P1.8		U0C0. SELO1	DSD. MCLK1	U1C1. SCLKOUT				DSD. MCLK1A			DSD. MCLK0D	DSD. MCLK2D	DSD. MCLK3D		
P1.9	U0C0. SCLKOUT		DSD. MCLK0	U1C1. DOUT0				DSD. MCLK0A			DSD. MCLK1C	DSD. MCLK2C	DSD. MCLK3C		
P1.10	ETH0. MDC	U0C0. SCLKOUT	CCU81. OUT21								CCU41. IN2C				
P1.11		U0C0. SELO0	CCU81. OUT11		ETH0. MDO	ETH0. MDIC					CCU41. IN3C				
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01												
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81. OUT20				CAN. N1_RXDC								
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81. OUT10												
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00	U1C0. DOUT0	DB. ETM_TRACED ATA3			DSD. MCLK2B			ERU1. 1A0				
P2.0	CAN. N0_TXD	CCU81. OUT21	DSD. GCPWMN	LEDTS0. COL1	ETH0. MDO	ETH0. MDIB				ERU0. 0B3		CCU40. IN1C			
P2.1		CCU81. OUT11	DSD. GCPWMP	LEDTS0. COL0	DB.TDQ/ TRACESWO		ETH0. CLK_RMIIA			ERU1. 0B0		CCU40. IN0C		ETH0. CLKRXA	
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2			CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A		CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A	ETH0. RXKERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A		CCU41. IN1A	HRPWM0. BL1A		
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A	ETH0. CRS_DVA	U0C1. DX0B	ERU0. 0A2	POSIF1. IN0A		CCU41. IN0A	HRPWM0. BL2A	ETH0. CRS_DVA	
P2.6			CCU80. OUT13	LEDTS0. COL3			DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3			CCU40. IN3C			
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2			DSD. DIN0B		ERU1. 1B0			CCU40. IN2C			
P2.8	ETH0. TXD0		CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5					CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1		CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4					CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.10	VADC. EMUX10														
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21		DB. ETM_TRACEC LK			U1C0. DX0D				CCU43. IN0B	CCU43. IN1B	CCU43. IN2B	CCU43. IN3B



**Table 11 Port I/O Functions (cont'd)**

Function	Output					Input									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input	
P2.15	VADC. EMLUX12		CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDE06	LEDTS0. TSIN6A	ETH0. COLA	U1C0. DX0C				CCU42. IN0B	CCU42. IN1B	CCU42. IN2B	CCU42. IN3B
P3.0		U0C1. SCLKOUT	CCU42. OUT0				U0C1. DX1B					CCU80. IN2C	CCU81. IN0C		
P3.1		U0C1. SELO0					U0C1. DX2B		ERU0. 0B1			CCU80. IN1C			
P3.2	USB. DRIVEVBUS	CAN. NO_TXD		LEDTS0. COLA					ERU0. 0A1			CCU80. IN0C			
P3.3		U1C1. SELO1	CCU42. OUT3					DSD. DIN3B				CCU42. IN3A	CCU80. IN3B		
P3.4		U1C1. SELO2	CCU42. OUT2	DSD. MCLK3				DSD. MCLK3B				CCU42. IN2A	CCU80. IN0B		
P3.5		U1C1. SELO3	CCU42. OUT1	U0C1. DOUT0					ERU0. 3B1			CCU42. IN1A			
P3.6		U1C1. SELO4	CCU42. OUT0	U0C1. SCLKOUT	DB. ETM_TRACED ATA0				ERU0. 3A1			CCU42. IN0A			
P4.0			DSD. MCLK1		DB. ETM_TRACED ATA1		U1C1. DX1C	DSD. MCLK1B	U0C1. DX0E						
P4.1		U1C1. MCLKOUT	DSD. MCLK0	U0C1. SELO0	DB. ETM_TRACED ATA2			DSD. MCLK0B				DSD. MCLK1D			
P5.0		DSD. GGPWMN	CCU81. OUT33					ETH0. RXD0D	U0C0. DX0D			CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. GGPWMP	CCU81. OUT32					ETH0. RXD1D				CCU81. IN0B			
P5.2			CCU81. OUT23					ETH0. GRS_DVD				CCU81. IN1B			ETH0. RXD1D
P5.7			CCU81. OUT02	LEDTS0. COLA											
P14.0							VADC. G0CH0								
P14.1							VADC. G0CH1								
P14.2							VADC. G0CH2	VADC. G1CH2							
P14.3							VADC. G0CH3	VADC. G1CH3				CAN. NO_RXDB			
P14.4							VADC. G0CH4		VADC. G2CH0						
P14.5							VADC. G0CH5		VADC. G2CH1			POSIF0. IN2B			
P14.6							VADC. G0CH6					POSIF0. IN1B		G0ORC6	

**Table 11 Port I/O Functions (cont'd)**

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWI0	Input	Input	Input	Input	Input	Input	Input	Input
P14.7							VADC. G0CH7					POSIF0. IN0B		G0ORC7
P14.8					DAC. OUT_0			VADC. G1CH0		VADC. G3CH2		ETH0. RXD0C		
P14.9					DAC. OUT_1			VADC. G1CH1		VADC. G3CH3		ETH0. RXD1C		
P14.12								VADC. G1CH4						
P14.13								VADC. G1CH5						
P14.14								VADC. G1CH6					G1ORC6	
P14.15								VADC. G1CH7					G1ORC7	
P15.2									VADC. G2CH2					
P15.3									VADC. G2CH3					
P15.8										VADC. G3CH0		ETH0. CLK_RMIIC		ETH0. CLKRXC
P15.9										VADC. G3CH1		ETH0. GRS_DVC		ETH0. RXDVC
USB_DP														
USB_DM														
HIB_IO_0	HIBOUT	WWDI. SERVICE_OUT						WAKEUPA						
HIB_IO_1	HIBOUT	WWDI. SERVICE_OUT						WAKEUPB						
TCK							DB.TCK/ SWCLK							
TMS					DB.TMS/ SWDIO									
PORST														
XTAL1							U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F				
XTAL2														
RTC_XTAL1									ERU0. 1B1					
RTC_XTAL2														

## **3 Electrical Parameters**

*Attention: All parameters in this chapter are preliminary target values and may change based on characterization results.*

### **3.1 General Parameters**

#### **3.1.1 Parameter Interpretation**

The parameters listed in this section partly represent the characteristics of the XMC4400 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column "Symbol":

- **CC**  
Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4400 and must be regarded for system design.
- **SR**  
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4400 is designed in.

### 3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 12 Absolute Maximum Rating Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	$T_{ST}$	SR	-65	–	150	°C	–
Junction temperature	$T_J$	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to $V_{SS}$	$V_{DDP}$	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to $V_{SS}$	$V_{IN}$	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to $V_{AGND}$	$V_{AIN}$ $V_{AREF}$	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	$I_{IN}$	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$\Sigma I_{IN}$	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	$\Sigma I_{IN}$	SR	-100	–	+100	mA	

1) The port groups are defined in [Table 14](#).

### 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 13** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ( $V_{DDP}$  or  $V_{DDA}$ )
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

**Table 13 Overload Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on analog port pins (P14)	$I_{OVA}$	SR	-3	–	3	mA	
Input current on any digital port pin during overload condition	$I_{OVD}$	SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition <sup>1)</sup>	$I_{OVG}$	SR	–	–	20	mA	$\sum  I_{OVx} $ , for all $I_{OVx} < 0$ mA
			–	–	20	mA	$\sum  I_{OVx} $ , for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	$I_{OVS}$	SR	–	–	80	mA	$\sum I_{OVG}$

1) The port groups are defined in **Table 14**.

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

**Table 14 Port Groups for Overload and Short-Circuit Current Sum Parameters**

Group	Pins
1	P0.[12:0], P3.[6:0]
2	P14.[15:0], P15.[9:2]
3	P2.[15:0], P5.[7:0]
4	P1.[15:0], P4.[1:0]

### 3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the [Section 3.2.1](#).

**Table 15 Pad Driver and Pad Classes Overview**

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTTL I/O, LVTTTL outputs	<b>A1</b> (e.g. GPIO)	6 MHz	100 pF	No
			<b>A1+</b> (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			<b>A2</b> (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

### 3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4400. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

**Table 16 Operating Conditions Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	$T_A$ SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	$V_{DDP}$ SR	3.13 <sup>1)</sup>	3.3	3.63 <sup>2)</sup>	V	
Core Supply Voltage	$V_{DDC}$ CC	– <sup>1)</sup>	1.3	–	V	Generated internally
Digital ground voltage	$V_{SS}$ SR	0	–	–	V	
ADC analog supply voltage	$V_{DDA}$ SR	3.0	3.3	3.6 <sup>2)</sup>	V	
Analog ground voltage for $V_{DDA}$	$V_{SSA}$ SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain <sup>3)</sup>	$V_{BAT}$ SR	1.95	–	3.6	V	When $V_{DDP}$ is supplied $V_{BAT}$ has to be supplied as well.
System Frequency	$f_{SYS}$ SR	–	–	120	MHz	
Short circuit current of digital outputs	$I_{SC}$ SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group <sup>4)</sup>	$\Sigma I_{SC\_PG}$ SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	$\Sigma I_{SC\_D}$ SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, [Section 3.3.2](#).

2) Voltage overshoot to 4.0 V is permissible at Power-Up and  $\overline{PORST}$  low, provided the pulse duration is less than 100  $\mu$ s and the cumulated sum of the pulses does not exceed 1 h over lifetime.

3) Different limits apply for LPAC operation, [Section 3.2.6](#)

4) The port groups are defined in [Table 14](#).

## 3.2 DC Parameters

### 3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

**Table 17 Standard\_Pads Parameters**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	$C_{IO}$ CC	–	10	pF	
Pull-down current	$ I_{PDL} $ CC	150	–	$\mu A$	<sup>1)</sup> $V_i \geq 0.6 \times V_{DDP}$
		–	10	$\mu A$	<sup>2)</sup> $V_i \leq 0.36 \times V_{DDP}$
Pull-Up current	$ I_{PUH} $ CC	–	10	$\mu A$	<sup>2)</sup> $V_i \geq 0.6 \times V_{DDP}$
		100	–	$\mu A$	<sup>1)</sup> $V_i \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes <sup>3)</sup>	$H_YSA$ CC	$0.1 \times V_{DDP}$	–	V	
PORST spike filter always blocked pulse duration	$t_{SF1}$ CC	–	10	ns	
PORST spike filter pass-through pulse duration	$t_{SF2}$ CC	100	–	ns	
PORST pull-down current	$t_{SF2}$ CC	13	–	mA	$V_i = 1 V$

- 1) Current required to override the pull device with the opposite logic level (“force current”).  
With active pull device, at load currents between force and keep current the input state is undefined.
- 2) Load current at which the pull device still maintains the valid logic level (“keep current”).  
With active pull device, at load currents between force and keep current the input state is undefined.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.



**Table 18 Standard\_Pads Class\_A1**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1}$ CC	-500	500	nA	$0\text{ V} \leq V_i \leq V_{DDP}$
Input high voltage	$V_{IHA1}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1}$ SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD <sup>1)</sup> = weak	$V_{OHA1}$ CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\ \mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\ \mu\text{A}$
Output high voltage, POD <sup>1)</sup> = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\ \text{mA}$
		2.4	–	V	$I_{OH} \geq -2\ \text{mA}$
Output low voltage	$V_{OLA1}$ CC	–	0.4	V	$I_{OL} \leq 500\ \mu\text{A}$ ; POD <sup>1)</sup> = weak
		–	0.4	V	$I_{OL} \leq 2\ \text{mA}$ ; POD <sup>1)</sup> = medium
Fall time	$t_{FA1}$ CC	–	150	ns	$C_L = 20\ \text{pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\ \text{pF}$ ; POD <sup>1)</sup> = medium
Rise time	$t_{RA1}$ CC	–	150	ns	$C_L = 20\ \text{pF}$ ; POD <sup>1)</sup> = weak
		–	50	ns	$C_L = 50\ \text{pF}$ ; POD <sup>1)</sup> = medium

1) POD = Pin Out Driver

**Table 19 Standard\_Pads Class\_A1+**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	$I_{OZA1+}$ CC	-1	1	$\mu\text{A}$	$0\text{ V} \leq V_i \leq V_{DDP}$
Input high voltage	$V_{IHA1+}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA1+}$ SR	-0.3	$0.36 \times V_{DDP}$	V	

**Table 19 Standard\_Pads Class\_A1+ (cont'd)**

Parameter	Symbol	Values		Unit	Note / Test Condition	
		Min.	Max.			
Output high voltage, POD <sup>1)</sup> = weak	$V_{OHA1+}$ CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400 \mu A$	
		2.4	–	V	$I_{OH} \geq -500 \mu A$	
Output high voltage, POD <sup>1)</sup> = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4 mA$	
		2.4	–	V	$I_{OH} \geq -2 mA$	
Output high voltage, POD <sup>1)</sup> = strong		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4 mA$	
		2.4	–	V	$I_{OH} \geq -2 mA$	
Output low voltage		$V_{OLA1+}$ CC	–	0.4	V	$I_{OL} \leq 500 \mu A$ ; POD <sup>1)</sup> = weak
			–	0.4	V	$I_{OL} \leq 2 mA$ ; POD <sup>1)</sup> = medium
	–		0.4	V	$I_{OL} \leq 2 mA$ ; POD <sup>1)</sup> = strong	
Fall time	$t_{FA1+}$ CC	–	150	ns	$C_L = 20 pF$ ; POD <sup>1)</sup> = weak	
		–	50	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = medium	
		–	28	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = strong; edge = slow	
		–	16	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = strong; edge = soft;	
Rise time	$t_{RA1+}$ CC	–	150	ns	$C_L = 20 pF$ ; POD <sup>1)</sup> = weak	
		–	50	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = medium	
		–	28	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = strong; edge = slow	
		–	16	ns	$C_L = 50 pF$ ; POD <sup>1)</sup> = strong; edge = soft	

1) POD = Pin Out Driver

**Table 20 Standard\_Pads Class\_A2**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input Leakage current	$I_{OZA2}$ CC	-6	6	$\mu\text{A}$	$0\text{ V} \leq V_i < 0.5 \cdot V_{DDP} - 1\text{ V};$ $0.5 \cdot V_{DDP} + 1\text{ V} < V_i \leq V_{DDP}$
		-3	3	$\mu\text{A}$	$0.5 \cdot V_{DDP} - 1\text{ V} < V_i < 0.5 \cdot V_{DDP} + 1\text{ V}$
Input high voltage	$V_{IHA2}$ SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{ILA2}$ SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD = weak	$V_{OHA2}$ CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\ \mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\ \mu\text{A}$
Output high voltage, POD = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\ \text{mA}$
		2.4	–	V	$I_{OH} \geq -2\ \text{mA}$
Output high voltage, POD = strong		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\ \text{mA}$
		2.4	–	V	$I_{OH} \geq -2\ \text{mA}$
Output low voltage, POD = weak	$V_{OLA2}$ CC	–	0.4	V	$I_{OL} \leq 500\ \mu\text{A}$
Output low voltage, POD = medium		–	0.4	V	$I_{OL} \leq 2\ \text{mA}$
Output low voltage, POD = strong		–	0.4	V	$I_{OL} \leq 2\ \text{mA}$

**Table 20 Standard\_Pads Class\_A2 (cont'd)**

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Fall time	$t_{FA2}$ CC	–	150	ns	$C_L = 20$ pF; POD = weak
		–	50	ns	$C_L = 50$ pF; POD = medium
		–	3.7	ns	$C_L = 50$ pF; POD = strong; edge = sharp
		–	7	ns	$C_L = 50$ pF; POD = strong; edge = medium
		–	16	ns	$C_L = 50$ pF; POD = strong; edge = soft
Rise time	$t_{RA2}$ CC	–	150	ns	$C_L = 20$ pF; POD = weak
		–	50	ns	$C_L = 50$ pF; POD = medium
		–	3.7	ns	$C_L = 50$ pF; POD = strong; edge = sharp
		–	7.0	ns	$C_L = 50$ pF; POD = strong; edge = medium
		–	16	ns	$C_L = 50$ pF; POD = strong; edge = soft

**3.2.2 Analog to Digital Converters (ADCx)**
**Table 21 ADC Parameters (Operating Conditions apply)**

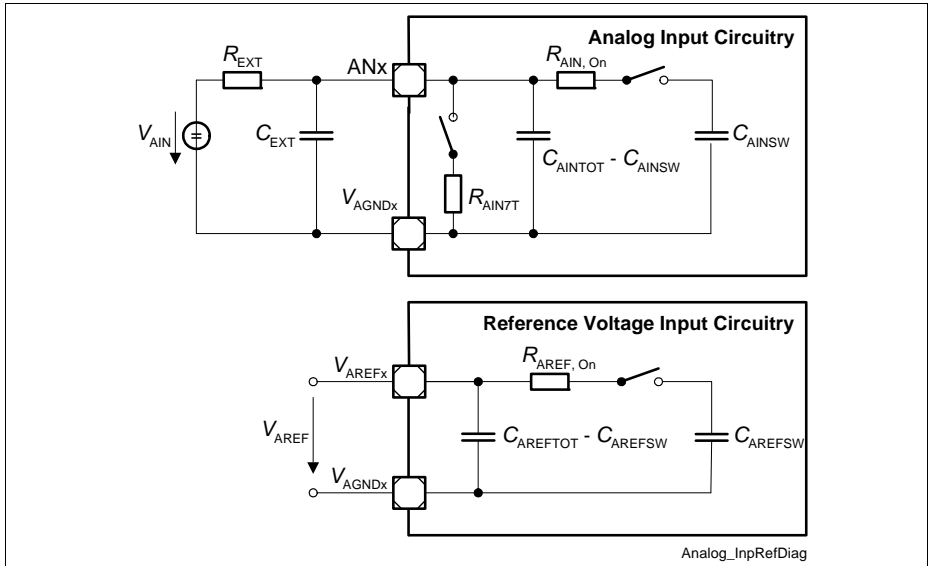
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage <sup>5)</sup>	$V_{AREF}$ SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05^{1)}$	V	
Analog reference ground <sup>5)</sup>	$V_{AGND}$ SR	$V_{SSM} - 0.05$	–	$V_{AREF} - 1$	V	
Analog reference voltage range <sup>2)5)</sup>	$V_{AREF} - V_{AGND}$ SR	1	–	$V_{DDA} + 0.1$	V	
Analog input voltage	$V_{AIN}$ SR	$V_{AGND}$	–	$V_{DDA}$	V	
Input leakage at analog inputs <sup>3)</sup>	$I_{OZ1}$ CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_i < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0 V \leq V_i \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_i \leq V_{DDA}$
Input leakage current at VAREF	$I_{OZ2}$ CC	-1	–	1	$\mu A$	$0 V \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	$I_{OZ3}$ CC	-1	–	1	$\mu A$	$0 V \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	$f_{ADCI}$ CC	2	–	30	MHz	$V_{DDA} = 3.3 V$
Switched capacitance at the analog voltage inputs <sup>4)</sup>	$C_{AINSW}$ CC	–	7	20	pF	
Total capacitance of an analog input	$C_{AINTOT}$ CC	–	25	30	pF	
Switched capacitance at the positive reference voltage input <sup>5)6)</sup>	$C_{AREFSW}$ CC	–	15	30	pF	
Total capacitance of the voltage reference inputs <sup>5)</sup>	$C_{AREFTOT}$ CC	–	20	40	pF	

**Table 21 ADC Parameters (Operating Conditions apply) (cont'd)**

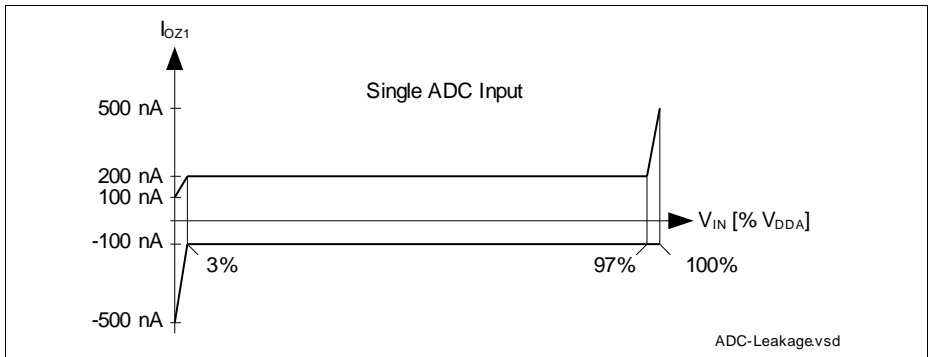
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	$TUE_{CC}$	-4	–	4	LSB	12-bit resolution;
Differential Non-Linearity Error <sup>8)</sup>	$EA_{DNL_{CC}}$	-3	–	3	LSB	$V_{DDA} = 3.3 V$ ; $V_{AREF} = V_{DDA}$ <sup>7)</sup>
Gain Error <sup>8)</sup>	$EA_{GAIN_{CC}}$	-4	–	4	LSB	
Integral Non-Linearity <sup>8)</sup>	$EA_{INL_{CC}}$	-3	–	3	LSB	
Offset Error <sup>8)</sup>	$EA_{OFF_{CC}}$	-4	–	4	LSB	
Worst case ADC $V_{DDA}$ power supply current per active converter	$I_{DDAA_{CC}}$	–	1.5	2	mA	during conversion $V_{DDP} = 3.6 V$ , $T_J = 150\text{ }^{\circ}C$
Charge consumption on $V_{AREF}$ per conversion <sup>5)</sup>	$Q_{CONV_{CC}}$	–	30	–	pC	$0 V \leq V_{AREF} \leq V_{DDA}$ <sup>9)</sup>
ON resistance of the analog input path	$R_{AIN_{CC}}$	–	700	1 700	Ohm	
ON resistance for the ADC test (pull down for AIN7)	$R_{AIN7T_{CC}}$	180	550	900	Ohm	
Resistance of the reference voltage input path	$R_{AREF_{CC}}$	–	700	1 700	Ohm	

- 1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
- 2) If the analog reference voltage is below  $V_{DDA}$ , then the ADC converter errors increase. If the reference voltage is reduced by the factor  $k$  ( $k < 1$ ), TUE, DNL, INL, Gain, and Offset errors increase also by the factor  $1/k$ .
- 3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see [Figure 7](#)).
- 4) The sampling capacity of the conversion C-network is pre-charged to  $V_{AREF}/2$  before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from  $V_{AREF}/2$ .
- 5) Applies to AINx, when used as alternate reference input.
- 6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
- 7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than  $\pm 1$  LSB.
- 8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
- 9) The resulting current for a conversion can be calculated with  $I_{AREF} = Q_{CONV} / t_c$ .  
The fastest 12-bit post-calibrated conversion of  $t_c = 550$  ns results in a typical average current of  $I_{AREF} = 54.5\text{ }\mu A$ .

The power-up calibration of the ADC requires a maximum number of  $4\ 352 f_{\text{ADCI}}$  cycles.



**Figure 6 ADCx Input Circuits**



**Figure 7 ADCx Analog Input Leakage Current**

**Conversion Time**

**Table 22 Conversion Time (Operating Conditions apply)**

Parameter	Symbol	Values	Unit	Note
Conversion time	$t_C$ CC	$2 \times T_{ADC} + (2 + N + STC + PC + DM) \times T_{ADCI}$	$\mu\text{S}$	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

**Conversion Time Examples**

System assumptions:

$f_{ADC} = 120 \text{ MHz}$  i.e.  $t_{ADC} = 8.33 \text{ ns}$ ,  $DIVA = 3$ ,  $f_{ADCI} = 30 \text{ MHz}$  i.e.  $t_{ADCI} = 33.3 \text{ ns}$

According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):

$$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 550 \text{ ns}$$

12-bit uncalibrated conversion:

$$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 483 \text{ ns}$$

10-bit uncalibrated conversion:

$$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 417 \text{ ns}$$

8-bit uncalibrated:

$$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 33.3 \text{ ns} + 2 \times 8.33 \text{ ns} = 350 \text{ ns}$$



**3.2.3 Digital to Analog Converters (DACx)**

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23 DAC Parameters (Operating Conditions apply)**

Parameter	Symbol	CC	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
RMS supply current	$I_{DD}$	CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	$RES$	CC	–	12	–	Bit	
Update rate	$f_{URATE\_A}$	CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to $\pm 1$ LSB accuracy
Update rate	$f_{URATE\_F}$	CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to $\pm 4$ LSB accuracy
Settling time	$t_{SETTLE}$	CC	–	1	2	$\mu$ s	at full scale jump, output voltage reaches target value $\pm 20$ LSB
Slew rate	$SR$	CC	2	5	–	V/ $\mu$ s	
Minimum output voltage	$V_{OUT\_MIN}$	CC	–	0.3	–	V	code value unsigned: 000 <sub>H</sub> ; signed: 800 <sub>H</sub>
Maximum output voltage	$V_{OUT\_MAX}$	CC	–	2.5	–	V	code value unsigned: FFF <sub>H</sub> ; signed: 7FF <sub>H</sub>
Integral non-linearity	$INL$	CC	-4	$\pm 2.5$	4	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	$DNL$	CC	-2	$\pm 1$	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

**Table 23 DAC Parameters (Operating Conditions apply) (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	$ED_{OFF}$ CC		±20		mV	
Gain error	$ED_{G\_IN}$ CC	-6.5	-1.5	3	%	
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	$f_{C1}$ CC	2.5	5	–	MHz	verified by design
Output sourcing current	$I_{OUT\_SOURCE}$ CC	–	-30	–	mA	
Output sinking current	$I_{OUT\_SINK}$ CC	–	0.6	–	mA	
Output resistance	$R_{OUT}$ CC	–	50	–	Ohm	
Load resistance	$R_L$ SR	5	–	–	kOhm	
Load capacitance	$C_L$ SR	–	–	50	pF	
Signal-to-Noise Ratio	SNR CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	THD CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	PSRR CC	–	56	–	dB	to $V_{DDA}$ verified by design

### Conversion Calculation

Unsigned:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN})$$

Signed:

$$DACxDATA = 4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN}) - 2048$$

### 3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages ( $V_{AIN}$ ) above the analog reference<sup>1)</sup> ( $V_{AREF}$ ) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

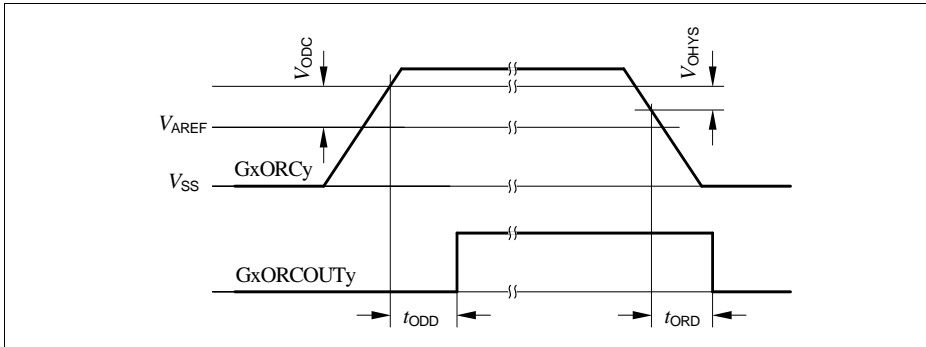
*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

The parameters in **Table 24** apply for the maximum reference voltage  $V_{AREF} = V_{DDA} + 50 \text{ mV}$ .

**Table 24 ORC Parameters** (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	$V_{ODC}$	CC	100	125	200	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	$V_{OHYS}$	CC	50	–	$V_{ODC}$	mV	
Detection Delay of a persistent Overvoltage	$t_{ODD}$	CC	55	–	450	ns	$V_{AIN} \geq V_{AREF} + 200 \text{ mV}$
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Always detected Overvoltage Pulse	$t_{OPDD}$	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 200 \text{ mV}$
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Never detected Overvoltage Pulse	$t_{OPDN}$	CC	–	–	49	ns	$V_{AIN} \geq V_{AREF} + 200 \text{ mV}$
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400 \text{ mV}$
Release Delay	$t_{ORD}$	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	$t_{OED}$	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.



**Figure 8 GxORCOUTy Trigger Generation**

### 3.2.5 High Resolution PWM (HRPWM)

The following chapters describe the operating conditions, characteristics and timing requirements, for all the components inside the HRPWM module. Each description is given for just one sub unit, e.g., one CSG or one HRC.

All the timing information is related to the module clock,  $f_{hrpwm}$ .

#### 3.2.5.1 Clocks

##### CSG External Clock

It is possible to select an external source, that can be used as a clock for the slope generation, HRPWMx.ECLKy. This clock is synchronized internally with the module clock and therefore the external clock needs to meet the criterion described on [Table 25](#).

**Table 25 External clock operating conditions**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Frequency	$f_{eclk}$	SR	–	–	$f_{hrpwm}/4$	MHz	
ON time	$t_{oneclk}$	SR	$2T_{ccu}^{1)2)}$	–	–	ns	
OFF time	$t_{offeclk}$	SR	$2T_{ccu}^{1)2)}$	–	–	ns	Only the rising edge is used

1) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

2) 50% duty cycle is not obligatory

**HRPWM DAC Conversion Clock**

The DAC conversion clock, can be generated internally or it can be controlled via a HRPWM module pin.

**Table 26 External DAC conversion trigger operating conditions**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency	$f_{\text{etrq}}$ SR	–	–	30 <sup>2)</sup>	MHz	
ON time	$t_{\text{onetrq}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	
OFF time	$t_{\text{offetrq}}$ SR	$2T_{\text{ccu}}^{1)2)}$	–	–	ns	

1) 50% duty cycle is not obligatory

2) Only valid if the signal was not previously synchronized/generated with the fccu clock (or a synchronous clock)

**3.2.5.2 CMP and 10-bit DAC characteristics**

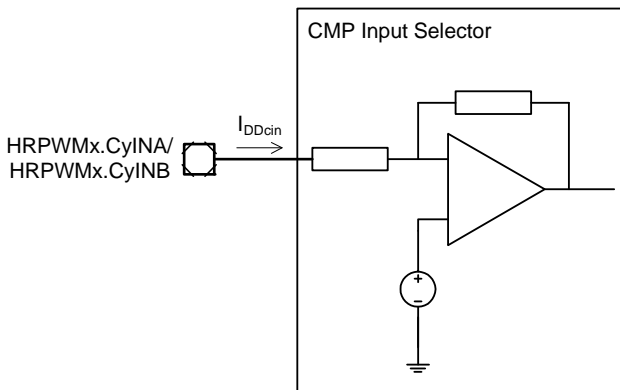
The [Table 27](#) summarizes the characteristics of the CSG unit.

**Table 27 CMP and 10-bit DAC characteristics (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAC Resolution	$RES_{CC}$		10		bits	
DAC differential nonlinearity	$DNL_{CC}$	tbd	–	± 1	LSB	
DAC integral nonlinearity	$INL_{CC}$	tbd	–	± 2	LSB	
CSG Gain Error	$E_G_{CC}$	–	–	±1.5	%	
CSG Offset Error	$V_{\text{OFFSET}_{CC}}$	–	–	±15	mV	
Bias startup time	$t_{\text{start}_{CC}}$	–	–	98	us	
Bias supply current	$I_{\text{DDbias}_{CC}}$	–	–	400	uA	
CSGy startup timer	$t_{\text{csgs}_{CC}}$	–	–	2	us	
Power down current	$I_{\text{DDpwd}_{CC}}$	–	–	400	nA	

**Table 27 CMP and 10-bit DAC characteristics** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input operation current	$I_{DDcin}$ CC	-10	–	+33	uA	See <a href="#">Figure 9</a>
High Speed Mode						
DAC propagation delay - Full scale	$t_{fshs}$ CC	tbd	tbd	80	ns	
Input Selector propagation delay - Full scale	$t_{ishs}$ CC	tbd	tbd	90	ns	
Propagation Delay - LSB	$t_{dly}$ CC	tbd	tbd	20	ns	
DAC CLK frequency	$f_{clk}$ SR	tbd	–	30	MHz	
Supply current	$I_{DDIs}$ CC	–	–	940	uA	
Low Speed Mode						
DAC propagation delay - Full Scale	$t_{OSIs}$ CC	tbd	tbd	tbd	ns	
Input Selector propagation delay - Full Scale	$t_{DHS}$ CC	tbd	tbd	tbd	ns	
Propagation delay - LSB	$t_{DLS}$ CC	tbd	tbd	200	ns	
Supply current	$I_{DDhs}$ CC	–	–	300	uA	



**Figure 9 Input operation current**

### 3.2.5.3 HRC characteristics

**Table 28** summarizes the characteristics of one HRC unit.

**Table 28 HRC characteristics** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HRC frequency	$f_{\text{HRC}}$ SR	64	–	–	MHz	$f_{\text{HRC}} = f_{\text{hrpwm}}$
High resolution step size <sup>1)2)</sup>	$t_{\text{HRS}}$ CC	tbd	150	tbd	ps	
Startup time (after reset release)	$t_{\text{start}}$ CC	–	–	2	us	

1) The step size for clock frequencies equal to 120 and 80 MHz is 150 ps.

2) The step size for clock frequencies different from 120 and 80 MHz but within the range from 120 to 64 MHz can be between 118 to 180 ps (fixed over process and operating conditions)

### 3.2.6 Low Power Analog Comparator (LPAC)

The Low Power Analog Comparator (LPAC) triggers a wake-up event from Hibernate state or an interrupt trigger during normal operation. It does so by comparing  $V_{\text{BAT}}$  or another external sensor voltage  $V_{\text{LPS}}$  with a pre-programmed threshold voltage.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 29 Low Power Analog Comparator Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$V_{\text{BAT}}$ supply voltage range for LPAC operation	$V_{\text{BAT}}$ SR	2.1	–	3.6	V	
Sensor voltage range	$V_{\text{LPCS}}$ CC	0	–	1.2	V	
Threshold step size	$V_{\text{th}}$ CC	–	18.75	–	mV	
Threshold trigger accuracy	$\Delta V_{\text{th}}$ CC	–	–	±10	%	for $V_{\text{th}} > 0.4 \text{ V}$
Conversion time	$t_{\text{LPCC}}$ CC	–	–	250	μs	
Power down current consumption	$I_{\text{LPCCPD}}$ CC	–	–	1	μA	LPAC off

**Table 29 Low Power Analog Comparator Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Average current consumption over time	$I_{LPCAC}$ CC	–	–	15	μA	for a conversion interval of 10 ms
Current consumption during conversion	$I_{LPCC}$ CC	–	150	–	μA	

### 3.2.7 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature  $T_J$ .

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 30 Die Temperature Sensor Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature sensor range	$T_{SR}$ SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	$\Delta T_{LE}$ CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	$\Delta T_{OE}$ CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$
Measurement time	$t_M$ CC	–	–	100	μs	
Start-up time after reset inactive	$t_{TSST}$ SR	–	–	10	μs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 596) / 2.03 \text{ [°C]} \quad (\text{PRELIMINARY})$$

This formula and the values defined in [Table 30](#) apply with the following calibration values:

- DTSCON.BGTRIM =  $\delta_H$  (PRELIMINARY)
- DTSCON.REFTRIM =  $4_H$  (PRELIMINARY)



### 3.2.8 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 31 USB OTG VBUS and ID Parameters (Operating Conditions apply)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	$V_{IN}$ CC	0.0	–	5.25	V	
A-device VBUS valid threshold	$V_{B1}$ CC	4.4	–	–	V	
A-device session valid threshold	$V_{B2}$ CC	0.8	–	2.0	V	
B-device session valid threshold	$V_{B3}$ CC	0.8	–	4.0	V	
B-device session end threshold	$V_{B4}$ CC	0.2	–	0.8	V	
VBUS input resistance to ground	$R_{VBUS\_IN}$ CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	$R_{VBUS\_PU}$ CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	$R_{VBUS\_PD}$ CC	656	–	–	Ohm	
USB.ID pull-up resistor	$R_{UID\_PU}$ CC	14	–	25	kOhm	
VBUS input current	$I_{VBUS\_IN}$ CC	–	–	150	$\mu$ A	$0\text{ V} \leq V_{IN} \leq 5.25\text{ V}$ : $T_{AVG} = 1\text{ ms}$

**Table 32 USB OTG Data Line (USB\_DP, USB\_DN) Parameters** (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage	$V_{IL}$ SR	–	–	0.8	V	
Input high voltage (driven)	$V_{IH}$ SR	2.0	–	–	V	
Input high voltage (floating) <sup>1)</sup>	$V_{IHZ}$ SR	2.7	–	3.6	V	
Differential input sensitivity	$V_{DIS}$ CC	0.2	–	–	V	
Differential common mode range	$V_{CM}$ CC	0.8	–	2.5	V	
Output low voltage	$V_{OL}$ CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	$V_{OH}$ CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	$R_{PUI}$ CC	900	–	1 575	Ohm	
DN pull-up resistor (upstream port receiving)	$R_{PUA}$ CC	1 425	–	3 090	Ohm	
DP, DN pull-down resistor	$R_{PD}$ CC	14.25	–	24.8	kOhm	
Input impedance DP, DN	$Z_{INP}$ CC	300	–	–	kOhm	$0 V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DN	$Z_{DRV}$ CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm  $\pm$  5% to 3.3 V  $\pm$  0.3 V connected to USB\_DP or USB\_DN and at B-connector with 15 kOhm  $\pm$  5% to ground connected to USB\_DP and USB\_DN.

### 3.2.9 Oscillator Pins

*Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

**Table 33 OSC\_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{\text{OSC}}$ SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time <sup>1)2)</sup>	$t_{\text{OSCS}}$ CC	–	–	10	ms	
Input voltage at XTAL1	$V_{\text{IX}}$ SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	
Input amplitude (peak-to-peak) at XTAL1 <sup>2)3)</sup>	$V_{\text{PPX}}$ SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	
Input high voltage at XTAL1 <sup>4)</sup>	$V_{\text{IHBX}}$ SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	
Input low voltage at XTAL1 <sup>4)</sup>	$V_{\text{ILBX}}$ SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	$I_{\text{ILX1}}$ CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

1)  $t_{\text{OSCS}}$  is defined from the moment the oscillator is enabled with SCU\_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of  $0.4 \times V_{\text{DDP}}$ .

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

**Table 34 RTC\_XTAL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	$f_{OSC}$ SR	–	32.768	–	kHz	
Oscillator start-up time <sup>1)2)3)</sup>	$t_{OSCS}$ CC	–	–	5	s	
Input voltage at RTC_XTAL1	$V_{IX}$ SR	-0.3	–	$V_{BAT} + 0.3$	V	
Input amplitude (peak-to-peak) at RTC_XTAL1 <sup>2)4)</sup>	$V_{PPX}$ CC	$0.2 \times V_{BAT}$	–	$V_{BAT} + 0.6$	V	
Input high voltage at RTC_XTAL1 <sup>5)</sup>	$V_{IHBX}$ SR	$0.6 \times V_{BAT}$	–	$V_{BAT} + 0.3$	V	
Input low voltage at RTC_XTAL1 <sup>5)</sup>	$V_{ILBX}$ SR	-0.3	–	$0.36 \times V_{BAT}$	V	
Input Hysteresis for RTC_XTAL1 <sup>5)6)</sup>	$V_{HYSX}$ CC	$0.1 \times V_{BAT}$		–	V	$3.0 \text{ V} \leq V_{BAT} < 3.6 \text{ V}$
		$0.03 \times V_{BAT}$		–	V	$V_{BAT} < 3.0 \text{ V}$
Input leakage current at RTC_XTAL1	$I_{ILX1}$ CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{IX} \leq V_{BAT}$

- 1)  $t_{OSCS}$  is defined from the moment the oscillator is enabled by the user with SCU\_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC\_XTAL1 of  $0.2 \times V_{BAT}$ .
- 2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
- 3) For a reliable start of the oscillation in crystal mode it is required that  $V_{BAT} \geq 3.0 \text{ V}$ . A running oscillation is maintained across the full  $V_{BAT}$  voltage range.
- 4) If the shaper unit is enabled and not bypassed.
- 5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.
- 6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

### 3.2.10 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

If not stated otherwise, the operating conditions for the parameters in the following table are:

$$V_{DDP} = 3.3 \text{ V}, T_A = 25 \text{ }^\circ\text{C}$$

**Table 35 Power Supply Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active supply current <sup>1)</sup> Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPA}$ CC	–	86	–	mA	120 / 120 / 120
		–	tbd	–		120 / 60 / 60
		–	tbd	–		60 / 60 / 120
		–	tbd	–		24 / 24 / 24
		–	tbd	–		1 / 1 / 1
Active supply current <sup>2)</sup> Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH}$ in MHz	$I_{DDPA}$ CC	–	80	–	mA	120 / 120 / 120
		–	tbd	–		120 / 60 / 60
		–	tbd	–		60 / 60 / 120
		–	tbd	–		24 / 24 / 24
		–	tbd	–		1 / 1 / 1
Sleep supply current <sup>3)</sup> Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPS}$ CC	–	tbd	–	mA	120 / 120 / 120
		–	tbd	–		120 / 60 / 60
		–	tbd	–		60 / 60 / 120
		–	tbd	–		24 / 24 / 24
		–	tbd	–		1 / 1 / 1
	$f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz	–	tbd	–		100 / 100 / 100

**Table 35 Power Supply Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current <sup>4)</sup> Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	$I_{DDPS}$ CC	–	tbd	–	mA	120 / 120 / 120
		–	tbd	–		120 / 60 / 60
		–	tbd	–		60 / 60 / 120
		–	tbd	–		24 / 24 / 24
		–	tbd	–		1 / 1 / 1
		–	tbd	–		100 / 100 / 100
Deep Sleep supply current <sup>5)</sup> Flash in Sleep mode Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz $f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz	$I_{DDPD}$ CC	–	tbd	–	mA	24 / 24 / 24
		–	tbd	–		4 / 4 / 4
		–	tbd	–		1 / 1 / 1
		–	tbd	–		100 / 100 / 100 <sup>6)</sup>
Hibernate supply current RTC on <sup>7)</sup>	$I_{DDPH}$ CC	–	tbd	–	$\mu$ A	$V_{BAT} = 3.3$ V
		–	tbd	–		$V_{BAT} = 2.4$ V
		–	tbd	–		$V_{BAT} = 2.0$ V
Hibernate supply current RTC off <sup>8)</sup>	$I_{DDPH}$ CC	–	tbd	–	$\mu$ A	$V_{BAT} = 3.3$ V
		–	tbd	–		$V_{BAT} = 2.4$ V
		–	tbd	–		$V_{BAT} = 2.0$ V
Hibernate off <sup>9)</sup>	$I_{DDPH}$ CC	–	tbd	–	$\mu$ A	$V_{BAT} = 3.3$ V
		–	tbd	–		$V_{BAT} = 2.4$ V
		–	tbd	–		$V_{BAT} = 2.0$ V
Worst case active supply current <sup>10)</sup>	$I_{DDPA}$ CC	–	–	tbd <sup>11)</sup>	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
$V_{DDA}$ power supply current	$I_{DDA}$ CC	–	–	– <sup>12)</sup>	mA	
$I_{DDP}$ current at PORST Low	$I_{DDP\_PORST}$ CC	–	–	tbd	mA	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
Power Dissipation	$P_{DISS}$ CC	–	–	tbd	W	$V_{DDP} = 3.6$ V, $T_J = 150$ °C
Wake-up time from Sleep to Active mode	$t_{SSA}$ CC	–	6	–	cycles	

**Table 35 Power Supply Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Wake-up time from Deep Sleep to Active mode		–	–	–	ms	Defined by the wake-up of the Flash module, see <a href="#">Section 3.2.11</a>
Wake-up time from Hibernate mode		–	–	–	ms	Wake-up via power-on reset event, see <a href="#">Section 3.3.2</a>

- 1) CPU executing code from Flash, all peripherals idle.
- 2) CPU executing code from Flash. Ethernet, USB and CCU clock off.
- 3) CPU in sleep, all peripherals idle, Flash in Active mode.
- 4) CPU in sleep, Flash in Active mode.
- 5) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
- 6) To wake-up the Flash from its Sleep mode,  $f_{CPU} \geq 1$  MHz is required.
- 7) OSC\_ULP operating with external crystal on RTC\_XTAL
- 8) OSC\_ULP off, Hibernate domain operating with OSC\_SI clock
- 9)  $V_{BAT}$  supplied, but Hibernate domain not started; for example state after factory assembly
- 10) Test Power Loop:  $f_{SYS} = 120$  MHz, CPU executing benchmark code from Flash, all CCUs in 100kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.  
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
- 11)  $I_{DDP}$  decreases typically by 25 mA when  $f_{SYS}$  decreases by 50 MHz, at constant  $T_J$
- 12) Sum of currents of all active converters (ADC and DAC)

**3.2.11 Flash Memory Parameters**

Note: These parameters are not subject to production test, but verified by design and/or characterization.

**Table 36 Flash Memory Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	$t_{ERP}$ CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	$t_{ERP}$ CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	$t_{ERP}$ CC	–	0.3	0.4	s	
Program time per page <sup>1)</sup>	$t_{PRP}$ CC	–	5.5	11	ms	
Erase suspend delay	$t_{FL\_ErSusp}$ CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	$\mu$ s	
Wake-up time	$t_{WU}$ CC	–	–	270	$\mu$ s	
Read access time	$t_a$ CC	20	–	–	ns	For operation with $1/f_{CPU} < t_a$ wait states must be configured <sup>2)</sup>
Data Retention Time, Physical Sector <sup>3)4)</sup>	$t_{RET}$ CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector <sup>3)4)</sup>	$t_{RETL}$ CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB) <sup>3)4)</sup>	$t_{RTU}$ CC	20	–	–	years	Max. 4 erase/program cycles per UCB

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.

2) The following formula applies to the wait state configuration:  $FCON.WSPFLASH \times (1/f_{CPU}) \geq t_a$ .

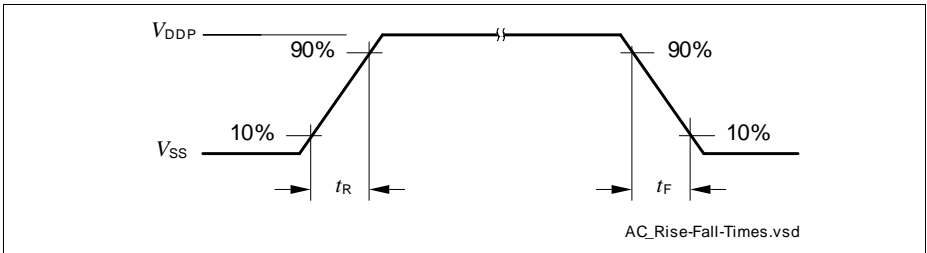
3) Storage and inactive time included.



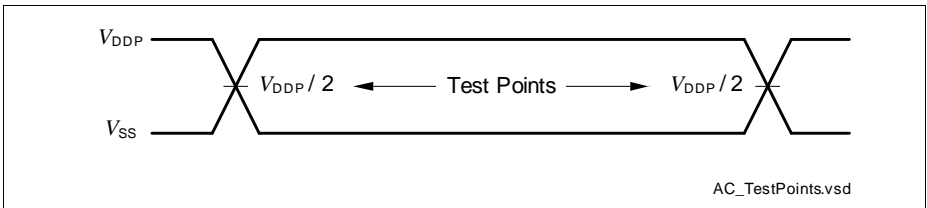
- 4) Values given are valid for an average weighted junction temperature of  $T_j = 110^\circ\text{C}$ . Further lifetime dependency values are give in the Quality Declarations.

### 3.3 AC Parameters

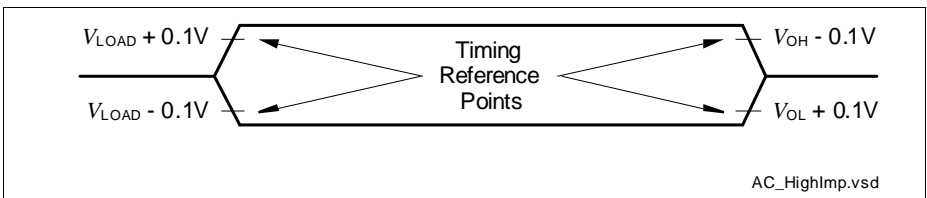
#### 3.3.1 Testing Waveforms



**Figure 10** Rise/Fall Time Parameters



**Figure 11** Testing Waveform, Output Delay



**Figure 12** Testing Waveform, Output High Impedance

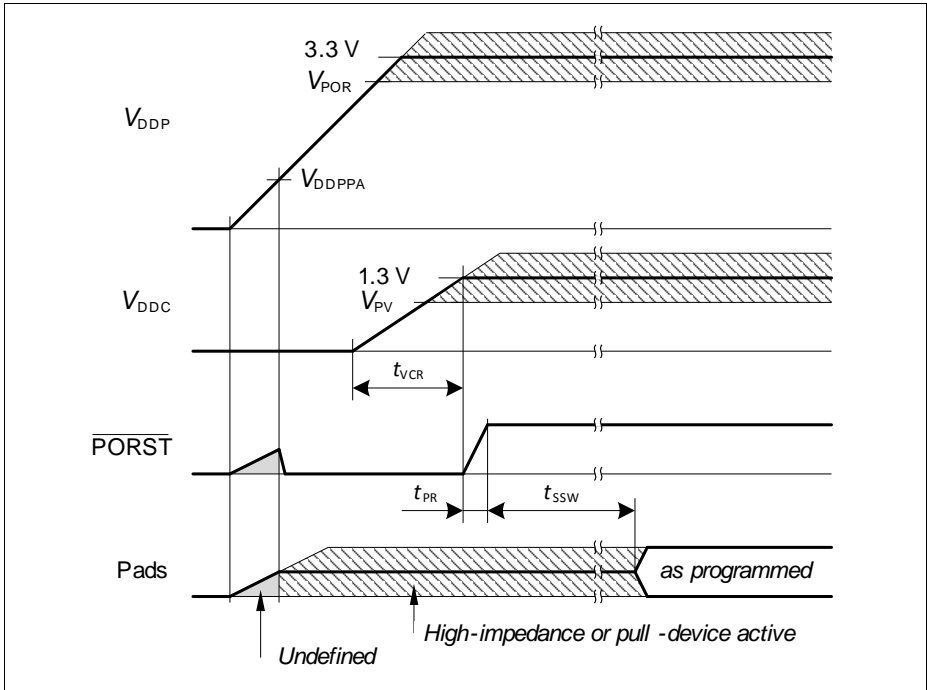
### 3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$  is always asserted when  $V_{\text{DDP}}$  and/or  $V_{\text{DDC}}$  violate the respective thresholds.

**Table 37 Supply Monitoring Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	$V_{\text{POR}}$ CC	2.79 <sup>1)</sup>	–	3.05 <sup>2)</sup>	V	<sup>3)</sup>
Core supply voltage reset threshold	$V_{\text{PV}}$ CC	–	–	1.17	V	
$V_{\text{DDP}}$ voltage to ensure defined pad states	$V_{\text{DDPPA}}$ CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	$t_{\text{PR}}$ SR	–	–	2	$\mu\text{s}$	
Startup time from power-on reset with code execution from Flash	$t_{\text{SSW}}$ CC	–	2.5	3.5	ms	Time to the first user code instruction
$V_{\text{DDC}}$ ramp up time	$t_{\text{VCR}}$ CC	–	550	–	$\mu\text{s}$	Ramp up after power-on or after a reset triggered by a violation of $V_{\text{POR}}$ or $V_{\text{PV}}$

- 1) Minimum threshold for reset assertion.
- 2) Maximum threshold for reset deassertion.
- 3) The  $V_{\text{DDP}}$  monitoring has a typical hysteresis of  $V_{\text{PORHYS}} = 180 \text{ mV}$ .



**Figure 13 Power-Up Behavior**

### 3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency  $f_{CPU}$ . Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 38 Power Sequencing Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	$\Delta I_{PLS}$ SR	-	-	50	mA	Load increase on $V_{DDP}$ $\Delta t \leq 10$ ns
Negative Load Step Current	$\Delta I_{NLS}$ SR	-	-	150	mA	Load decrease on $V_{DDP}$ $\Delta t \leq 10$ ns
$V_{DDC}$ Voltage Over- / Undershoot from Load Step	$\Delta V_{LS}$ CC	-	-	$\pm 100$	mV	For maximum positive or negative load step
Positive Load Step Settling Time	$t_{PLSS}$ SR	50	-	-	$\mu$ s	
Negative Load Step Settling Time	$t_{NLSS}$ SR	100	-	-	$\mu$ s	
External Buffer Capacitor on $V_{DDC}$	$C_{EXT}$ SR	-	10	-	$\mu$ F	In addition $C = 100$ nF capacitor on each $V_{DDC}$ pin

### Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$ , target frequency  $f_{CPU} = 120$  MHz, main PLL  $f_{VCO} = 480$  MHz, stepping done by K2 divider,  $t_{PLSS}$  between individual steps:

24 MHz - 48 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 10 - 7 - 5 - 4)

24 MHz - 68 MHz - 96 MHz - 120 MHz (K2 steps 20 - 7 - 5 - 4)

24 MHz - 68 MHz - 120 MHz (K2 steps 20 - 7 - 4)

### 3.3.4 Phase Locked Loop (PLL) Characteristics

#### Main and USB PLL

**Table 39 PLL Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	$D_P$ CC	–	–	±5	ns	accumulated over 300 cycles $f_{SYS} = 120$ MHz
Duty Cycle <sup>1)</sup>	$D_{DC}$ CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	$f_{REF}$ CC	4	–	16	MHz	
VCO frequency range	$f_{VCO}$ CC	260	–	520	MHz	
PLL lock-in time	$t_L$ CC	–	–	400	µs	

1) 50% for even K2 divider values,  $50 \pm (10/K2)$  for odd K2 divider values.

### 3.3.5 Internal Clock Source Characteristics

#### Fast Internal Clock Source

**Table 40 Fast Internal Clock Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{\text{OFINC}}$ CC	–	32.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	$\Delta f_{\text{OFI}}$ CC	-0.5	–	0.5	%	automatic calibration <sup>1)2)</sup>
		-20	–	20	%	forced calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-40	–	30	%	no calibration, $V_{\text{DDP}} = 3.3 \text{ V}$
		-10	–	10	%	$3.0 \text{ V} < V_{\text{DDP}} < 3.6 \text{ V}$
Start-up time	$t_{\text{OFIS}}$ CC	–	50	–	$\mu\text{s}$	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the  $V_{\text{DDP}}$  supply voltage.

Slow Internal Clock Source

**Table 41** Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	$f_{OSI}$ CC	–	32.768	–	kHz	
Accuracy	$\Delta f_{OSI}$ CC	-4	–	4	%	$V_{BAT} = \text{const.}$ $0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$V_{BAT} = \text{const.}$ $T_A < 0\text{ }^{\circ}\text{C}$ or $T_A > 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$2.4\text{ V} \leq V_{BAT}$ , $T_A = 25\text{ }^{\circ}\text{C}$
		-10	–	10	%	$1.95\text{ V} \leq V_{BAT} < 2.4\text{ V}$ , $T_A = 25\text{ }^{\circ}\text{C}$
Start-up time	$t_{OSIS}$ CC	–	50	–	$\mu\text{s}$	



### 3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

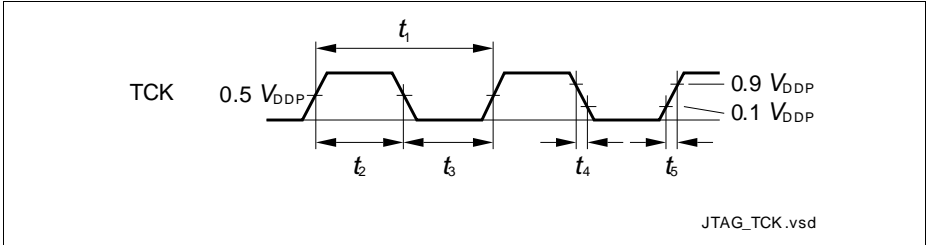
*Note: Operating conditions apply.*

**Table 42 JTAG Interface Timing Parameters**

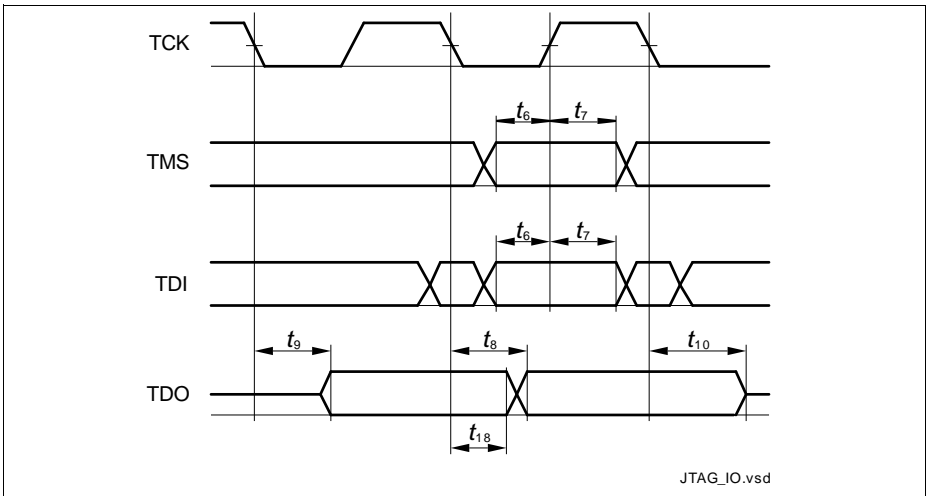
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	$t_1$ SR	25	–	–	ns	
TCK high time	$t_2$ SR	10	–	–	ns	
TCK low time	$t_3$ SR	10	–	–	ns	
TCK clock rise time	$t_4$ SR	–	–	4	ns	
TCK clock fall time	$t_5$ SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	$t_6$ SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	$t_7$ SR	6	–	–	ns	
TDO valid after TCK falling edge <sup>1)</sup> (propagation delay)	$t_8$ CC	–	–	13	ns	$C_L = 50$ pF
		3	–	–	ns	$C_L = 20$ pF
TDO hold after TCK falling edge <sup>1)</sup>	$t_{18}$ CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge <sup>1)2)</sup>	$t_9$ CC	–	–	14	ns	$C_L = 50$ pF
TDO valid to high imped. from TCK falling edge <sup>1)</sup>	$t_{10}$ CC	–	–	13.5	ns	$C_L = 50$ pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.



**Figure 14 Test Clock Timing (TCK)**



**Figure 15 JTAG Timing**

### 3.3.7 Serial Wire Debug Port (SW-DP) Timing

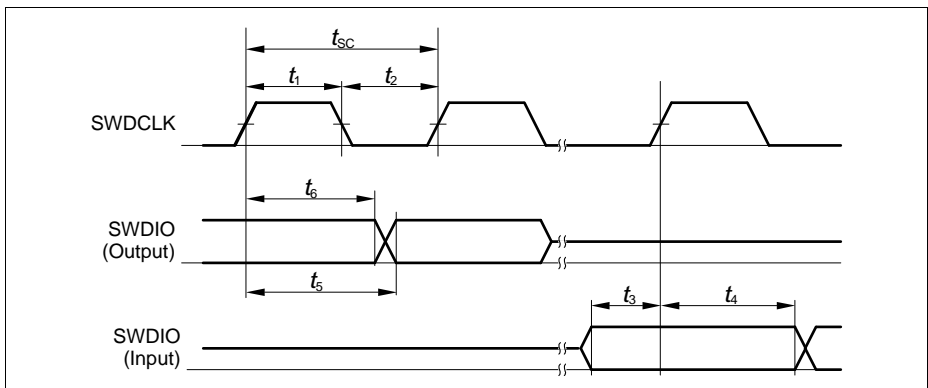
The following parameters are applicable for communication through the SW-DP interface.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

**Table 43 SWD Interface Timing Parameters (Operating Conditions apply)**

Parameter	Symbol	SR	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	$t_{SC}$	SR	25	–	–	ns	$C_L = 30$ pF
			40	–	–	ns	$C_L = 50$ pF
SWDCLK high time	$t_1$	SR	10	–	500000	ns	
SWDCLK low time	$t_2$	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	$t_3$	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	$t_4$	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	$t_5$	CC	–	–	17	ns	$C_L = 50$ pF
			–	–	13	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	$t_6$	CC	3	–	–	ns	



**Figure 16 SWD Timing**

**3.3.8 Embedded Trace Macro Cell (ETM) Timing**

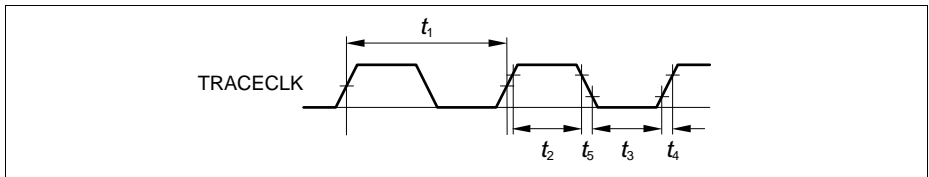
The Data timing are to the active clock edge, in half-rate clocking mode that is the rising and falling clock edge.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

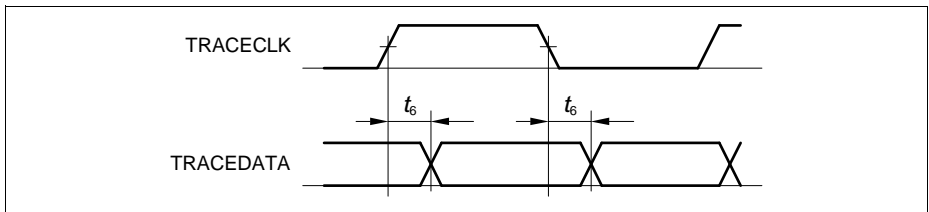
*Note: Operating conditions apply, with  $C_L \leq 15 \text{ pF}$ .*

**Table 44 ETM Interface Timing Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TRACECLK period	$t_1$ CC	16.7	–	–	ns	–
TRACECLK high time	$t_2$ CC	2	–	–	ns	–
TRACECLK low time	$t_3$ CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	$t_4$ CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	$t_5$ CC	–	–	3	ns	–
TRACEDATA output valid time	$t_6$ CC	-2	–	3	ns	–



**Figure 17 ETM Clock Timing**



**Figure 18 ETM Data Timing**

### 3.3.9 Peripheral Timing

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

*Note: Operating conditions apply.*

#### 3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

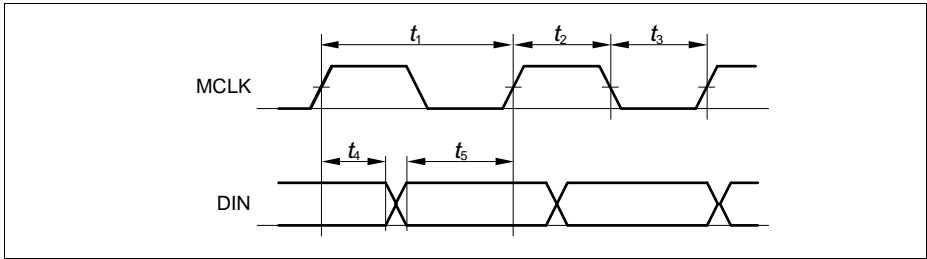
The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).

Data timing are to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 45 DSD Interface Timing Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MCLK period in master mode	$t_1$ CC	tbd	–	–	ns	
MCLK high time in master mode	$t_2$ CC	tbd	–	–	ns	
MCLK low time in master mode	$t_3$ CC	tbd	–	–	ns	
MCLK period in slave mode	$t_1$ SR	tbd	–	–	ns	$t_1 \geq 2 \times 1 / f_{\text{PERIPH}}$
MCLK high time in slave mode	$t_2$ SR	tbd	–	–	ns	
MCLK low time in slave mode	$t_3$ SR	tbd	–	–	ns	
DIN input setup time to the active clock edge	$t_4$ SR	tbd	–	–	ns	
DIN input hold time to the active clock edge	$t_5$ SR	tbd	–	–	ns	



**Figure 19 DSD Data Timing**

### 3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 46 USIC SSC Master Mode Timing**

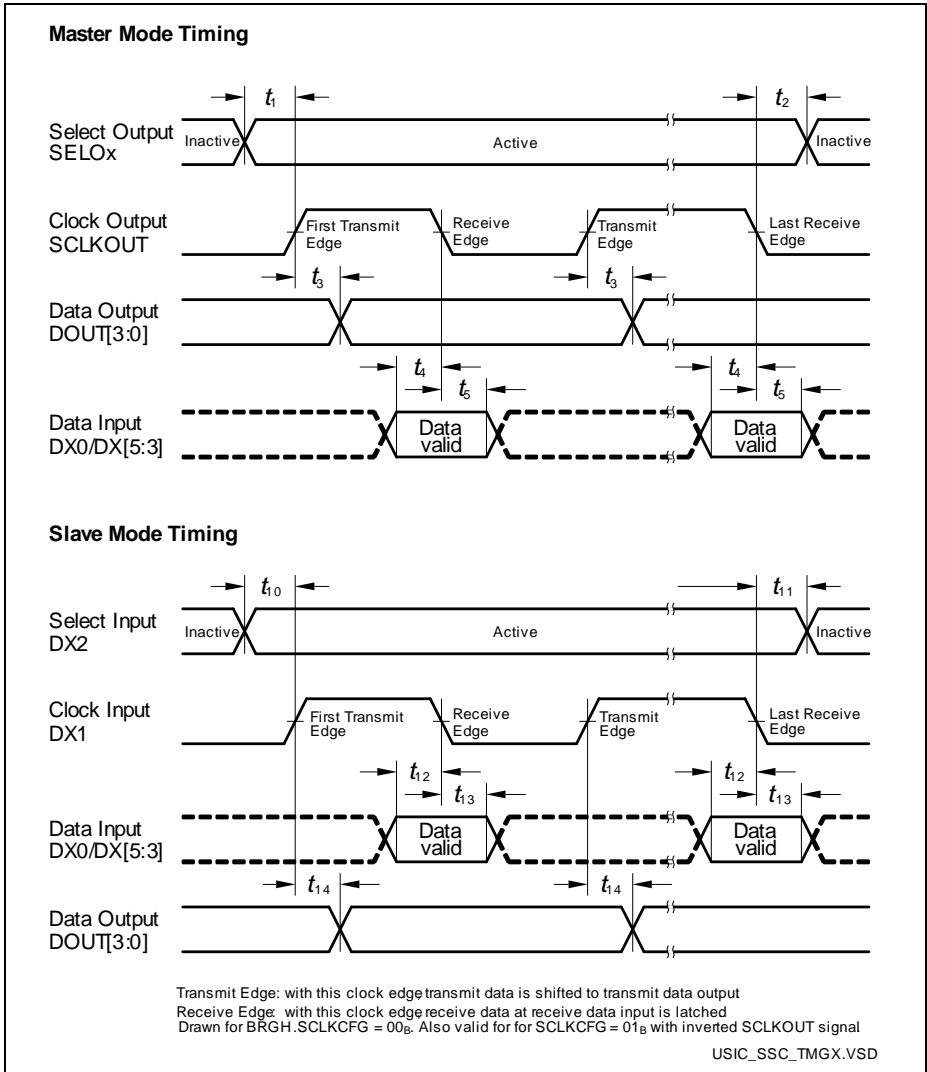
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	$t_{CLK}$ CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	$t_1$ CC	$t_{SYS} - 6.5^{1)}$	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	$t_2$ CC	$t_{SYS} - 8.5^{1)}$	–	–	ns	
Data output DOUT[3:0] valid time	$t_3$ CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	$t_4$ SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	$t_5$ SR	1	–	–	ns	

1)  $t_{SYS} = 1 / f_{PB}$

**Table 47 USIC SSC Slave Mode Timing**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	$t_{CLK}$	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge <sup>1)</sup>	$t_{10}$	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge <sup>1)</sup>	$t_{11}$	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge <sup>1)</sup>	$t_{12}$	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge <sup>1)</sup>	$t_{13}$	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	$t_{14}$	CC	0	–	24	ns	

1) These input timing are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



**Figure 20 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*



### 3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

*Note: Operating Conditions apply.*

**Table 48 USIC IIC Standard Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	-	-	1000	ns	
Data hold time	$t_3$ CC/SR	0	-	-	μs	
Data set-up time	$t_4$ CC/SR	250	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	$t_6$ CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	$t_7$ CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	$t_8$ CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	$t_9$ CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	$C_b$ SR	-	-	400	pF	

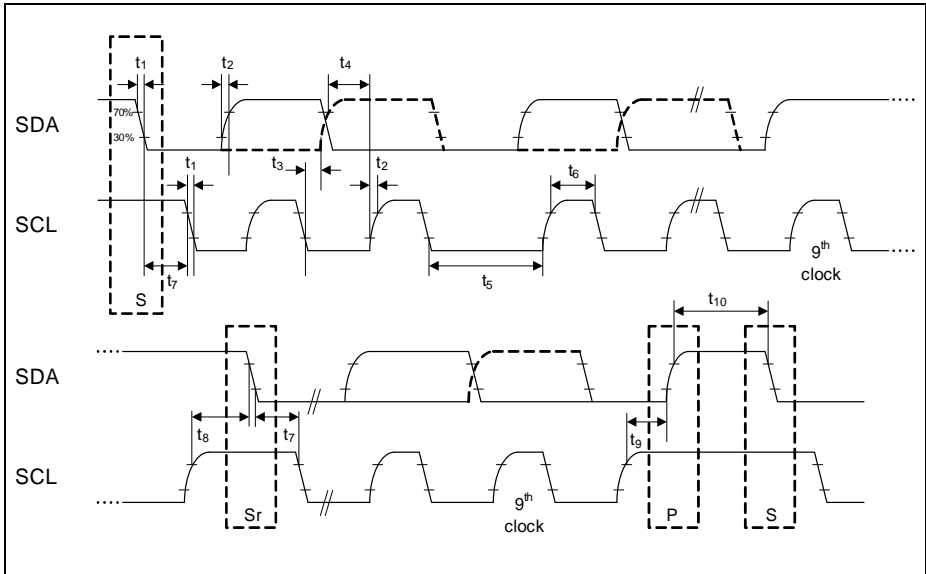
1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

**Table 49 USIC IIC Fast Mode Timing<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	$t_1$ CC/SR	20 + 0.1 * C <sub>b</sub> 2)	-	300	ns	
Rise time of both SDA and SCL	$t_2$ CC/SR	20 + 0.1 * C <sub>b</sub> 2)	-	300	ns	
Data hold time	$t_3$ CC/SR	0	-	-	µs	
Data set-up time	$t_4$ CC/SR	100	-	-	ns	
LOW period of SCL clock	$t_5$ CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	$t_6$ CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	$t_7$ CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	$t_8$ CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	$t_9$ CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	$t_{10}$ CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C <sub>b</sub> SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C<sub>b</sub> refers to the total capacitance of one bus line in pF.



**Figure 21 USIC IIC Stand and Fast Mode Timing**

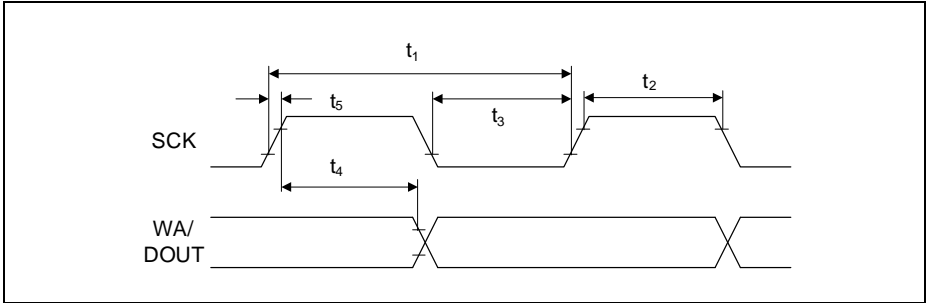
### 3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 50 USIC IIS Master Transmitter Timing**

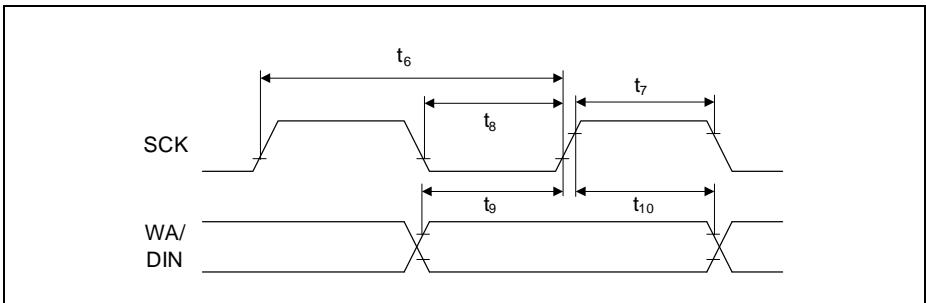
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_1$ CC	33.3	–	–	ns	
Clock HIGH	$t_2$ CC	0.35 x $t_{1min}$	–	–	ns	
Clock Low	$t_3$ CC	0.35 x $t_{1min}$	–	–	ns	
Hold time	$t_4$ CC	0	–	–	ns	
Clock rise time	$t_5$ CC	–	–	0.15 x $t_{1min}$	ns	



**Figure 22 USIC IIS Master Transmitter Timing**

**Table 51 USIC IIS Slave Receiver Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	$t_6$ SR	66.6	—	—	ns	
Clock HIGH	$t_7$ SR	$0.35 \times t_{6min}$	—	—	ns	
Clock Low	$t_8$ SR	$0.35 \times t_{6min}$	—	—	ns	
Set-up time	$t_9$ SR	$0.2 \times t_{6min}$	—	—	ns	
Hold time	$t_{10}$ SR	0	—	—	ns	



**Figure 23 USIC IIS Slave Receiver Timing**

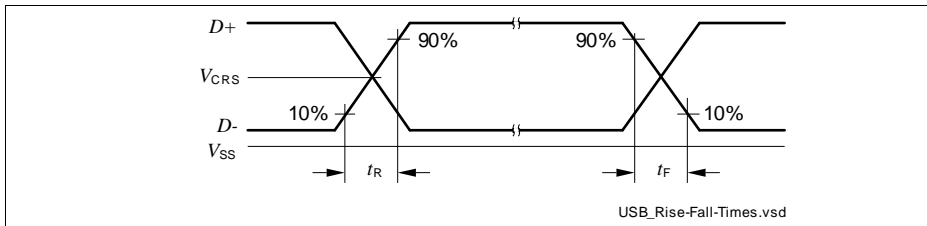
### 3.3.10 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 52 USB Timing Parameters** (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	$t_R$	CC	4	–	20	ns	$C_L = 50 \text{ pF}$
Fall time	$t_F$	CC	4	–	20	ns	$C_L = 50 \text{ pF}$
Rise/Fall time matching	$t_R/t_F$	CC	90	–	111.11	%	$C_L = 50 \text{ pF}$
Crossover voltage	$V_{CRS}$	CC	1.3	–	2.0	V	$C_L = 50 \text{ pF}$



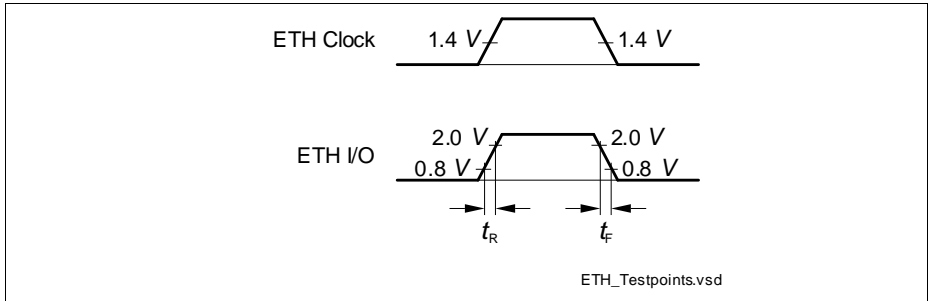
**Figure 24 USB Signal Timing**

### 3.3.11 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that  $f_{SYS} \geq 100$  MHz.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.11.1 ETH Measurement Reference Points

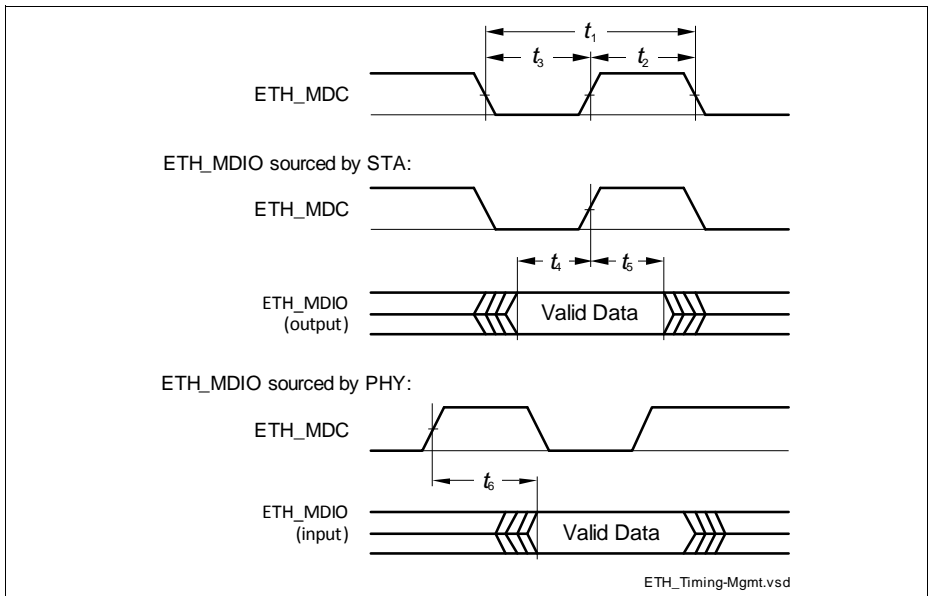


**Figure 25 ETH Measurement Reference Points**

**3.3.11.2 ETH Management Signal Parameters (ETH\_MDC, ETH\_MDIO)**

**Table 53 ETH Management Signal Timing Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	$t_1$	CC	400	–	–	ns	$C_L = 25 \text{ pF}$
ETH_MDC high time	$t_2$	CC	160	–	–	ns	
ETH_MDC low time	$t_3$	CC	160	–	–	ns	
ETH_MDIO setup time (output)	$t_4$	CC	10	–	–	ns	
ETH_MDIO hold time (output)	$t_5$	CC	10	–	–	ns	
ETH_MDIO data valid (input)	$t_6$	SR	0	–	300	ns	



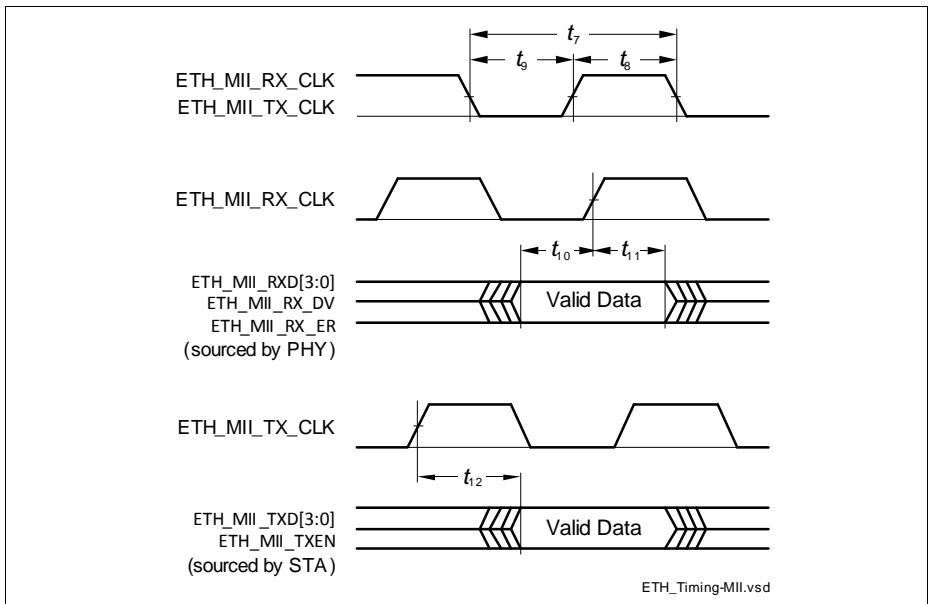
**Figure 26 ETH Management Signal Timing**

**3.3.11.3 ETH MII Parameters**

In the following, the parameters of the MII (Media Independent Interface) are described.

**Table 54 ETH MII Signal Timing Parameters**

Parameter	Symbol	SR	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	$t_7$	SR	400	–	–	ns	$C_L = 25 \text{ pF}$
Clock high time, 10 Mbps	$t_8$	SR	140	–	260	ns	
Clock low time, 10 Mbps	$t_9$	SR	140	–	260	ns	
Clock period, 100 Mbps	$t_7$	SR	40	–	–	ns	
Clock high time, 100 Mbps	$t_8$	SR	14	–	26	ns	
Clock low time, 100 Mbps	$t_9$	SR	14	–	26	ns	
Input setup time	$t_{10}$	SR	10	–	–	ns	
Input hold time	$t_{11}$	SR	10	–	–	ns	
Output valid time	$t_{12}$	CC	0	–	25	ns	



**Figure 27 ETH MII Signal Timing**

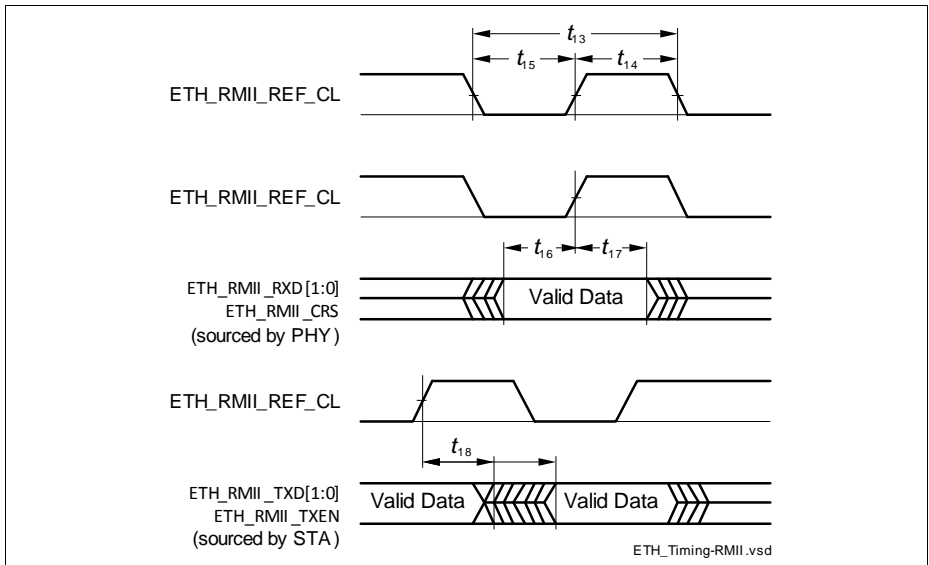


**3.3.11.4 ETH RMII Parameters**

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

**Table 55 ETH RMII Signal Timing Parameters**

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	$t_{13}$	SR	20	–	–	ns	$C_L = 25 \text{ pF}$ ; 50 ppm
ETH_RMII_REF_CL clock high time	$t_{14}$	SR	7	–	13	ns	$C_L = 25 \text{ pF}$
ETH_RMII_REF_CL clock low time	$t_{15}$	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRD setup time	$t_{16}$	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRD hold time	$t_{17}$	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	$t_{18}$	CC	4	–	15	ns	



**Figure 28 ETH RMII Signal Timing**

## 4 Package and Reliability

The XMC4400 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

### 4.1 Package Parameters

**Table 56** provides the thermal characteristics of the packages used in XMC4400.

**Table 56 Thermal Characteristics of the Packages**

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	7.0 × 7.0	mm	PG-LQFP-100-11
		-	5.8 × 5.8	mm	PG-LQFP-64-19
Thermal resistance Junction-Ambient	R <sub>ΘJA</sub> CC	-	20.5	K/W	PG-LQFP-100-11 <sup>1)</sup>
		-	tbd	K/W	PG-LQFP-64-19 <sup>1)</sup>

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground V<sub>SS</sub>, independent of EMC and thermal requirements.*

#### 4.1.1 Thermal Considerations

When operating the XMC4400 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance R<sub>ΘJA</sub>” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by  $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$  (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

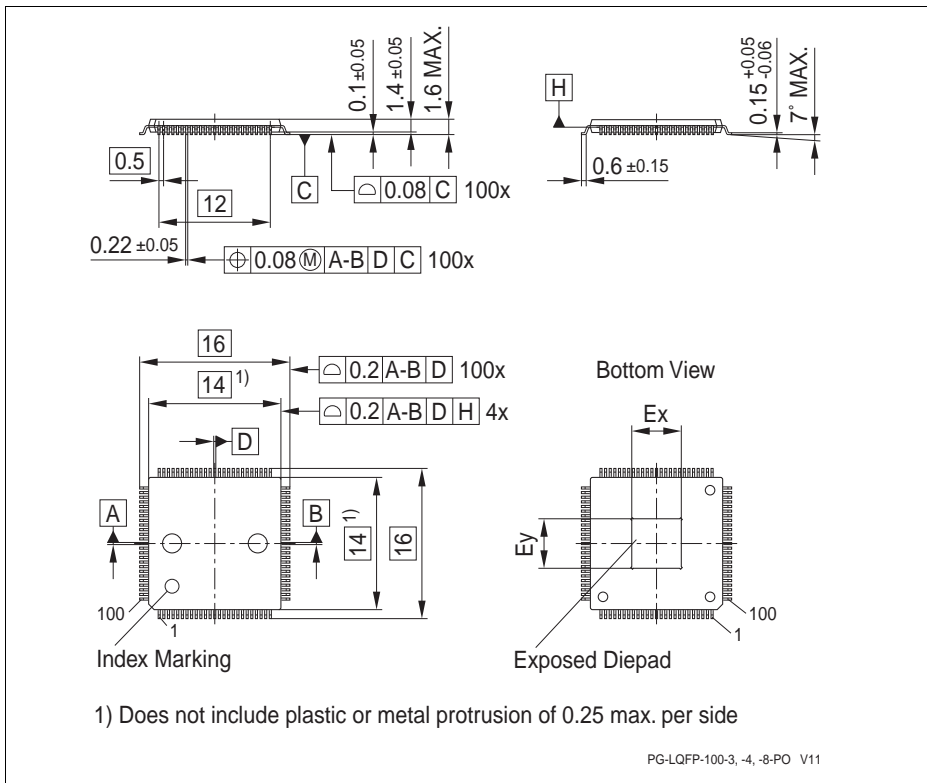
$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers ( $P_{IODYN}$ ) depends on the capacitive load connected to the respective pins and their switching frequencies.

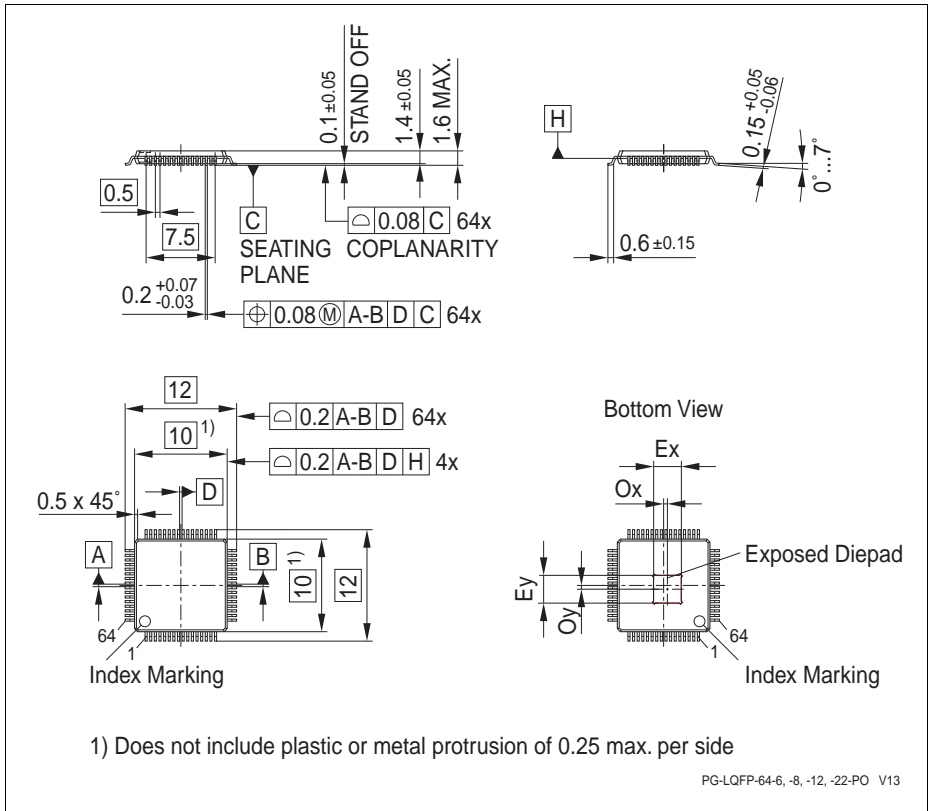
If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce  $V_{DDP}$ , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

## 4.2 Package Outlines



**Figure 29 PG-LQFP-100-11 (Plastic Green Low Profile Quad Flat Package)**



**Figure 30 PG-LQFP-64-19 (Plastic Green Low Profile Quad Flat Package)**

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": <http://www.infineon.com/packages>

## 5 Quality Declarations

The qualification of the XMC4400 is executed according to the JEDEC standard JESD47H.

*Note: For automotive applications refer to the Infineon automotive microcontrollers.*

**Table 57 Quality Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	$t_{OP}$ CC	20	–	–	a	$T_J \leq 109^\circ\text{C}$ , device permanent on
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM}$ SR	–	–	2 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	$V_{CDM}$ SR	–	–	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	$MSL$ CC	–	–	3	–	JEDEC J-STD-020C

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