TLE7269G

Twin LIN Transceiver

Automotive Power

Never stop thinking

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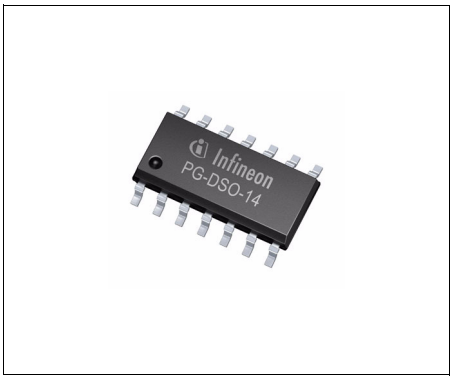
1 Overview



PG-DSO-14

Features

- Two stand-alone LIN transceivers up to 20 kBaud transmission rate
- Pin compatible to single LIN Transceivers (e.g TLE7259-2GE/GU)
- Compliant to LIN specification 1.3, 2.0, 2.1 and SAE J2602
- Very high ESD robustness, ± 8 kV according to IEC61000-4-2
- Optimized for low electromagnetic emission (EME)
- Optimized for high immunity against electromagnetic interference (EMI)
- Very low current consumption in sleep mode with Wake-Up functions
- Wake-Up source detection on Wake-Up disable function
- Very low leakage current on the BUS output
- Control output for voltage regulator
- Digital I/O levels compatible for 3.3 V and 5 V microcontrollers
- Bus short to V_{BAT} protection and Bus short to GND handling
- Over-temperature and Under-voltage protection
- Flash mode and Low-Slope Mode
- Green Product (RoHs compliant)
- AEC compliant

Description

The TLE7269G is a transceiver for the Local Interconnect Network (LIN) with integrated Wake-Up and protection features. It is designed for in-vehicle networks using data transmission rates from 2.4 kBaud to 20 kBaud. The TLE7269G functions as a bus driver between the protocol controller and the physical bus inside the LIN network. Compliant to all LIN standards and with a wide operational supply range the TLE7269G can be used in all automotive applications.

Two stand-alone LIN transceivers are integrated on one monolithic circuit inside TLE7269G. Both transceivers offer different operation modes and separate INH outputs to control external circuitry, like voltage regulators. In Sleep-mode the TLE7269G draws less than 10 µA of quiescent current for both integrated LIN Transceivers, while both transceivers are still able to wake up off of LIN bus traffic or the local Wake-Up input. The very low leakage current on the BUS pins makes the TLE7269G especially suitable for partially supplied networks and supports the low quiescent current requirements of the LIN network.

Based on the Infineon Smart Power Technology SPT®, the TLE7269G provides excellent ESD robustness together with a very high electromagnetic immunity (EMI). The TLE7269G reaches a very low level of electromagnetic emission (EME) within a broad frequency range and independent from the battery voltage.

The Infineon Smart Power Technology SPT® allows bipolar and CMOS control circuitry in accordance with DMOS power devices to exist on the same monolithic circuit. The TLE7269G and the Infineon SPT® technology are AEC qualified and tailored to withstand the harsh conditions of the Automotive Environment.

Type	Package	Marking
TLE7269G	PG-DSO-14	7269G

2 Block Diagram

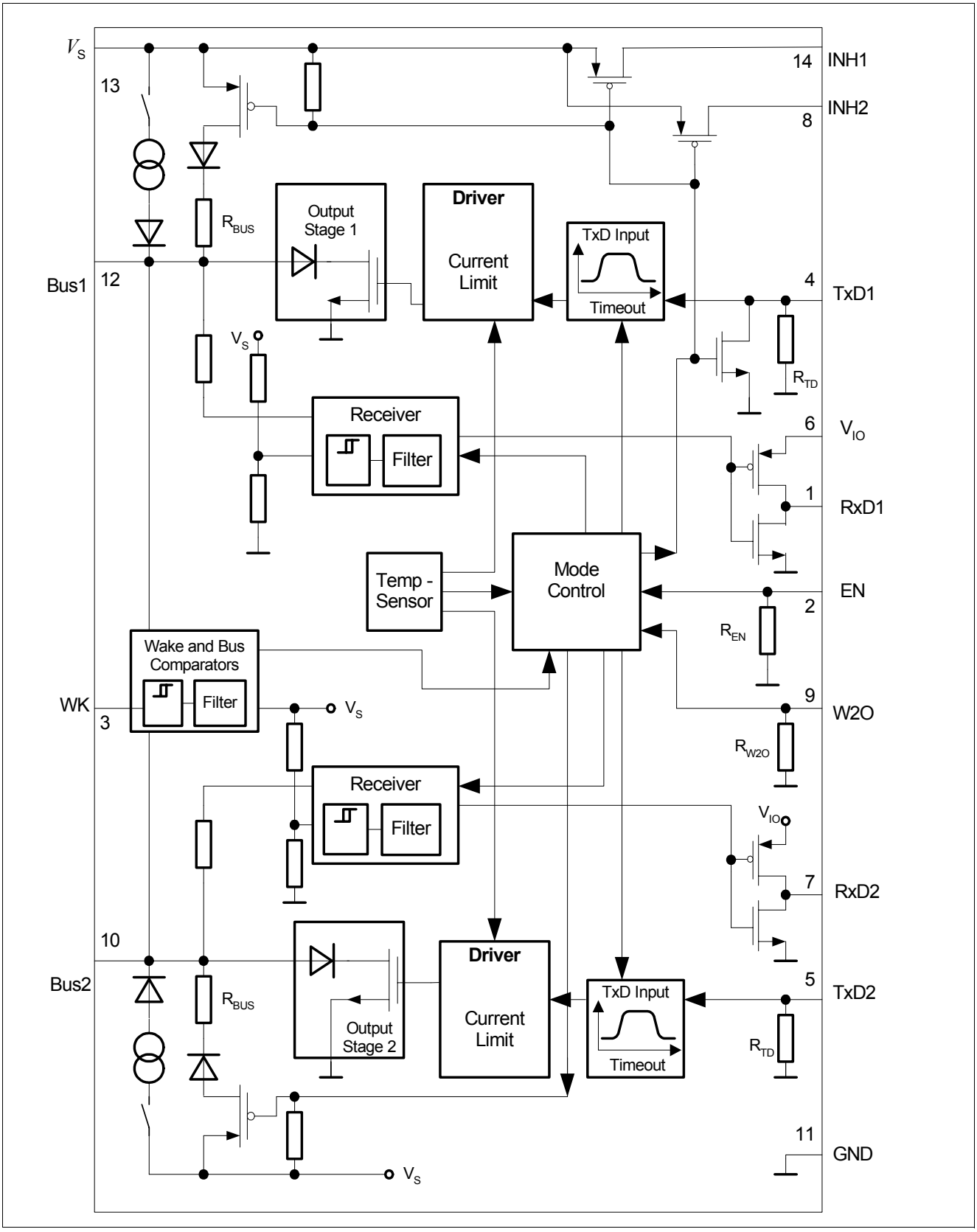


Figure 1 Functional Block Diagram

3 Pin Configuration

3.1 Pin Assignment

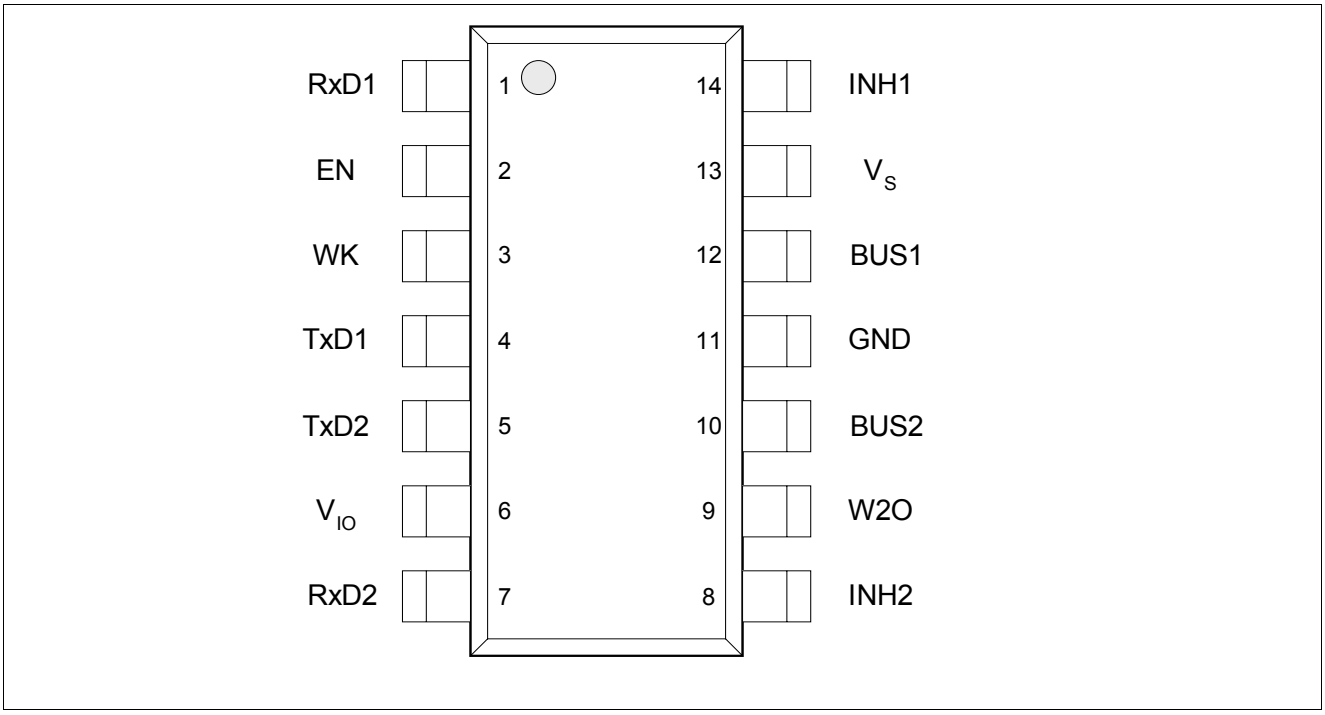


Figure 2 Pin Configuration (top view)

Note: The pin configuration of the TLE7269G is pin compatible to the devices TLE7259G and TLE7259-2GE/GU. In comparison to the TLE7259G and the TLE 7259-2GE/GU, no pull up resistors on the RxD pins are required for the TLE7269G. Details can be found inside the ***"Pin Compatibility to the Single LIN Transceivers" on Page 28****.*

3.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Function
1	RxD1	**Receive data output 1;** LOW in dominant state, active LOW after a Wake-Up event at BUS1 or WK pin
2	EN	**Enable input;** integrated pull-down, device set to normal operation mode when HIGH
3	WK	**Wake input;** active LOW, negative edge triggered, internal pull-up
4	TxD1	**Transmit data input 1;** integrated pull-down, LOW in dominant state; active LOW after Wake-Up via WK pin
5	TxD2	**Transmit data input 2;** integrated pull-down, LOW in dominant state
6	V_{IO}	**Logic Voltage supply input;** 3.3V or 5V supply for the RxD and TxD pins
7	RxD2	**Receive data output 2;** LOW in dominant state, active LOW after a Wake-Up event at BUS2

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
8	INH2	**Inhibit output 2;** battery supply related output HIGH (V_S) in Normal and Stand-By operation mode can be used to control an external voltage regulator can be used to control external bus termination resistor when the device will be used as Master node
9	W2O	**Wake BUS 2 OFF;** switch off Wake-Up feature on BUS 2; active HIGH, integrated pull-down
10	BUS 2	**Bus 2 input / output;** LIN bus line input/output LOW in dominant state Internal termination and pull-up current source
11	GND	**Ground**
12	BUS 1	**Bus 1 input / output;** LIN bus line input/output LOW in dominant state Internal termination and pull-up current source
13	V_S	**Battery supply input**
14	INH1	**Inhibit output 1;** battery supply related output HIGH (V_S) in Normal and Stand-By operation mode can be used to control an external voltage regulator can be used to control external bus termination resistor when the device will be used as Master node

4 Functional Description

The LIN Bus is a single wire, bi-directional bus, used for in-vehicle networks. The LIN Transceiver TLE7269G is the interface between the microcontroller and the physical LIN Bus (see **Figure 17** and **Figure 18**). The logical values of the microcontroller are driven to the LIN bus via the TxD inputs of the TLE7269G. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rate to minimize the EME level of the LIN network. The RxD outputs read back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise on the LIN Bus and to increase the EMI (Electro Magnetic Immunity) level of the transceiver.

Two logical states are possible on the LIN bus according to the LIN Specification 2.1 (see **Figure 3**):

In dominant state, the voltage on the LIN bus is set to the GND level. In recessive state, the voltage on the LIN bus is set to the supply voltage V_S. By setting the TxD1, TxD2 inputs of the TLE7269G to “Low” the transceiver generates a dominant level on the BUS1, BUS2 LIN interface pins. The RxD1, RxD2 outputs read back the signal on the LIN bus and indicate a dominant signal on the LIN bus with a logical “Low” to the microcontroller. Setting the TXD1, TxD2 pins to “High” the transceiver TLE7269G sets the BUS1, BUS2 LIN interface pins to recessive level, at the same time the recessive level on the LIN bus is indicated by a logical “High” on the RxD1, RxD2 outputs.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE7269G for master node applications, a resistor in the range of 1 kΩ and a reverse diode must be connected between the LIN bus and the power supply V_S or between the LIN bus and INH pin of the TLE7269G (see **Figure 17** and **Figure 18**).

Both integrated transceivers can operate independent from each other and several operation modes and Wake-Up functions are implemented. The bus Wake-Up function of the transceiver 2 can be turned off via the W2O pin.

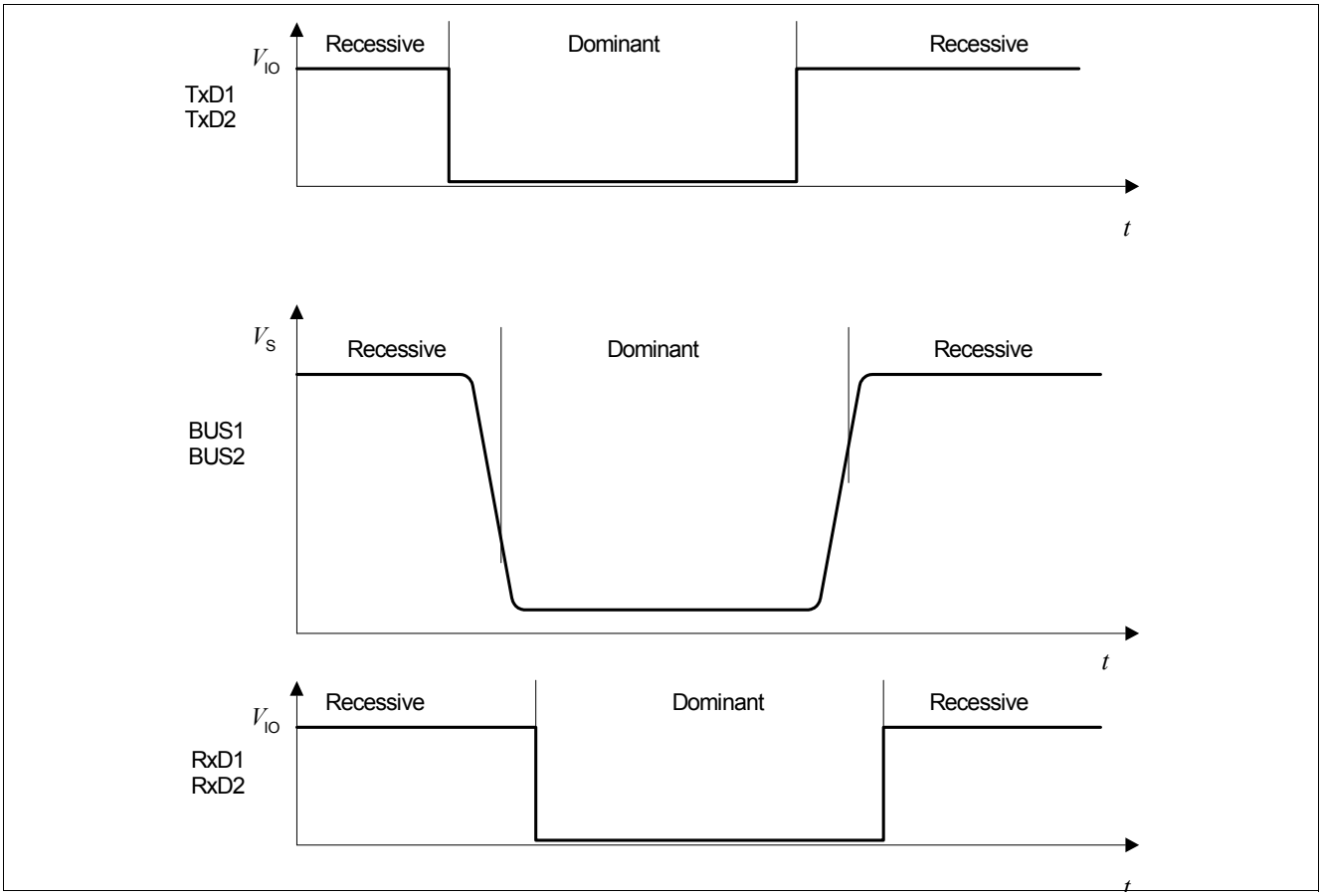


Figure 3 LIN bus signals

4.1 Operating Modes

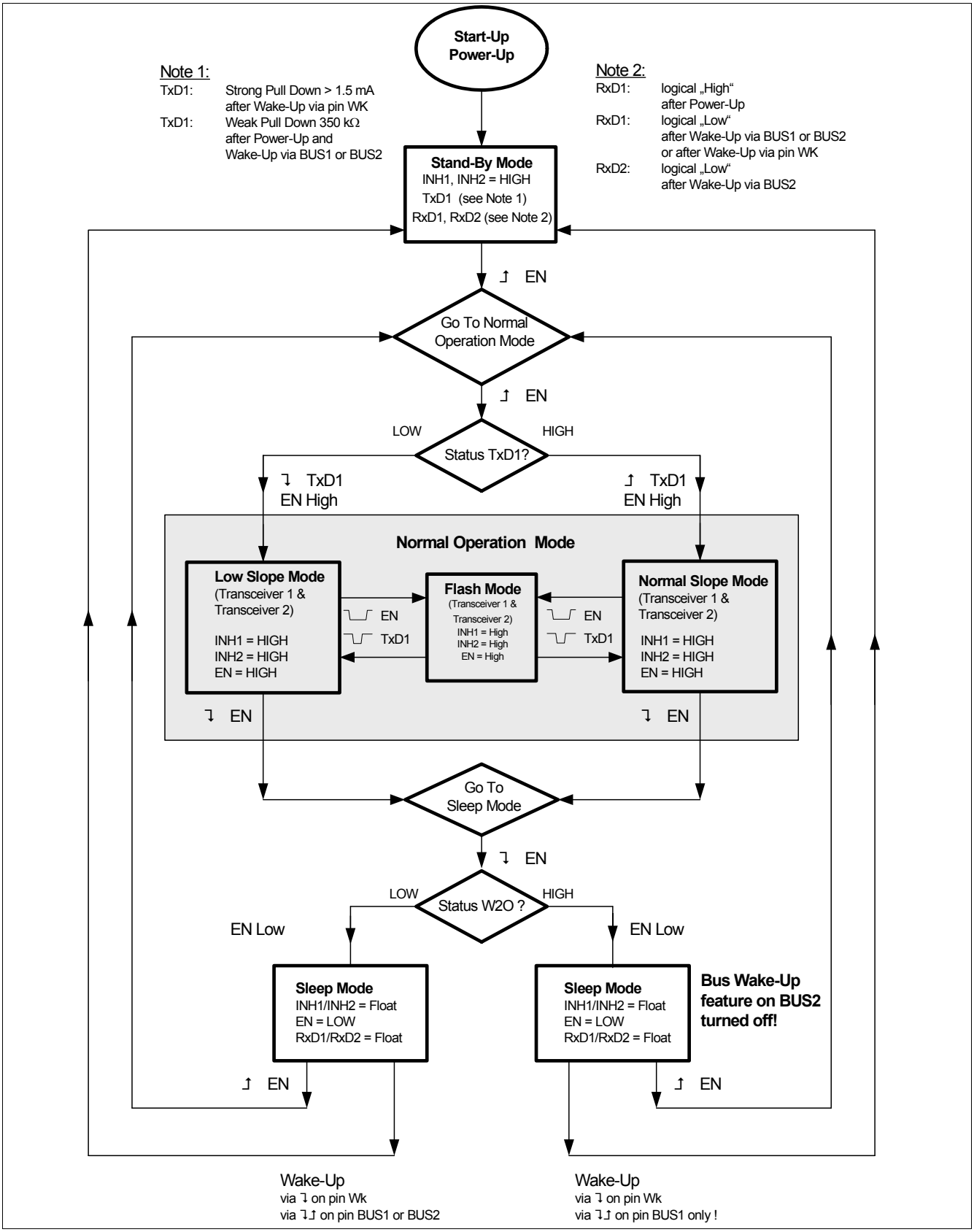


Figure 4 Operation Mode State Diagram

The TLE7269G has 3 major operation modes:

- Stand-By mode
- Normal Operation mode
- Sleep mode

The Normal Operation mode contains 3 sub-operation modes, which differentiate by the slew rate control of the LIN Bus signal (see **Figure 4**).

Sub-operation modes with different slew rates on the BUS1,BUS2 pins:

- Low Slope mode, for data transmission rates up to 10.4 kBaud
- Normal Slope mode, for data transmission rates up to 20 kBaud
- Flash mode, for programming of the external microcontroller

The TLE7269G contains 2 separate LIN transceivers, which are able to operate in two independent LIN networks with two different data transmission rates. The operation mode of the TLE7269G is selected by the EN pin and the TxD1 pin. Selecting the operation mode applies to the whole device. Transceiver1 and transceiver2 are always set to the same operation mode and sub-operation mode (see **Figure 4**).

Table 2 Operating modes

Mode	EN	INH1 INH2	TxD1 TXD2	RxD1 RxD2	LIN Bus Termination	Comments
Sleep	Low	Floating	Low	High resistive	High Impedance	No Wake-Up request detected
Stand-By	Low	High	Low High[2)]	Low High [1)]	30 kΩ (typical)	RxD1 “Low” after local or bus Wake-Up (BUS 1, BUS 2) RxD2 “Low” after bus Wake-Up on Bus2. RxD2 “High” on all other Wake-Up and Power-Up events. RxD1 “High” after Power-Up TxD1 strong pull down after local Wake-Up (WK pin)[2)] TxD1 weak pull down after bus Wake-Up (BUS1, BUS2) or Power-Up[2)]
Normal Operation	High	High	Low High	Low High	30 kΩ (typical)	RxD1, RxD2 reflects the signal on the BUS1, BUS2 TxD1,TxD2 driven by the microcontroller

1) To indicate the Wake-Up sources via the RxD pins the power supply V_{IO} has to be present

2) The TxD1 input needs an external termination to indicate a “High” or a “Low” signal. The external termination could be a pull-up resistor or an active microcontroller output.

4.2 Normal Operation Mode

The TLE7269G enters the Normal Operation mode after the microcontroller sets EN to “High” (see **Figure 4**). In Normal Operation mode both LIN bus receivers and both LIN bus transmitters are active. Data from the microcontroller is transmitted to the LIN bus1 or LIN bus2 via the TxD1 or TxD2 pin, the receiver detects the data stream on the LIN bus1 or bus2 and forwards it to the RxD1 or RxD2 output pins. In Normal Operation mode, the INH1 pin and the INH2 are “High” (set to V_S) and the bus termination is set to 30 kΩ for both integrated transceivers.

Normal Slope mode, Low Slope mode and the Flash mode are Normal Operation modes and in these sub-modes the behavior of the INH pin and the bus termination is the same. To set the device into one of these 3 sub-modes the TxD1 pin and the EN pin are used for the sub-operation mode selection. In order to avoid any bus disturbance during a mode change, the output stages of the TLE7269G are disabled and set to recessive state during the mode change procedure. To release the TLE7269G for data communication on the LIN bus1 and LIN bus2, the TxD1 and TxD2 pins need to be set to “High” for the time $t_{to,rec}$.

4.2.1 Normal Slope Mode

In Normal Slope mode data transmission rates up to 20 kBauds are possible. Setting the EN pin to “High” starts the transition to Normal Operation mode. Depending on the signal on the TxD1 pin, the TLE7269G changes either into Normal Slope mode or Low Slope mode (see **Figure 5**).

The mode change to Normal Slope mode is defined by the time t_{MODE} and the time $t_{TXD,SET}$. The time t_{MODE} specifies the delay time between the threshold, where the EN pin detects a “High” input signal, and the actual mode change of TLE7269G into Normal Slope mode. The time $t_{TXD,SET}$ defines the setup time in which the TxD1 pin has be set to “High”. After the time $t_{TXD,SET}$ expires, the logical “High” signal on the TxD1 pin has to be stable to put the part into Normal Slope mode.

In the time window t_{MODE} - $t_{TXD,SET}$ the TLE7269G makes the transition to Normal Slope mode but remains in Stand-By mode until the time t_{MODE} expires.

Finally to release the data communication it is required to set the TxD1 and the TxD2 pin to “High” for the time $t_{to,rec.}$

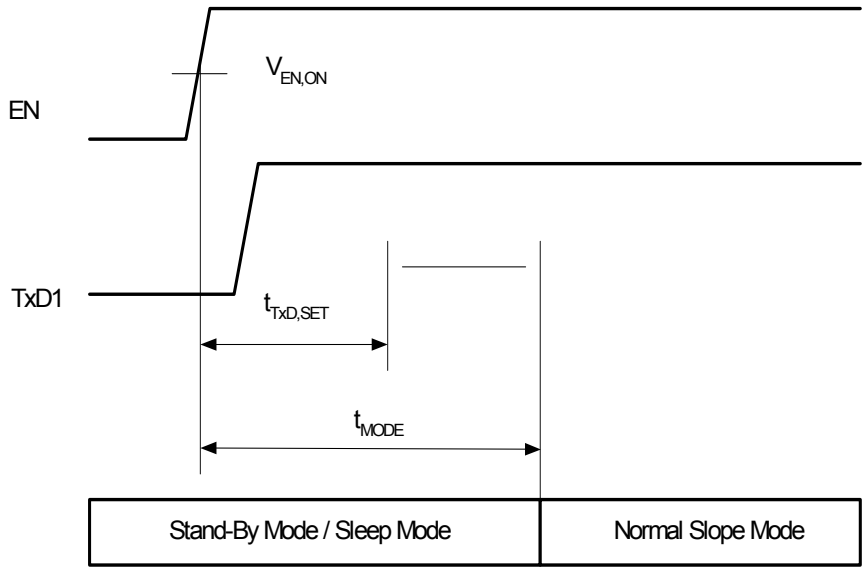


Figure 5 Timing to enter Normal Slope Mode

4.2.2 Low Slope Mode

In Low Slope mode data transmission rates up to 10.4 kBauds are possible. Setting the EN pin to “High” starts the transition to Normal Operation mode. Depending on the signal of the TxD1 pin the TLE7269G changes either into Normal Slope mode or Low Slope mode (see **Figure 6**).

The mode change to Low Slope mode is defined by the time t_{MODE} and the time $t_{TXD,SET}$. The time t_{MODE} specifies the delay time between the threshold, where the EN pin detects a “High” input signal, and the actual mode change of TLE7269G to Low Slope mode. The time $t_{TXD,SET}$ defines the setup time in which the TxD1 pin can be set to “Low”. After the time $t_{TXD,SET}$ expires, the logical “Low” signal on the TxD1 pin has to be stable to put the part into Low Slope mode.

In the time window t_{MODE} - $t_{TXD,SET}$ the TLE7269G makes the transition into Low Slope mode but remains in Stand-By mode until the time t_{MODE} expires.

Finally to release the data communication it is required to set the TxD1 and the TxD2 pin to “High” for the time $t_{to,rec.}$

4.3 Stand-By Mode

The Stand-By mode is entered automatically after:

- A Power-Up event on the supply V_S.
- A bus Wake-Up event on pin BUS1 or pin BUS2.
- A local Wake-Up event on the pin WK.
- A power on reset caused by power supply V_S or by the power supply V_{IO}
- In Stand-By mode the Wake-Up sources are monitored by the TxD1, RxD1 and RxD2 pins.

In Stand-By mode no communication on the LIN Bus is possible. The output stages are disabled and the LIN Bus termination remains activated on both integrated transceivers. Only the RxD1, RxD2 and the TxD1 pin are used to indicate the Wake-Up source. The TxD2 pin remains inactive. The RxD1 pin remains “Low” after a local Wake-Up event on the pin WK and a bus Wake-Up event on either the bus 1 or the bus 2. The RxD2 pin remains “Low” only after a bus Wake-Up event on the bus 2. A Power-Up event is indicated by a logical “High” on the RxD1 pin. The signal on the TxD1 pin indicates the Wake-Up source, a weak pull-down signals a bus Wake-Up event on the bus 1 and bus 2 and a strong pull-down signals a local Wake-Up event caused by the WK pin (see **Table 2** and **Table 3**). In order to detect a Wake-Up event via the TxD1 pin, the external microcontroller output needs to provide a logical “High” signal. The Wake-Up flags indicating the Wake-Up source on the pins TxD1, RxD1 and RxD2 are reset by changing the operation mode to Normal Operation mode.

The signal on the EN pin remains “Low” due to an internal pull-down resistor. Setting the EN pin to “High”, by the microcontroller returns the TLE7269G to Normal Operation mode. In Stand-By mode the INH1 and INH2 outputs are switching to V_S. The INH outputs can be used to control external device like a voltage regulator.

Table 3 Logic table for wake up monitoring

Inputs				Outputs			
power up	**WK**	**BUS1**	**BUS2**	**RxD1**[1)]	**RxD2**[1)]	**TxD1**[2)]	**Remarks**
Yes	1	1	1	1	1	1	No Wake-Up, Power-Up event
No	Wake-Up[3)]	1	1	0	1	0	Wake via wake pin
No	1	Wake-Up[4)]	1	0	1	1	Wake via BUS1
No	1	1	Wake-Up[4)]	0	0	1	Wake via BUS2

1) To indicate the Wake-Up or Power-Up event on the RxD pin, the supply V_{IO} has to be present

2) The TxD1 input needs an external termination to indicate a “High” or a “Low” signal. The external termination could be a pull-up resistor or an active microcontroller output.

3) A local Wake-Up event is considered after a low signal on the pin WK (see **Chapter 4.8**).

4) A bus Wake-Up event is considered after the low to high transition on the bus (see **Chapter 4.7**).

Note: In the case of a sequence of Wake-Up events only the first Wake-Up event will be monitored on TxD1, RxD1 and RxD2. Subsequent Wake-Up events are ignored.

4.4 Sleep Mode

In order to reduce the current consumption the TLE7269G offers a Sleep mode. In Sleep mode the quiescent current on V_S and the leakage current on the pins BUS1 and BUS2 are cut back to a minimum.

To switch the TLE7269G from Normal Operation mode to Sleep mode, the EN pin has to be set to “Low”. Conversely a logical “High” on the EN pin sets the device directly back to Normal Operation mode (see **Figure 4**).

While the TLE7269G is in Sleep mode the following functions are available:

- The output stages are disabled and the internal bus terminations are switched off (High Impedance on the pins BUS1 and BUS2). Internal current sources on the bus pins ensure that the levels on the pins BUS1 and BUS2 remain recessive and protect the LIN network against accidental bus Wake-Up events.
- The receiver stages are turned off.
- RxD1, RxD2 output pins are inactive and “High resistive”. The TxD1, TxD2 pins are disabled. The logical state on the TxD1 pin and the TxD2 pin is “Low” due to the internal pull-down resistors.
- The INH1 and INH2 outputs are switched off and floating.
- The bus Wake-Up comparator is active and turns the TLE7269G to Stand-By mode in case of a bus Wake-Up event.
- The WK pin is active and turns the TLE7269G to Stand-By mode in case of a local Wake-Up.
- The EN pin remains active, switching the EN pin to “High” changes the operation mode to Normal Operation mode.

4.5 Wake-Up Events

A Wake-Up event changes the operation mode of the TLE7269G from Sleep mode to Stand-By mode. Both integrated transceivers are changing the mode.

There are 4 different ways to Wake-Up the TLE7269G from Sleep mode.

- Bus or also called remote Wake-Up via a dominant signal on the pin BUS1.
- Bus or also called remote Wake-Up via a dominant signal on the pin BUS2.
- Local Wake-Up via a minimum dominant time (t_{WK}) on the WK pin.
- Mode change from Sleep mode to Normal Operation mode, by setting EN pin to logical “High”.

4.6 Wake-Up Bus2 Off

A Wake-Up event on the LIN bus1 or on the bus2 wakes up the TLE7269G and sets it to Stand-By mode. In applications where a Wake-Up via bus1 is required but a Wake-Up via bus2 is not wanted, the bus Wake-Up event on the BUS2 can be disabled. This is done by setting the W2O pin to “High”. During the mode change from Normal Operation mode to Sleep mode the TLE7269G checks for the status on the pin W2O. In case the W2O pin is “High”, the Wake-Up feature for the transceiver 2 will be disabled. The TLE7269G can still be wake off by a bus Wake-Up event on LIN bus1 or by a local Wake-Up event on the pin WK. A bus Wake-Up event on the bus 2 won’t be recognized and the device remains in Sleep mode (see **Figure 4**).

In case the Wake-Up Bus2 Off feature is not used, the W2O pin can be left open, due to the internal pull-down resistor, a not connected W2O pin is set to logical “Low”. The function of the EN pin remain unchanged.

4.7 Bus Wake-Up via LIN bus 1 and bus 2

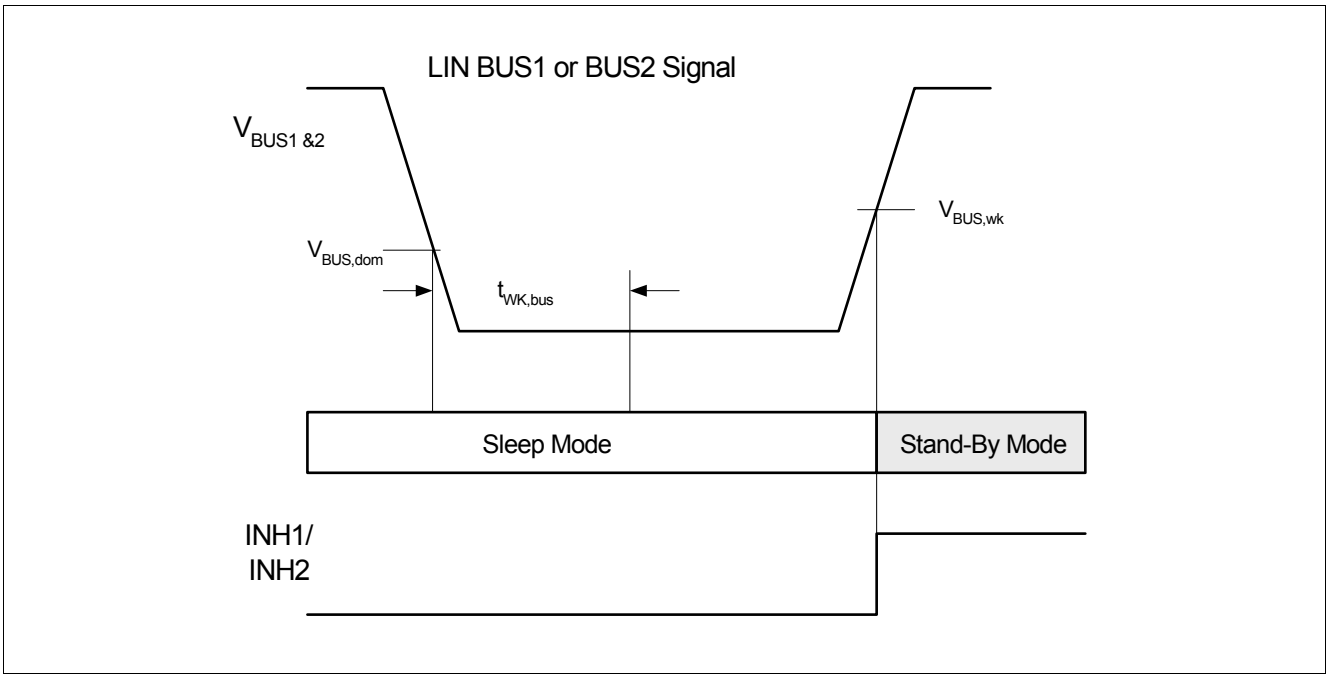


Figure 8 Bus Wake-Up behavior

The bus Wake-Up event, often called remote Wake-Up, changes the operation mode from Sleep mode to Stand-By mode. The TLE7269G wakes-up via a bus Wake-Up event on either the pin BUS1 or BUS2. The bus Wake-Up behavior is identical on both pins. A falling edge on the LIN bus, followed by a dominant bus signal t > $t_{WK,bus}$ results in a bus Wake-Up event. The mode change to Stand-By mode becomes active with the following rising edge on the LIN bus. The TLE7269G remains in Sleep mode until it detects a change from dominant to recessive on the LIN bus (see **Figure 8**).

In Stand-By mode the TxD1 pin indicates the source of the Wake-Up event, the TxD2 pin remains inactive. A weak pull-down on the pin TxD1 indicates a bus Wake-Up event (see **Figure 4** or **Table 2**). The RxD1 pin signals if a Wake-Up event occurred or the power-up event. A “Low” signal on the RxD1 pin reports a local or bus Wake-Up event, a logical “High“ signal on RxD1 indicates a power-up event. A “Low” signal on the RxD2 pin indicates a Wake-Up event on the pin BUS2.

4.8 Local Wake-Up

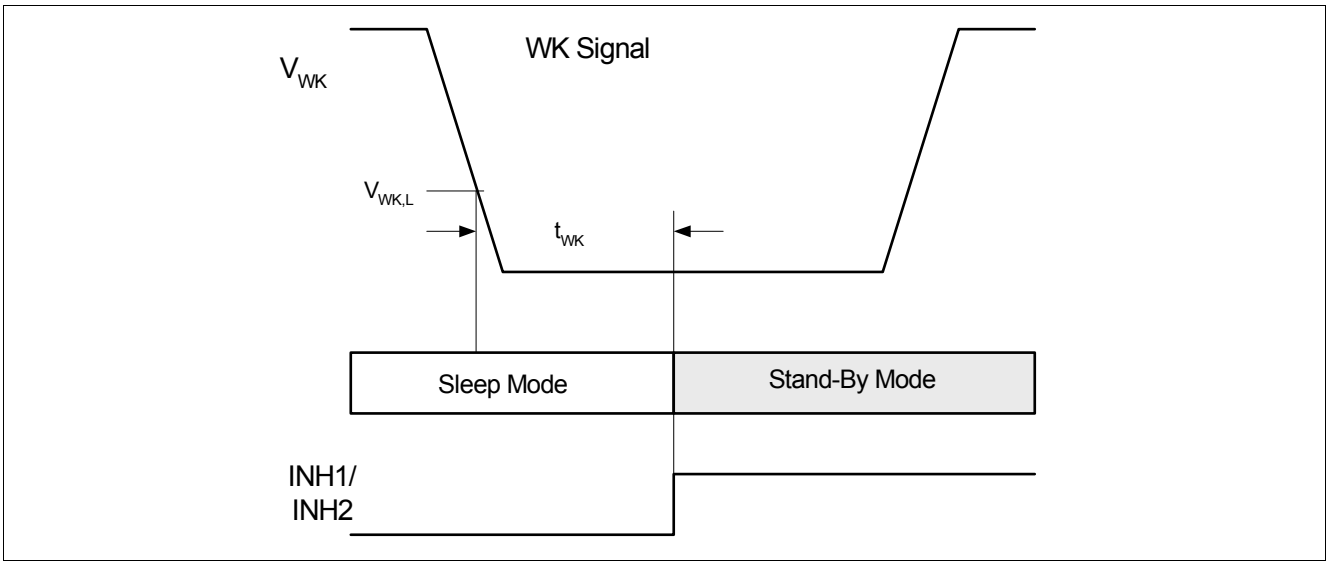


Figure 9 Local Wake-Up behavior

Beside the remote Wake-Up, a Wake-Up of the TLE7269G via the WK pin is possible. This type of Wake-Up event is called “Local Wake Up”. A falling edge on the WK pin followed by a “Low” signal for t > t_{WK} results in a local Wake-Up (see **Figure 9**) and changes the operation mode to Stand-By mode.

In Stand-By mode the TxD1 pin indicates the source of the Wake-Up event, the TxD2 pin remains inactive. A strong pull-down on the pin TxD1 indicates a bus Wake-Up event (see **Figure 4**). The RxD1 pin signals if a Wake-Up event or the Power-Up event occurred. A “Low” signal on the RxD1 pin reports a local or bus Wake-Up event, a logical “High” signal on RxD1 indicates a Power-Up event. A “Low” signal on the RxD2 pin indicates a Wake-Up event on the pin BUS2.

4.9 Mode Transition via EN pin

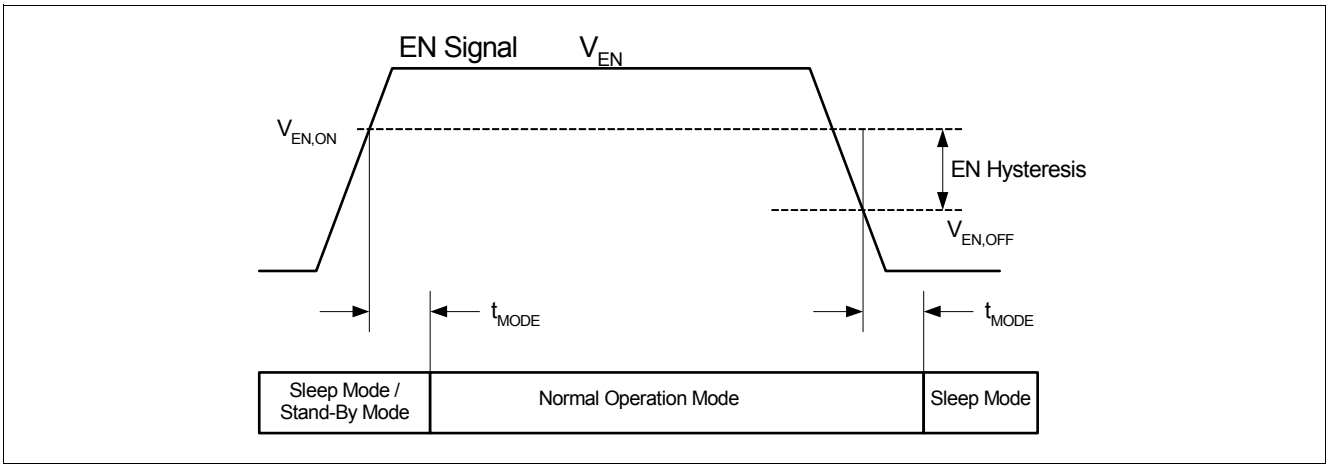


Figure 10 Mode Transition via EN pin

It is also possible to change from Sleep mode to Normal Operation mode by setting the EN pin to logical “High”.This feature is useful if the external microcontroller is continuously powered and not connected to the INH1 pin or the INH2 pin. The EN pin has an integrated pull-down resistor to ensure the device remains in Sleep or Stand-By mode even if the voltage on the EN pin is floating. The EN pin has an integrated hysteresis to avoid the toggling of the operation modes during the transition of the EN signal (see **Figure 10**).

A transition from logical “High” to logical “Low” on the EN pin changes the operation mode from Normal Operation mode to Sleep mode. If the TLE7269G is already in Sleep mode, changing the EN from “Low” to “High” results into a mode change from Sleep mode to Normal Operation mode. If the device is in Stand-By mode a change from “Low” to “High” on the EN pin changes the mode to Normal Operation mode (see **Figure 4**).

4.10 Power-On Reset

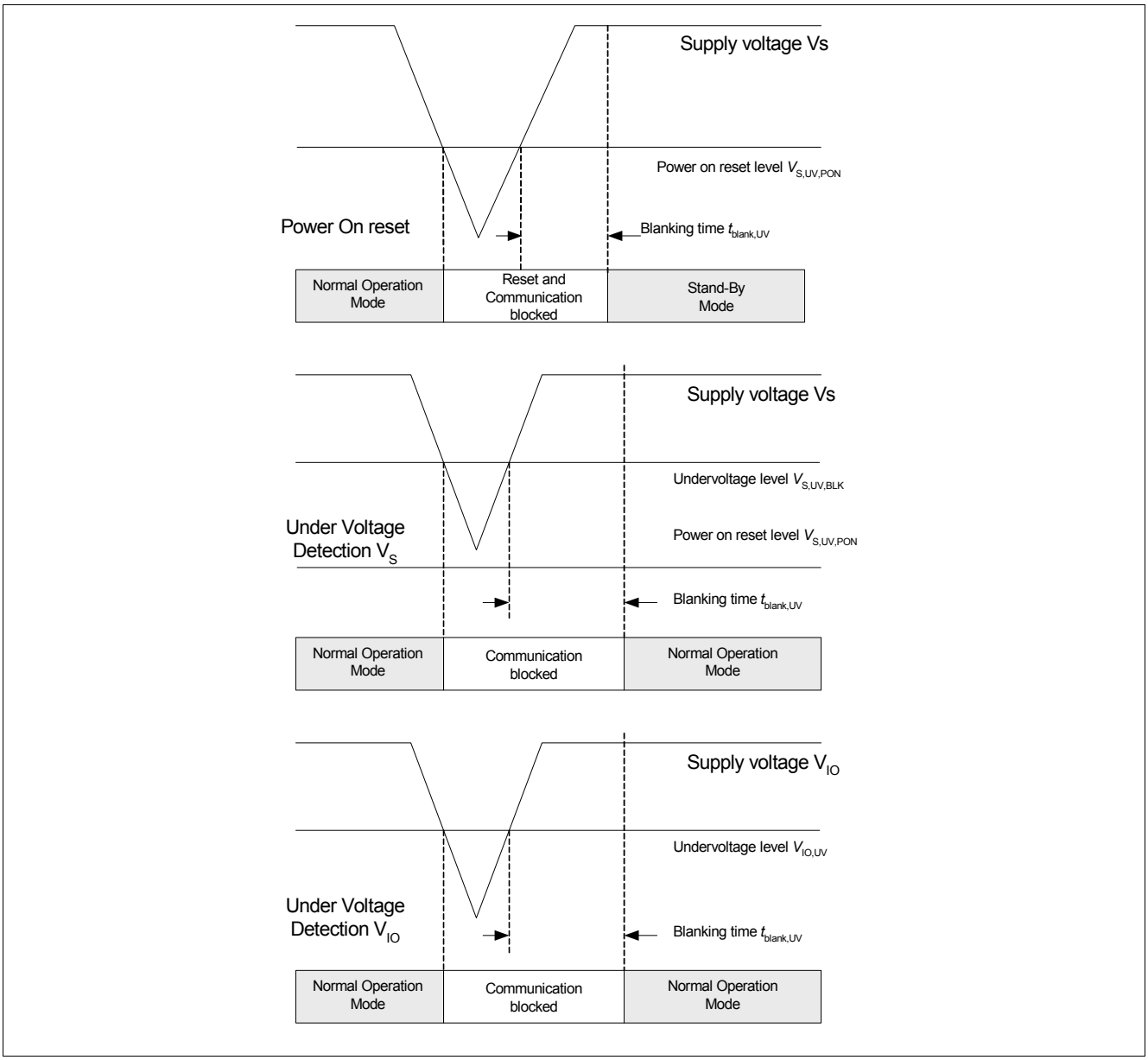


Figure 11 Power-on reset and Under-Voltage situation

A dropping power supply V_S or a dropping microcontroller supply V_{IO} on a local ECU can effect the communication of the whole LIN network. To avoid any blocking of the LIN network by a local ECU the TLE7269G has an integrated Power-On reset at the supply V_S and an Under-Voltage detection at the supply V_S and the supply V_{IO}. In case the supply voltage V_S is dropping below the Power-On reset level $V_S < V_{S,UV,PON}$, the TLE7269G changes the operation mode to Stand-By mode. In Stand-By mode the output stage of the TLE7269G is disabled and no communication to the LIN bus is possible. The internal bus termination remains active as well as the INH pins (see **Figure 11** and **Figure 4**).

In Stand-By mode the RxD1 pin signals the low power supply condition with a “High” signal. A logical “High” on the EN pin changes the operation mode back to Normal Operation mode.

In case the supply voltage V_S is dropping below the specified operation range (see **Table 5**), the TLE7269G disables the output and receiver stages. This feature secures the communication on the LIN bus. If the power supply V_S reaches a higher level as the Under-Voltage level $V_S > V_{S,UV,BLK}$ the TLE7269G continues with normal operation. A mode change only applies if the power supply V_S drops below the power on reset level ($V_S < V_{S,UV,PON}$).

If the power supply V_{IO} drops below the Under-Voltage level $V_{IO} > V_{IO,UV}$ the output and receiver stages will be disabled as well. When V_{IO} reaches a higher level as the Under-Voltage $V_{IO} > V_{IO,UV}$ level the TLE7269G continues with normal operation and data transmission.

4.11 TxD Time Out function

If the TxD1 or TxD2 signal is dominant for a time $t > t_{timeout}$ the TxD time-out function deactivates the transmission of the LIN signal to the bus and disables both, the output stage 1 and the output stage 2. This is realized to prevent the bus from being blocked by a permanent “Low” signal on the TxD1 or TxD2 pin, caused by an error on the external microcontroller (see **Figure 12**).

The transmission is released again, after a rising edge at TxD1 or TxD2 has been detected.

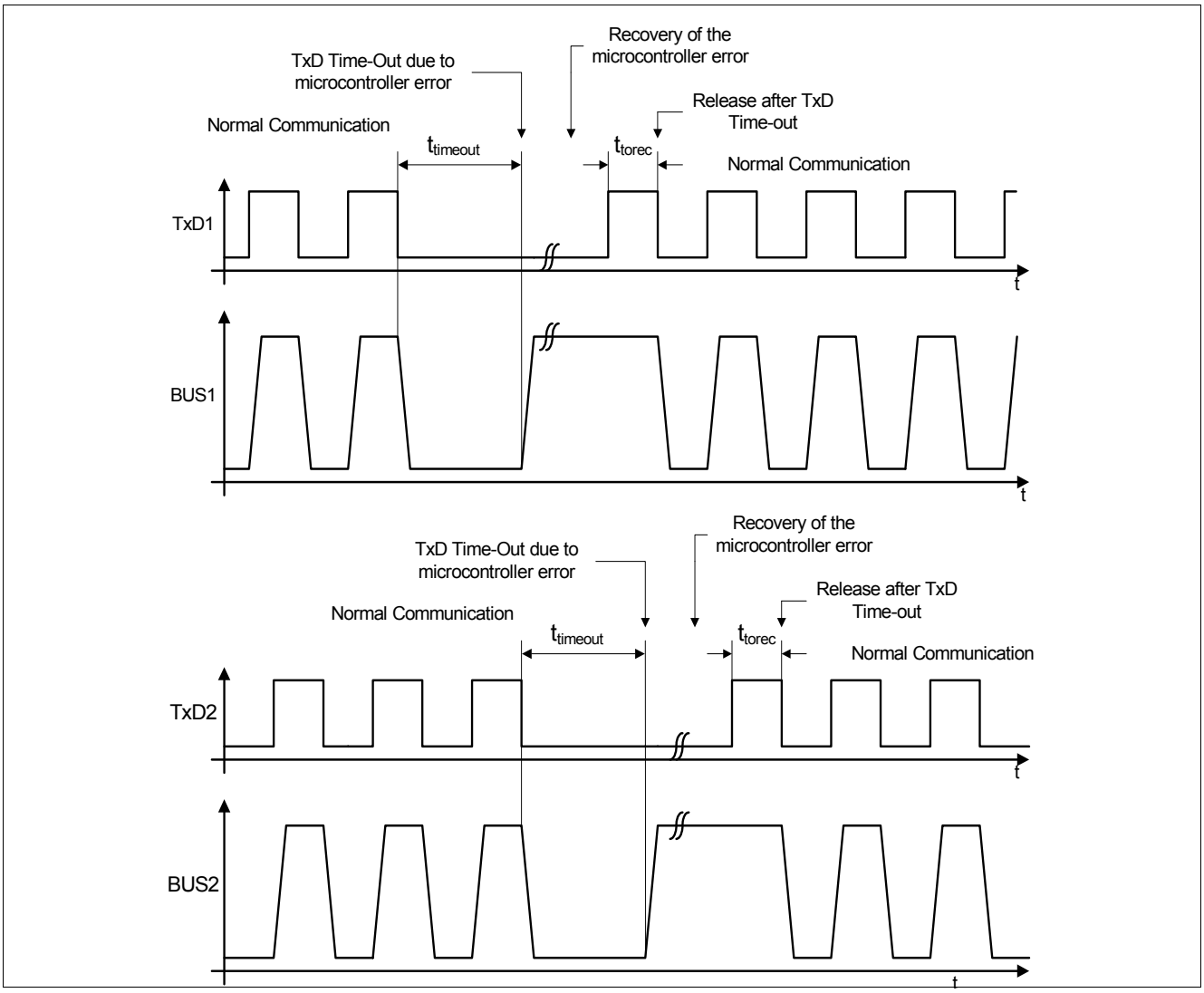


Figure 12 TxD Time-Out function

4.12 Over Temperature protection

The TLE7269G has one integrated over temperature sensor to protect the device against thermal overstress on the output stage 1 and output stage 2. In case of an over temperature event, the temperature sensor will disable both output stages (see **Figure 1**). An over temperature event will not cause any mode change nor will it be signaled by either the RxD pins or the TxD pins. When the junction temperature falls below the thermal shut down level $T_J < T_{jSD}$, the output stages are re-enabled and data communication can start again on BUS1 and BUS2. A 10°C hysteresis avoids toggling during the temperature shut down.

4.13 3.3 V and 5 V Logic Capability

The TLE7269G can be used for 3.3 V and 5 V microcontrollers. The inputs and the outputs are capable to operate with both voltage levels. The logic level is defined by suppling 3.3V or 5V to the V_{IO}. The inputs (TxD1, TxD2) take the reference voltage from the V_{IO} pin. The RxD1 output and RxD2 output are push-pull outputs, they work on the voltage given by V_{IO} pin. No external pull-up resistors are required.

The pin EN works without the voltage on the microcontroller supply V_{IO}. The TLE7269G can be set from Sleep mode to Normal Operation mode by setting EN to “High”, without supplying V_{IO}.

4.14 BUS Short to GND Feature

The TLE7269G has a feature implemented to protect the battery from running out of charge in the case of BUS short to GND failure.

In this failure case a normal master termination, a 1 kΩ resistor and diode between the LIN bus and the power supply V_S, would cause a constantly drawn current even in sleep mode. The resulting resistance of this short to GND is in the range 1 kΩ. To avoid this current during a generator off state, like in a parked car, the TLE7269G has a bus short to GND feature implemented, which is activated in Sleep mode.

This feature is only applicable, if the master termination of BUS1 is connected to INH1 pin and the master termination of BUS2 is connected to INH2 pin, instead of being connected to the power supply V_S (see **Figure 17** and **Figure 18**). Internally, the 30 kΩ path is also switched off from the power supply V_S (see **Figure 1**).

A separate Master Termination Switch is implemented at pins BUS1 and BUS2, to avoid a voltage drop on the recessive level of LIN bus, in case of a dominant level or a short to ground on at the LIN bus.

4.15 LIN Specifications 1.2, 1.3, 2.0 and 2.1

The device fulfills the Physical Layer Specification of LIN 1.2, 1.3, 2.0 and 2.1.

The differences between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The LIN specification 2.0 is a super set of the 1.3 version. The 2.0 version offers new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

In terms of the physical layer the LIN 2.1 Specification doesn’t include any changes and is fully compliant to the LIN Specification 2.0.

LIN 2.1 is the latest version of the LIN specification, released in December 2006.

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings[1)]

All voltages with respect to ground; positive current flowing into pin;

(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
Voltages						
5.1.1	Battery supply voltage	V_S	-0.3	40	V	LIN Spec 2.1 Param. 10
5.1.2	Logic supply voltage	V_{IO}	-0.3	5.5	V	–
5.1.3	Bus and WK input voltage versus GND versus V_S	 $V_{BUS,G}$ $V_{BUS,Vs}$	 -40 -40	 40 40	 V V	–
5.1.4	Logic voltages at EN, W2O, TxD1, TxD2, RxD1, RxD2	V_{logic}	-0.3	5.5	V	–
5.1.5	INH1, INH2 voltage versus GND versus V_S	 $V_{INH,G}$ $V_{INH,Vs}$	 -0.3 -40	 40 0.3	 V V	–
Currents						
5.1.6	Output current at INH1, INH2	I_{INH}	-150	80	mA	2)
Temperatures						
5.1.7	Junction temperature	T_j	-40	150	°C	–
5.1.8	Storage temperature	T_s	-55	150	°C	–
ESD Resistivity						
5.1.9	Electrostatic discharge voltage at V_S, BUS1, BUS2, WK versus GND	V_{ESD}	-6	6	kV	Human Body Model (100pF via 1.5 kΩ)[3)]
5.1.10	Electrostatic discharge voltage W2O versus V_S	V_{ESD}	-1	1	kV	Human Body Model (100pF via 1.5 kΩ)[3)]
5.1.11	Electrostatic discharge voltage all pins except W2O versus V_S	V_{ESD}	-2	2	kV	Human Body Model (100pF via 1.5 kΩ)[3)]

1) Not subject to production test, specified by design

2) Output current is internally limited to -150 mA

3) ESD susceptibility HBM according to EIA / JESD 22-A 114

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5.2 Functional Range

Table 5 Operating Range

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Supply voltages							
5.2.1	Supply Voltage Range for Normal Operation	$V_{S(nor)}$	7	–	27	V	LIN Spec 2.1 Param. 10
5.2.2	Extended Supply Voltage range for operation	$V_{S(ext)}$	5	–	40	V	Parameter deviations possible
5.2.3	Supply voltage V_{IO}	V_{IO}	3	–	5.5	V	–
Thermal parameters							
5.2.4	Junction temperature	T_j	-40	–	150	°C	1)

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

5.3 Thermal Characteristics

Table 6 Thermal Characteristics[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Thermal Resistance							
5.3.5	Junction to Soldering Point	R_{thJSP}	–	–	25	K/W	measured to pin 11
5.3.6	Junction to Ambient	R_{thJA}	–	130	–	K/W	2)
Thermal Shutdown Junction Temperature							
5.3.7	Thermal shutdown temp.	T_{jSD}	150	170	190	°C	–
5.3.8	Thermal shutdown hyst.	ΔT	–	10	–	K	–

1) Not subject to production test, specified by design

2) JESD 51-2, 51-3, FRA4 76,2 mm x 114,3 mm x 1,5 mm, 70 µm Cu, minimal footprint, Ta = 27°C

6 Electrical Characteristics

6.1 Functional Device Characteristics

Table 7 Electrical Characteristics

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{io} = 5V; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Current Consumption							
6.1.1	Current consumption at V_S(both channels recessive)	$I_{S,rec}$	0.5	1.6	3.0	mA	recessive state, without R_L; V_S = 13.5 V V_{TxD} = V_{io}
6.1.2	Current consumption normal mode at V_{io}	$I_{VIO,norm}$	–	10	50	µA	Normal Operation mode. V_{IO}=5 V
6.1.3	Current consumption at V_S (both channels dominant)	$I_{S,dom}$	–	3	5.0	mA	dominant state, without R_L; V_S = 13.5 V; V_{TxD} = 0 V
6.1.4	Current consumption in sleep mode at V_{io}	$I_{VIO,Sleep}$	–	1	10	µA	Sleep mode, V_{IO}=5 V
6.1.5	Current consumption in sleep mode	$I_{S,Sleep}$	–	7	12	µA	Sleep mode, V_S = 18 V; V_{BUS}= V_{WK} = V_S;
6.1.6	Current consumption in sleep mode	$I_{S,Sleep,typ}$	–	5	10	µA	Sleep mode, T_j < 85 °C; V_S = 13.5 V; V_{WK}= V_S= V_{BUS};
Under Voltage Detection							
6.1.7	Blocking under voltage detection at V_S (V_S on the falling edge)	$V_{s,UV,BLK}$	3.5	–	5	V	Communication blocked no reset (see **Figure 11**)
6.1.8	Power ON under voltage detection at V_S	$V_{s,UV,PON}$	–	–	3.5	V	Device reset to Stand-By-Mode [1](see **Figure 11**)
6.1.9	Under voltage detection at V_{IO}	$V_{IO,UV}$	1.5	2.5	3	V	Communication blocked no reset (see **Figure 11**)
6.1.10	Under voltage blanking time	$t_{blankUV}$	–	5	–	µs	[1]
Receiver Outputs: RxD1, RxD2							
6.1.11	HIGH level output current	$I_{RD,H}$	–10	-4	-2	mA	V_{RD} = 0.8 × V_{IO}
6.1.12	LOW level output current	$I_{RD,L}$	2	4	10	mA	V_{RD} = 0.2 × V_{IO}

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{io} = 5V; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Transmission Inputs: TxD1, TxD2							
6.1.13	HIGH level input voltage range	$V_{TD,H}$	0.7 × V_{IO}	–	V_{IO}	V	Recessive state
6.1.14	Input hysteresis	$V_{TD,hys}$	–	0.12 × V_{IO}	–	V	1)
6.1.15	LOW level input voltage range	$V_{TD,L}$	0	–	0.3 × V_{IO}	V	Dominant state
6.1.16	Pull-down resistance	R_{TD}	100	350	800	kΩ	V_{TxD} = V_{io}
6.1.17	Low level leakage current	I_{TD}	–	0	10	µA	V_{EN} = 0 V; V_{TxD} = 0 V
6.1.18	Dominant current standby mode after Wake-Up	$I_{TD,L}$	1.5	3	10	mA	V_{TxD} = 0.9 V; WK = 0 V; V_S = 13.5 V. Only valid for TxD 1
6.1.19	Input capacitance	Ci	–	5	–	pF	1)
W2O Input							
6.1.20	HIGH level input voltage range	$V_{W2O,H}$	0.7 × V_{IO}	–	V_{IO}	V	–
6.1.21	LOW level input voltage range	$V_{W2O,L}$	0	–	0.3 × V_{io}	V	–
6.1.22	Input hysteresis	$V_{W2O,hys}$	–	0.12 × V_{IO}	–	V	1)
6.1.23	Pull-down resistance	R_{W2O}	15	35	60	kΩ	–
6.1.24	Input Capacitance	Ci $_{W2O}$	–	5	–	pF	1)
Enable Input: EN							
6.1.25	HIGH level input voltage range	$V_{EN,on}$	2	–	V_{IO}	V	Normal Operation Mode
6.1.26	LOW level input voltage range	$V_{EN,off}$	0	–	0.8	V	Sleep Mode or Stand-By Mode
6.1.27	Input hysteresis	$V_{EN,hys}$		300		mV	1)
6.1.28	Pull-down resistance	R_{EN}	15	30	60	kΩ	–
6.1.29	Input capacitance	Ci $_{EN}$	–	5	–	pF	1)
Inhibit, Master Termination Outputs: INH1, INH2							
6.1.30	Inhibit R_{on} resistance	$R_{INH,on}$	22	36	50	Ω	I_{INH} = -15 mA
6.1.31	Maximum INH output current	I_{INH}	-150	–	-40	mA	V_{INH} = 0 V
6.1.32	Leakage current	$I_{INH,lk}$	-5.0	–	5.0	µA	Sleep Mode; V_{INH} = 0 V

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{io} = 5V; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
Wake Input: WK							
6.1.33	High level input voltage	$V_{WK,H}$	V_S - 1 V	–	V_S + 3 V	V	V_S = 13.5 V;
6.1.34	Low level input voltage	$V_{WK,L}$	-0.3	–	V_S - 4 V	V	V_S = 13.5 V;
6.1.35	Pull-up current	$I_{WK,PU}$	-60	-30	-3	µA	V_{WK} = 0V
6.1.36	High level leakage current	$I_{WK,H,leak}$	-5	–	5	µA	V_S = 0 V; V_{WK} = 40 V
6.1.37	Dominant time for wake-up	t_{WK}	30	–	150	µs	–
6.1.38	Input Capacitance	Ci_{WK}	–	15	–	pF	[1]
Bus Receiver: BUS1, BUS2							
6.1.39	Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.48 × V_S	–	V	–
6.1.40	Receiver dominant state	V_{BUSdom}	V_S - 40 V	–	0.4 × V_S	V	LIN Spec 2.1 (Par. 17) [2]
6.1.41	Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	–	0.52 × V_S	0.6 × V_S	V	–
6.1.42	Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 x V_s	V	LIN Spec 2.1 (Par. 18) [3]
6.1.43	Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	LIN Spec 2.1 (Par. 19) [4]
6.1.44	Receiver hysteresis	V_{HYS}	0.02 × V_S	0.04 × V_S	0.175 × V_S	V	LIN Spec 2.1 (Par. 20) [5]
6.1.45	Wake-up threshold voltage	$V_{BUS,wk}$	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–
6.1.46	Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	–
Bus Transmitter: BUS1, BUS2							
6.1.47	Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level
6.1.48	Bus dominant output voltage maximum load	$V_{BUS,do}$	– – –	– – –	1.2 0.2 x V_S 2.0	V V V	V_{TxD} = 0 V; R_L = 500 Ω 6,0 ≤ V_S ≤ 7,3 V; 7,3 < V_S ≤ 10 V; 10 < V_S ≤ 18 V; (see **Figure 14**)
6.1.49	Bus short circuit current	I_{BUS_LIM}	40	100	150	mA	V_{BUS} = 13.5 V; LIN Spec 2.1 (Par. 12);
6.1.50	Leakage current	$I_{BUS_NO_GND}$	-1000	-450	–	µA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.1 (Par. 15)
6.1.51	Leakage current	$I_{BUS_NO_BAT}$	–	2	8	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.1 (Par. 16)

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{io} = 5V; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
6.1.52	Leakage current	$I_{BUS_PAS_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.1 (Par. 13)
6.1.53	Leakage current	$I_{BUS_PAS_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.1 (Par. 14)
6.1.54	Bus pull-up resistance	R_{slave}	20	30	47	kΩ	Normal mode LIN Spec 2.1 (Par. 26)
6.1.55	LIN output current	I_{BUS}	-60	-30	-5	µA	Sleep mode V_S = 13.5 V; V_{EN} = 0 V
6.1.56	Input Capacitance	Ci_{BUS}	–	15	–	pF	1)
Dynamic Transceiver Characteristics: BUS1, BUS2							
6.1.57	Propagation delay LIN bus to RxD Dominant to RxD Low Recessive to RxD High	 t_{rx_pdf} t_{rx_pdr}	 – –	 1 1	 6 6	 µs µs	LIN Spec 2.1 (Par. 31) V_{io} = 5 V; C_{RxD} = 20 pF
6.1.58	Receiver delay symmetry	t_{rx_sym}	-2	–	2	µs	LIN Spec 2.1 (Par. 32) $t_{rx_sym} = t_{rx_pdf} - t_{rx_pdr}$; V_{io} = 5 V; C_{RxD} = 20 pF
6.1.59	Delay time for mode Change	t_{MODE}	–	–	120	µs	1) See **Figure 5**, **Figure 6**
6.1.60	TxD1 Setup time for mode selection	$t_{TXD,SET}$	–	–	50	µs	1) See **Figure 5**, **Figure 6**
6.1.61	TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V
6.1.62	TxD dominant time out recovery time	t_{torec}	–	–	15	µs	1)
6.1.63	EN toggling to enter the flash mode	t_{fl1}	25	35	50	µs	1) See **Figure 7**
6.1.64	TxD1 time for flash activation	t_{fl2} t_{fl3} t_{fl4}	5 10 10	– – –	– – –	µs	1) See **Figure 7**

Table 7 Electrical Characteristics (cont'd)

7.0 V < V_S < 27 V; R_L = 500 Ω; V_{io} = 5V; -40 °C < T_j < 125 °C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Pos.	Parameter	Symbol	Limit Values			Unit	Remarks
			Min.	Typ.	Max.		
6.1.65	Duty cycle D1 (for worst case at 20 kBit/s)	D1	0.396	–	–	–	duty cycle 1 [6] TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) =0.581 × V_S; V_S = 7.0 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 27)
6.1.66	Duty cycle D2 (for worst case at 20 kBit/s)	D2	–	–	0.581	–	duty cycle 2 [6] TH_{Rec}(min)= 0.422 × V_S; TH_{Dom}(min)= 0.284 × V_S V_S = 7.6 … 18 V; t_{bit} = 50 µs; D2 = $t_{bus_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 28)
6.1.67	Duty cycle D3 (for worst case at 10.4 kBit/s) Low Slope Mode	D3	0.417	–	–	–	duty cycle 3 [6] TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) =0.616 × V_S V_S = 7.0 … 18 V; t_{bit} = 96µs; D3 = $t_{bus_rec(min)}$/2 t_{bit}; LIN Spec 2.1 (Par. 29)
6.1.68	Duty cycle D4 (for worst case at 10.4 kBit/s) Low Slope Mode	D4	–	–	0.590	–	duty cycle 4 [6] TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) =0.251 × V_S V_S = 7.6 … 18 V; t_{bit} = 96µs; D4 = $t_{bus_rec(max)}$/2 t_{bit}; LIN Spec 2.1 (Par. 30)

1) Not subject to production test, specified by design
2) Minimum limit specified by design
3) Maximum limit specified by design
4) $V_{BUS_CNT} = (V_{th_dom} - V_{th\ rec})/2;$
5) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
6) Bus load concerning LIN Spec 2.1:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6,8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}

6.2 Diagrams

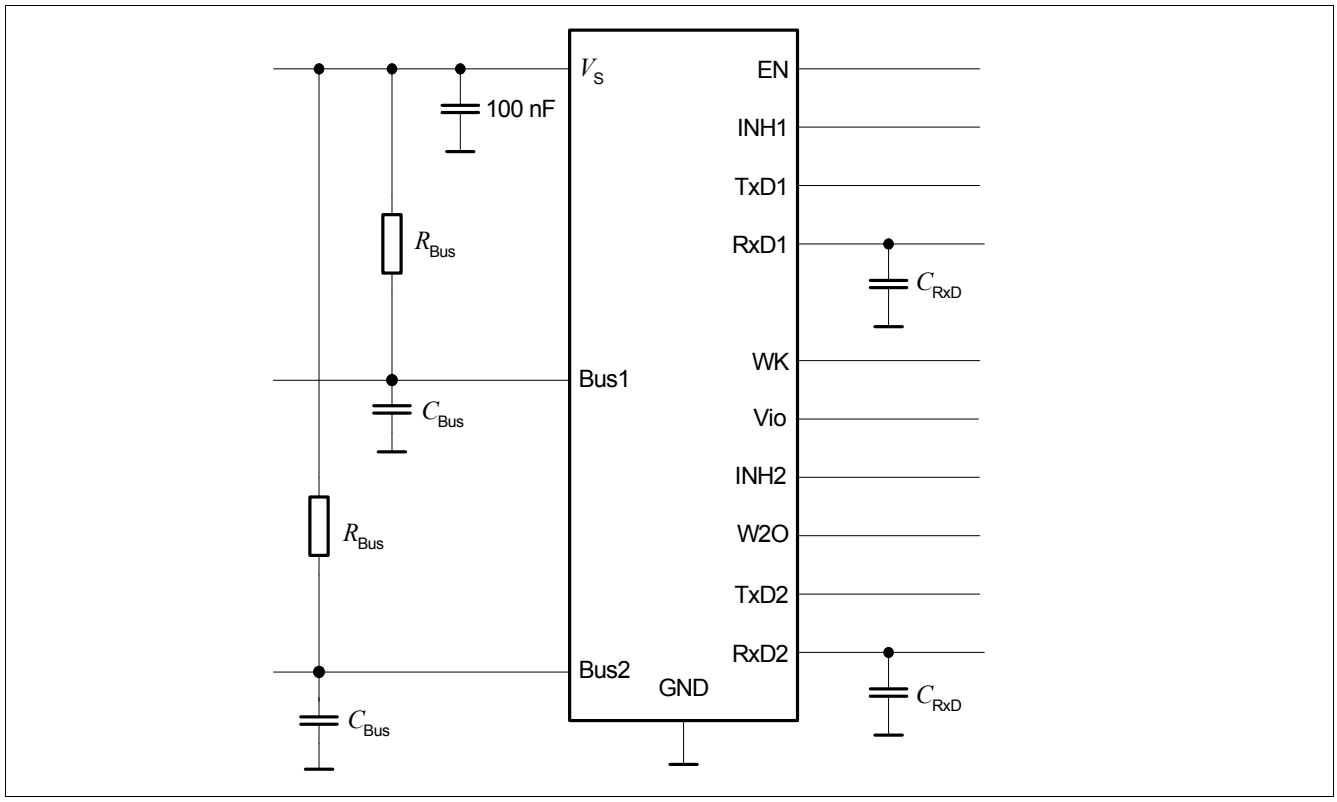


Figure 13 Simplified test circuit for dynamic characteristics

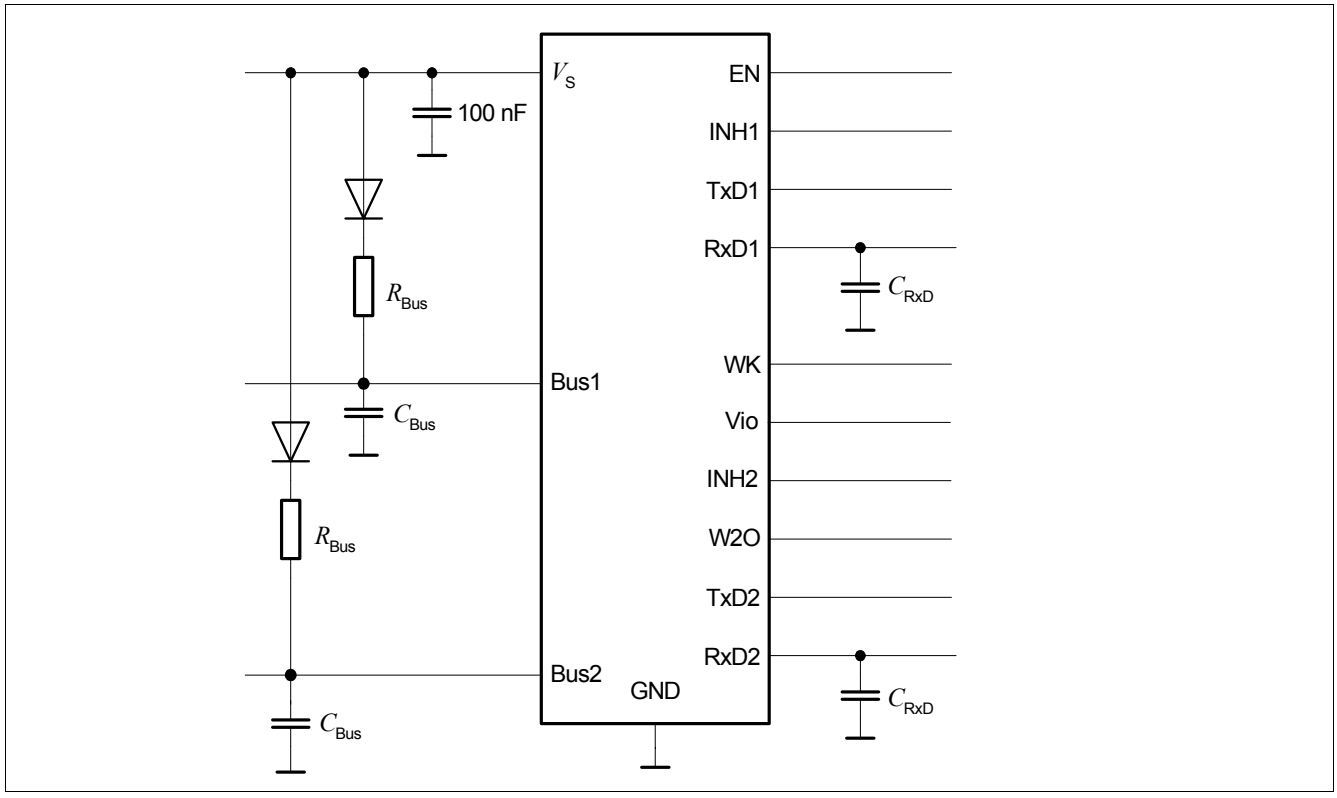


Figure 14 Simplified test circuit for static characteristics

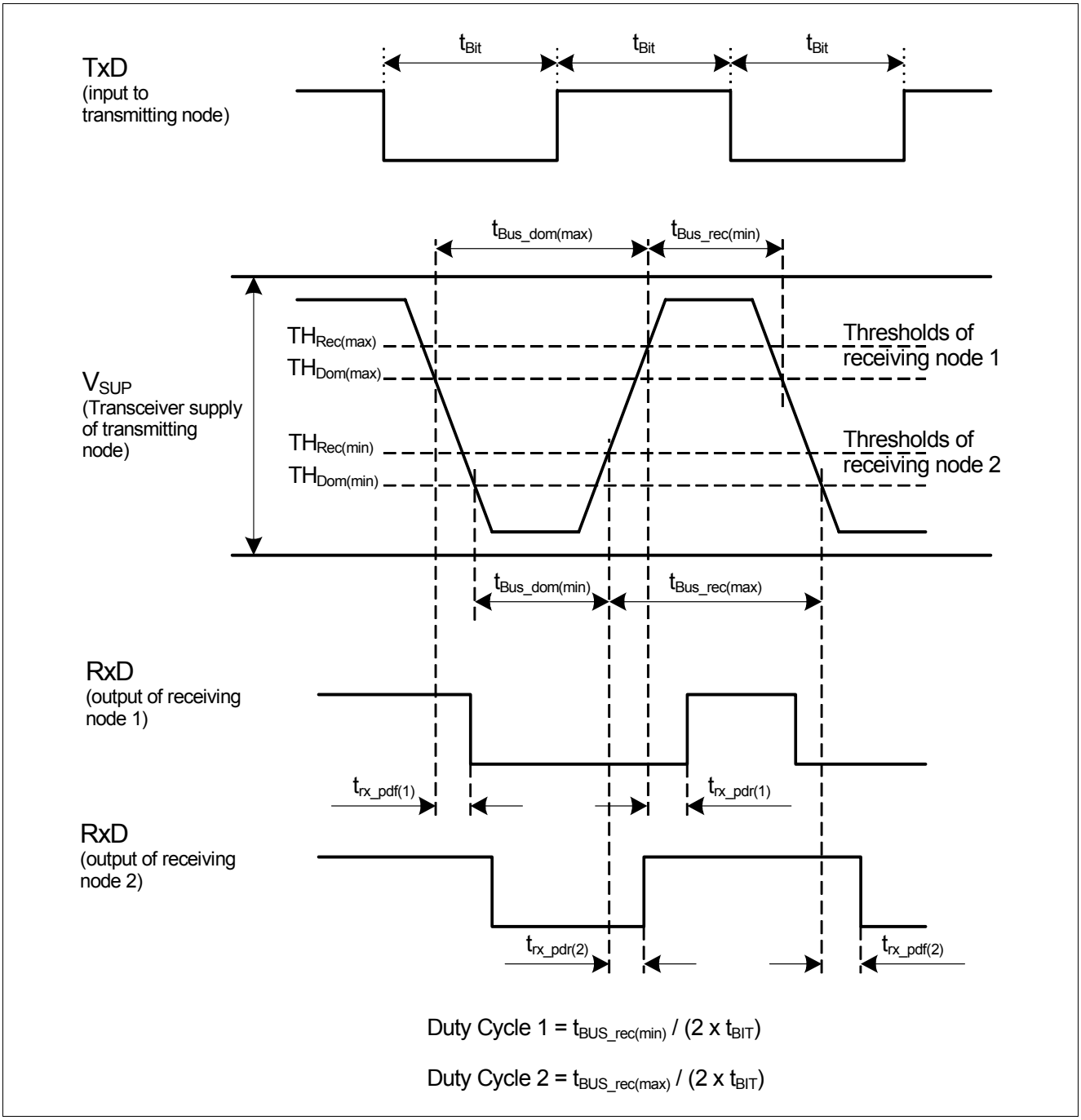


Figure 15 Timing diagram for dynamic characteristics

7 Application Information

7.1 ESD Robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 8 ESD Robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, BUS1 and BUS2 versus GND	≥ +9	kV	1)Positive pulse
Electrostatic discharge voltage at pin V_S, BUS1 and BUS2 versus GND	≤ -9	kV	1)Negative pulse
Electrostatic discharge voltage at pin WK versus GND	≥ +8	kV	1)Positive pulse
Electrostatic discharge voltage at pin WK versus GND	≤ -8	kV	1)Negative pulse

1) ESD susceptibility “ESD GUN” according LIN EMC 1.3 Test Specification, Section 4.3. (IEC 61000-4-2) -Tested by external test house (IBEE Zwickau, EMC Testreport Nr. 05-06-06).

7.2 Pin Compatibility to the Single LIN Transceivers

The Twin LIN Transceiver TLE7269G is pin and function compatible to the Single LIN Transceivers like the TLE7259G, the TLE7259-2GE and its derivative the TLE7259-2GU. The TLE7269G has a pin for the V_{IO} supply. This supply pin is usually connected to the power supply of the external microcontroller. The TLE7259G and the TLE7259-2GE/U don’t have a V_{IO} pin. In order to provide the same functions on the TLE7259G and TLE7259-2GE/GU, these two LIN transceiver need an external pull-up resistor between the RxD pin and the microcontroller supply.

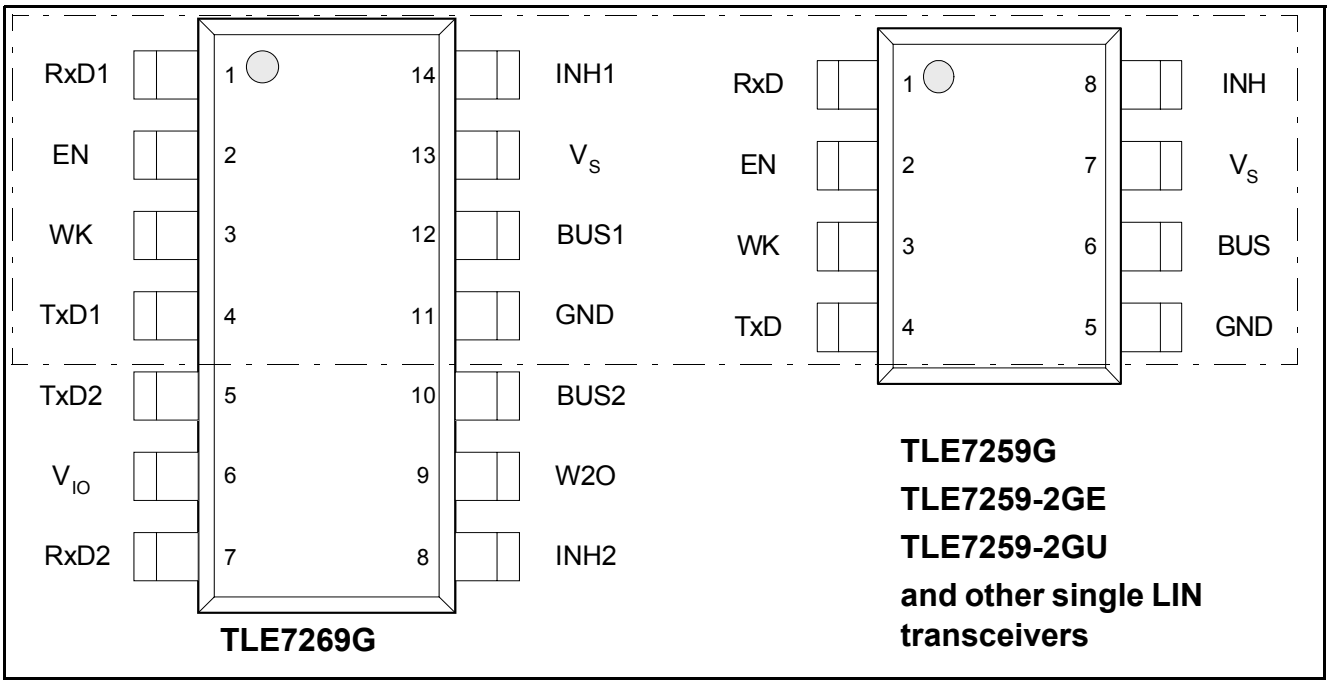


Figure 16 Pin configuration TLE7269G and TLE7259G, TLE7259-2GE/GU

7.3 Master Termination

To achieve the required timings for the dominant to recessive transition of the bus signal an additional external termination resistor of 1 kΩ is mandatory. It is recommended to place this resistor at the master node. To avoid reverse currents from the bus line into the battery supply line it is recommended to place a diode in series with the external pull-up. For small systems (low bus capacitance) the EMC performance of the system is supported by an additional capacitor of at least 1 nF at the master node (see **Figure 17** and **Figure 18**).The values for the Master Termination resistor and the bus capacitance influence the performance of the LIN network. They depend on the number of nodes inside the LIN network and on the parasitic cable capacitances of the LIN bus wiring.

7.4 External Capacitors

A capacitor of 10 µF at the supply voltage input V_S buffers the input voltage. In combination with the required reverse polarity diode this prevents the device from detecting a power down conditions in case of negative transients on the supply line (see **Figure 17** and **Figure 18**).

The 100 nF capacitor close to the V_S pin and a 33 nF capacitor close to the V_{IO} pin of the TLE7269G are required to get the best EMC performance.

7.5 Application Example

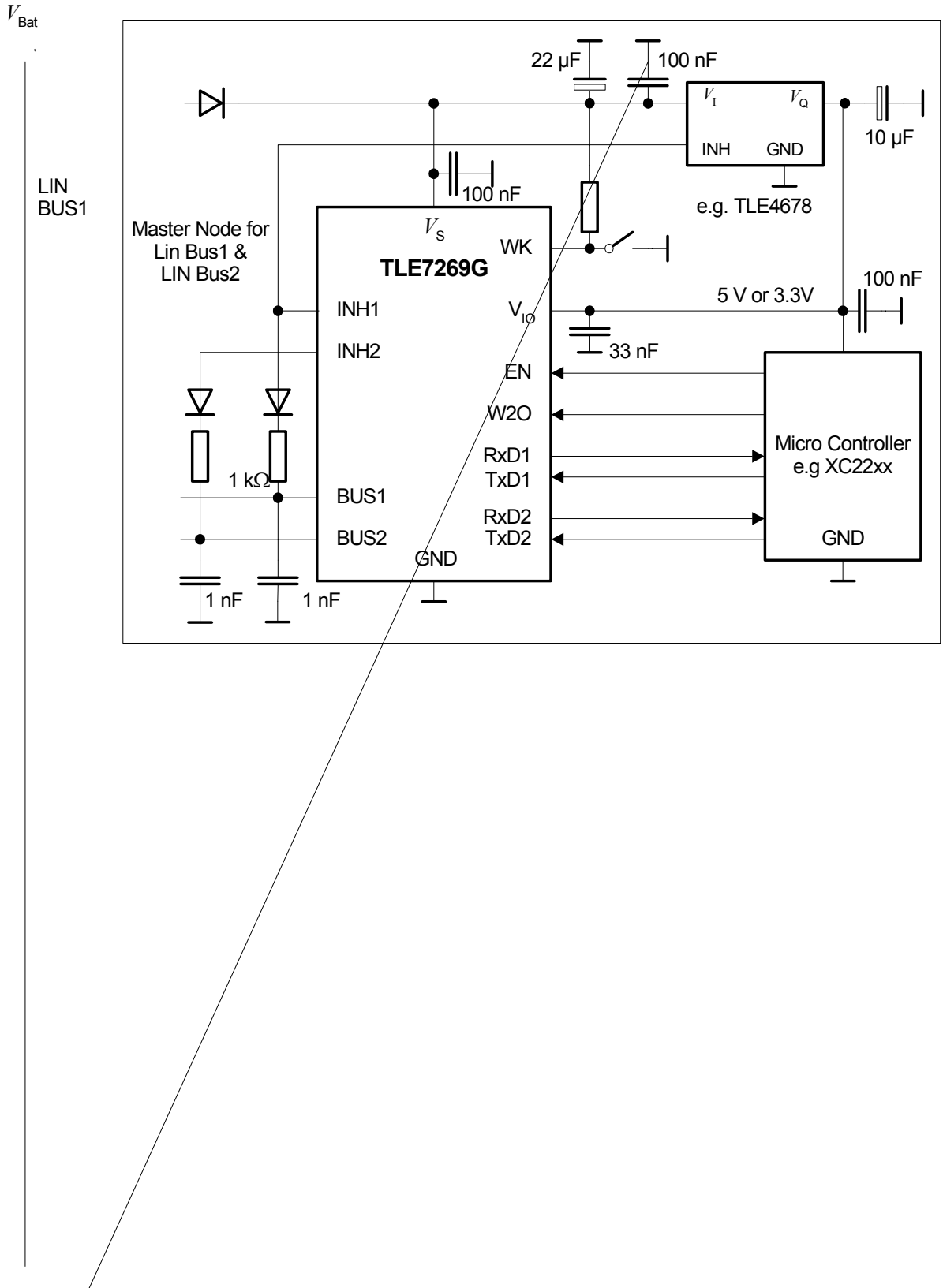


Figure 17 Simplified Application Circuit with Bus Short to GND Feature applied

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9 Revision History

Revision	Date	Changes
1.2	2007-10-02	Data Sheet created