

XMC1300

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM[®] Cortex[™]-M0
32-bit processor core

Data Sheet

V1.1 2013-10

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Revision History: V1.1 2013-10

Previous Versions:

Page	Subjects
Page 36	Flash Memory Parameters chapter has been moved to be a sub-section in the DC Parameter.
Page 55	Table 31 is updated to enhance the presentation. A new parameter, Moisture sensitivity level, is added.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc1000> to get access to the latest versions of those documents.

1 Summary of Features

The XMC1300 devices are members of the XMC1000 family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1300 series addresses the real-time control needs of motor control, digital power conversion. It also features peripherals for LED Lighting applications.

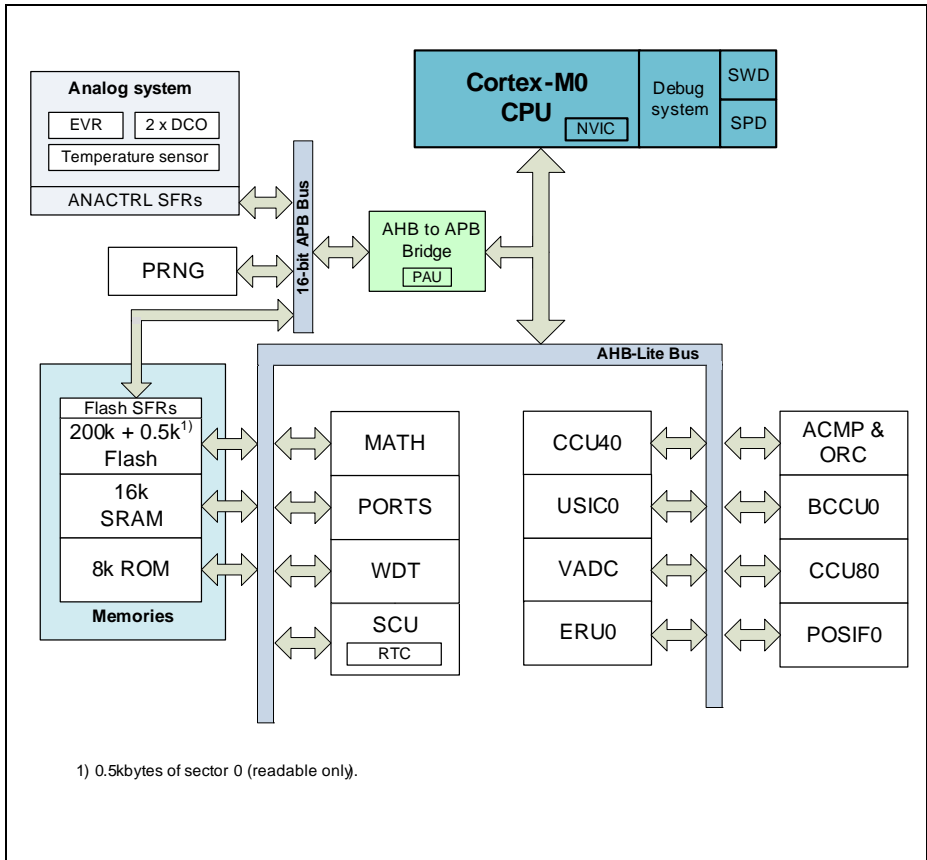


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M0 CPU
 - Most of 16-bit Thumb instruction set

Summary of Features

- Subset of 32-bit Thumb2 instruction set
- High code density with 32-bit performance
- Single cycle 32-bit hardware multiplier
- System timer (SysTick) for Operating System support
- Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- MATH Co-processor (MATH), consists of a CORDIC unit for trigonometric calculation and a division unit

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces

Analog Frontend Peripherals

- A/D Converters, up to 12 channels, includes 2 sample and hold stages and a fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Position Interfaces (POSIF) for hall and quadrature encoders and motor positioning
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG), provides random data with fast generation times

Input/Output Lines With Individual Bit Controllability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Configurable pad hysteresis

Debug System

- Access through the standard ARM serial wire debug (SWD) or the single pin debug (SPD) interface
- A breakpoint unit (BPU) supporting up to 4 hardware breakpoints
- A watchpoint unit (DWT) supporting up to 2 watchpoints

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code "XMC1<DDD>-<Z><PPP><T><FFFF>" identifies:

- <DDD> the derivatives function set
- <Z> the package variant
 - T: TSSOP
 - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
 - F: -40°C to 85°C
 - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see [Table 1](#).

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XMC1300 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16

Summary of Features

Table 1 Synopsis of XMC1300 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T038F0008	PG-TSSOP-38-9	8	16
XMC1301-T038F0016	PG-TSSOP-38-9	16	16
XMC1301-T038F0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0016	PG-TSSOP-38-9	16	16
XMC1302-T038X0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0200	PG-TSSOP-38-9	200	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1300 Device Types¹⁾

Derivative	ADC channel	ACMP	BCCU	MATH
XMC1301-T016	6	2	-	-
XMC1301-T038	12	3	-	-
XMC1302-T038	12	3	1	1

1) Features that are not included in this table are available in all the derivatives

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 bytes value with the most significant 7 bytes stored in Flash configuration sector 0 (CS0) at address location : 1000 0F00_H (MSB) - 1000 0F1B_H (LSB). The least significant byte of the Chip Identification Number is the value of register DBGROMID.

Table 3 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00003000 101ED083 _H	AA

Summary of Features

Table 3 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00005000 101ED083 _H	AA
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00009000 101ED083 _H	AA
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00011000 101ED083 _H	AA
XMC1302-T038X0200	00013013 01FF00FF 00001FF7 0000900F 00000B00 00001000 00033000 101ED083 _H	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

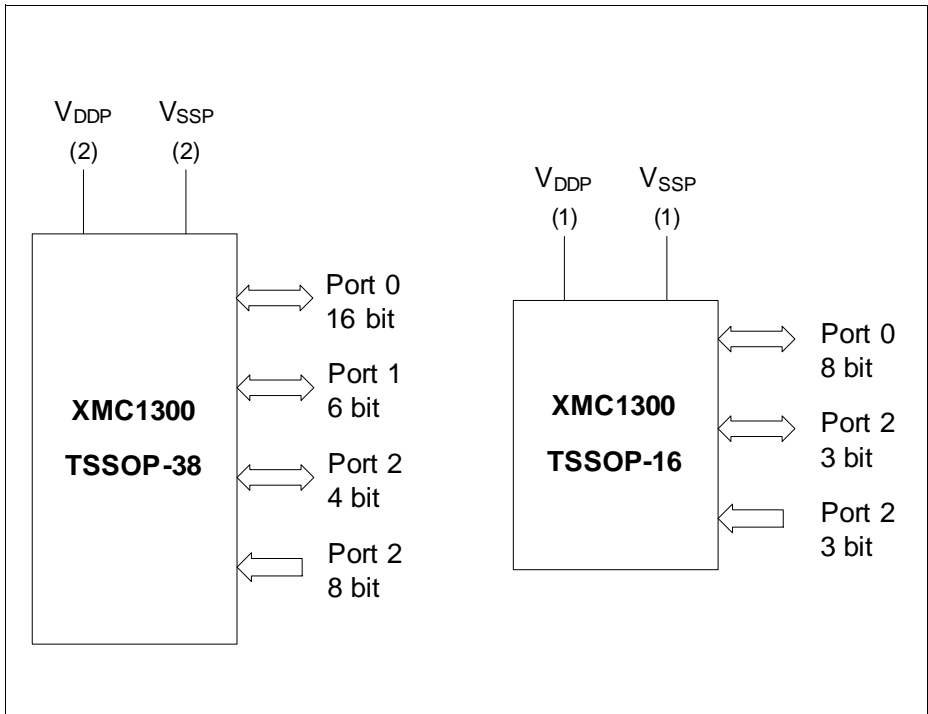


Figure 2 XMC1300 Logic Symbol for TSSOP-38 and TSSOP-16

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

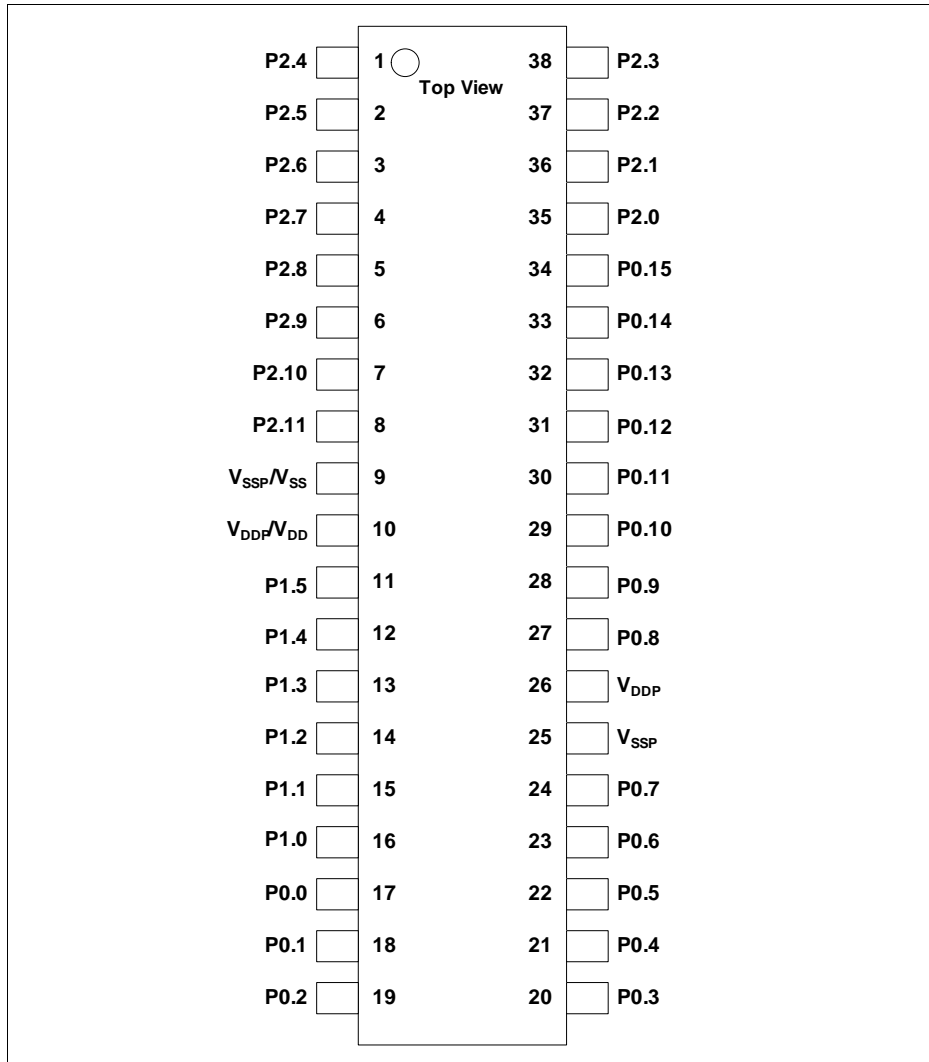


Figure 3 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

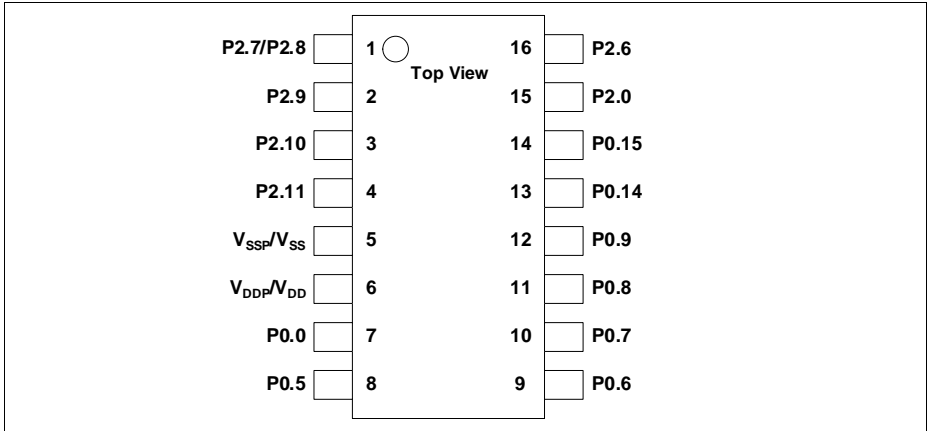


Figure 4 XMC1300 PG-TSSOP-16 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 4 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 5 Package Pin Mapping

Function	TSSOP 38	TSSOP 16	Pad Type	Notes
P0.0	17	7	STD_INOUT	
P0.1	18	-	STD_INOUT	
P0.2	19	-	STD_INOUT	
P0.3	20	-	STD_INOUT	
P0.4	21	-	STD_INOUT	
P0.5	22	8	STD_INOUT	
P0.6	23	9	STD_INOUT	
P0.7	24	10	STD_INOUT	
P0.8	27	11	STD_INOUT	
P0.9	28	12	STD_INOUT	
P0.10	29	-	STD_INOUT	
P0.11	30	-	STD_INOUT	
P0.12	31	-	STD_INOUT	

General Device Information

Table 5 Package Pin Mapping (cont'd)

Function	TSSOP 38	TSSOP 16	Pad Type	Notes
P0.13	32	-	STD_INOUT	
P0.14	33	13	STD_INOUT	
P0.15	34	14	STD_INOUT	
P1.0	16	-	High Current	
P1.1	15	-	High Current	
P1.2	14	-	High Current	
P1.3	13	-	High Current	
P1.4	12	-	High Current	
P1.5	11	-	High Current	
P2.0	35	15	STD_INOUT/AN	
P2.1	36	-	STD_INOUT/AN	
P2.2	37	-	STD_IN/AN	
P2.3	38	-	STD_IN/AN	
P2.4	1	-	STD_IN/AN	
P2.5	2	-	STD_IN/AN	
P2.6	3	16	STD_IN/AN	
P2.7	4	1	STD_IN/AN	
P2.8	5	1	STD_IN/AN	
P2.9	6	2	STD_IN/AN	
P2.10	7	3	STD_INOUT/AN	
P2.11	8	4	STD_INOUT/AN	
VSS	9	5	Power	Supply GND, ADC reference GND
VDD	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VSSP	25	-	Power	I/O port ground
VDDP	26	-	Power	I/O port supply

2.2.2 Port I/O Functions

The following general building block is used to describe each PORT pin:

Table 6 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 7 Port I/O Functions

Function	Outputs							Inputs															
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input			
P0.0	ERU0. PDOU0		ERU0. GOUT0	CCU40. OUT0	CCU80. OUT00	USIC0_CH0 SELO0	USIC0_CH1 SELO0					BCCU0. TRAPINB	CCU40. IN0C			USIC0_CH0 DX2A	USIC0_CH1 DX2A						
P0.1	ERU0. PDOU1		ERU0. GOUT1	CCU40. OUT1	CCU80. OUT01	BCCU0. OUT8	SCU. VDROP						CCU40. IN1C										
P0.2	ERU0. PDOU2		ERU0. GOUT2	CCU40. OUT2	CCU80. OUT02	VADC0. EMUX02	CCU80. OUT10						CCU40. IN2C										
P0.3	ERU0. PDOU3		ERU0. GOUT3	CCU40. OUT3	CCU80. OUT03	VADC0. EMUX01	CCU80. OUT11						CCU40. IN3C										
P0.4	BCCU0. OUT0			CCU40. OUT1	CCU80. OUT13	VADC0. EMUX00	WWDT. SERVICE_ OUT						CCU80. IN0B										
P0.5	BCCU0. OUT1			CCU40. OUT0	CCU80. OUT12	ACMP2. OUT	CCU80. OUT01						CCU80. IN1B										
P0.6	BCCU0. OUT2			CCU40. OUT0	CCU80. OUT11	USIC0_CH1 MCLKOUT	USIC0_CH1 DOU0						CCU40. IN0B			USIC0_CH1 DX0C							
P0.7	BCCU0. OUT3			CCU40. OUT1	CCU80. OUT10	USIC0_CH0 SCLKOUT	USIC0_CH1 DOU0						CCU40. IN1B			USIC0_CH0 DX1C	USIC0_CH1 DX0D	USIC0_CH1 DX1C					
P0.8	BCCU0. OUT4			CCU40. OUT2	CCU80. OUT20	USIC0_CH0 SCLKOUT	USIC0_CH1 SCLKOUT						CCU40. IN2B			USIC0_CH0 DX1B	USIC0_CH1 DX1B						
P0.9	BCCU0. OUT5			CCU40. OUT3	CCU80. OUT21	USIC0_CH0 SELO0	USIC0_CH1 SELO0						CCU40. IN3B			USIC0_CH0 DX2B	USIC0_CH1 DX2B						
P0.10	BCCU0. OUT6			ACMP0. OUT	CCU80. OUT22	USIC0_CH0 SELO1	USIC0_CH1 SELO1						CCU80. IN2B			USIC0_CH0 DX2C	USIC0_CH1 DX2C						
P0.11	BCCU0. OUT7			USIC0_CH0 MCLKOUT	CCU80. OUT23	USIC0_CH0 SELO2	USIC0_CH1 SELO2									USIC0_CH0 DX2D	USIC0_CH1 DX2D						
P0.12	BCCU0. OUT8				CCU80. OUT33	USIC0_CH0 SELO3	CCU80. OUT20					BCCU0. TRAPINA	CCU40. IN0A	CCU40. IN1A	CCU40. IN2A	CCU40. IN3A	CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A		USIC0_CH0 DX2E	
P0.13	WWDT. SERVICE_ OUT				CCU80. OUT32	USIC0_CH0 SELO4	CCU80. OUT21					CCU80. IN3B	POSIF0. IN0B			USIC0_CH0 DX2F							
P0.14	BCCU0. OUT7				CCU80. OUT31	USIC0_CH0 DOU0	USIC0_CH0 SCLKOUT						POSIF0. IN1B			USIC0_CH0 DX0A	USIC0_CH0 DX1A						
P0.15	BCCU0. OUT8				CCU80. OUT30	USIC0_CH0 DOU0	USIC0_CH1 MCLKOUT						POSIF0. IN2B			USIC0_CH0 DX0B							
P1.0	BCCU0. OUT0	CCU40. OUT0			CCU80. OUT00	ACMP1. OUT	USIC0_CH0 DOU0		USIC0_CH0 DOU0	USIC0_CH0 HWI0			POSIF0. IN2A			USIC0_CH0 DX0C							
P1.1	VADC0. EMUX00	CCU40. OUT1			CCU80. OUT01	USIC0_CH0 DOU0	USIC0_CH1 SELO0		USIC0_CH0 DOU1	USIC0_CH0 HWI1			POSIF0. IN1A			USIC0_CH0 DX0D	USIC0_CH0 DX1D	USIC0_CH1 DX2E					
P1.2	VADC0. EMUX01	CCU40. OUT2			CCU80. OUT10	ACMP2. OUT	USIC0_CH1 DOU0		USIC0_CH0 DOU2	USIC0_CH0 HWI2			POSIF0. IN0A			USIC0_CH1 DX0B							
P1.3	VADC0. EMUX02	CCU40. OUT3			CCU80. OUT11	USIC0_CH1 SCLKOUT	USIC0_CH1 DOU0		USIC0_CH0 DOU3	USIC0_CH0 HWI3						USIC0_CH1 DX0A	USIC0_CH1 DX1A						
P1.4	VADC0. EMUX10	USIC0_CH1 SCLKOUT			CCU80. OUT20	USIC0_CH0 SELO0	USIC0_CH1 SELO1									USIC0_CH0 DX0E	USIC0_CH1 DX0E						
P1.5	VADC0. EMUX11	USIC0_CH0 DOU0		BCCU0. OUT1	CCU80. OUT21	USIC0_CH0 SELO1	USIC0_CH1 SELO1									USIC0_CH1 DX0F							

Table 7 Port I/O Functions (cont'd)

Function	Outputs								Inputs													
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU80. OUT20	USIC0_CH0 DOUT0	USIC0_CH0 SCLKOUT						VADC0. G0CH5		ERU0.0B0	USIC0_CH0 DX0E	USIC0_CH0 DX1E	USIC0_CH1 DX2F				
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU80. OUT21	USIC0_CH0 DOUT0	USIC0_CH1 SCLKOUT					ACMP2.INP	VADC0. G0CH6		ERU0.1B0	USIC0_CH0 DX0F	USIC0_CH1 DX3A	USIC0_CH1 DX4A				
P2.2												ACMP2.INN	VADC0. G0CH7		ERU0.0B1	USIC0_CH0 DX3A	USIC0_CH0 DX4A	USIC0_CH1 DX5A	ORC0.AIN			
P2.3													VADC0. G1CH5		ERU0.1B1	USIC0_CH0 DX5B	USIC0_CH1 DX3C	USIC0_CH1 DX4C	ORC1.AIN			
P2.4													VADC0. G1CH6		ERU0.0A1	USIC0_CH0 DX3B	USIC0_CH0 DX4B	USIC0_CH1 DX5B	ORC2.AIN			
P2.5													VADC0. G1CH7		ERU0.1A1	USIC0_CH0 DX3D	USIC0_CH1 DX3E	USIC0_CH1 DX4E	ORC3.AIN			
P2.6												ACMP1.INN	VADC0. G0CH0		ERU0.2A1	USIC0_CH0 DX3E	USIC0_CH0 DX4E	USIC0_CH1 DX5D	ORC4.AIN			
P2.7												ACMP1.INP	VADC0. G1CH1		ERU0.3A1	USIC0_CH0 DX3C	USIC0_CH1 DX3D	USIC0_CH1 DX4D	ORC5.AIN			
P2.8												ACMP0.INN	VADC0. G0CH1	VADC0. G1CH0	ERU0.3B1	USIC0_CH0 DX3D	USIC0_CH0 DX4D	USIC0_CH1 DX5C	ORC6.AIN			
P2.9												ACMP0.INP	VADC0. G0CH2	VADC0. G1CH4	ERU0.3B0	USIC0_CH0 DX5A	USIC0_CH1 DX3B	USIC0_CH1 DX4B	ORC7.AIN			
P2.10	ERU0. PDOUT1	CCU40. OUT2	ERU0. GOUT1		CCU80. OUT30	ACMP0. OUT	USIC0_CH1 DOUT0						VADC0. G0CH3	VADC0. G1CH2	ERU0.2B0	USIC0_CH0 DX3C	USIC0_CH0 DX4C	USIC0_CH1 DX0F				
P2.11	ERU0. PDOUT0	CCU40. OUT3	ERU0. GOUT0		CCU80. OUT31	USIC0_CH1 SCLKOUT	USIC0_CH1 DOUT0					ACMP.REF	VADC0. G0CH4	VADC0. G1CH3	ERU0.2B1	USIC0_CH1 DX0E	USIC0_CH1 DX1E					

3 Electrical Parameter

This section provides the electrical parameter which are implementation-specific for the XMC1300.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_S	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on any pin with respect to V_{SSP}	V_{IN}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower
Voltage on any analog input pin with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	$V_{DDP} + 0.5$ or max. 6	V	–
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	SR	–	–	50	mA	–
Analog comparator input voltage	V_{CM}	SR	-0.3	–	$V_{DDP} + 0.3$	V	

3.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 9 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	105	°C	Temp. Range X
Digital supply voltage ¹⁾	V_{DDP} SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK} CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK} CC	–	–	66.4	MHz	Peripherals clock

1) See also the Supply Monitoring thresholds, [Chapter 3.3.3](#).

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 10 provides the characteristics of the input/output pins of the XMC1300.

Table 10 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values	Unit	Test Conditions	
					Min.
Output low voltage on port pins (with standard pads)	V_{OLP} CC	–	1.0	V	$I_{OL} = 11$ mA (5 V) $I_{OL} = 7$ mA (3.3 V)
		–	0.4	V	$I_{OL} = 5$ mA (5 V) $I_{OL} = 3.5$ mA (3.3 V)
Output low voltage on high current pads	V_{OLP1} CC	–	1.0	V	$I_{OL} = 50$ mA (5 V) $I_{OL} = 25$ mA (3.3 V)
		–	0.32	V	$I_{OL} = 10$ mA (5 V)
		–	0.4	V	$I_{OL} = 5$ mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP} CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -10$ mA (5 V) $I_{OH} = -7$ mA (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4.5$ mA (5 V) $I_{OH} = -2.5$ mA (3.3 V)
Output high voltage on high current pads	V_{OHP1} CC	$V_{DDP} - 0.32$	–	V	$I_{OH} = -6$ mA (5 V)
		$V_{DDP} - 1.0$	–	V	$I_{OH} = -8$ mA (3.3 V)
		$V_{DDP} - 0.4$	–	V	$I_{OH} = -4$ mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS} SR	–	$0.19 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS} SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL} SR	–	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾

Electrical Parameter
Table 10 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	$0.85 \times V_{DDP}$	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ³⁾
Input Hysteresis ¹⁾	HYS	CC	$0.08 \times V_{DDP}$	–	V	CMOS Mode (5 V), Standard Hysteresis
			$0.03 \times V_{DDP}$	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			$0.02 \times V_{DDP}$	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			$0.5 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(5 V), Large Hysteresis
			$0.4 \times V_{DDP}$	$0.75 \times V_{DDP}$	V	CMOS Mode(3.3 V), Large Hysteresis
			$0.2 \times V_{DDP}$	$0.65 \times V_{DDP}$	V	CMOS Mode(2.2 V), Large Hysteresis
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current ²⁾	I_{OZP}	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105^\circ C$
Overload current on any pin	I_{OVP}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma I_{OVP} $	SR	–	25	mA	³⁾
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	⁴⁾
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high current pins	I_{MP1A}	SR	-8	50	mA	–
Maximum current into V_{DDP} (TSSOP28/16)	I_{MVDD1}	SR	–	130	mA	³⁾

Electrical Parameter

Table 10 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current into V_{DDP} (TSSOP38)	I_{MVDD2}	SR	–	260	mA	³⁾
Maximum current out of V_{SS} (TSSOP28/16)	I_{MVSS1}	SR	–	130	mA	³⁾
Maximum current out of V_{SS} (TSSOP38)	I_{MVSS2}	SR	–	260	mA	³⁾

- 1) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
- 3) Not subject to production test, verified by design/characterization.
- 4) Not subject to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

3.2.2 Analog to Digital Converters (ADC)

Table 11 shows the Analog to Digital Converter (ADC) characteristics.

Table 11 ADC Characteristics (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	1.8	–	3.0	V	SHSCFG.AREF = 11 _B
		3.0	–	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground (SH0-CH0, SH1-CH0)	V_{REFGND} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Internal reference voltage (full scale value)	V_{REFINT} CC	4.82	5	5.18	V	-40°C - 105°C
		4.9	5	5.1	V	0°C - 85°C ¹⁾
Switched capacitance of an analog input ¹⁾	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	¹⁾
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	¹⁾

Electrical Parameter
Table 11 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTR _{xz} .GAIN _y = 00 _B (unity gain)
		3			–	GNCTR _{xz} .GAIN _y = 01 _B (gain g1)
		6			–	GNCTR _{xz} .GAIN _y = 10 _B (gain g2)
		12			–	GNCTR _{xz} .GAIN _y = 11 _B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	$V_{DDP} = 5.0$ V
		3	–	–	1 / f_{ADC}	$V_{DDP} = 3.3$ V
		30	–	–	1 / f_{ADC}	$V_{DDP} = 1.8$ V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	²⁾
Conversion time in 12-bit mode	t_{C12} CC	22			1 / f_{ADC}	²⁾
Maximum sample rate in 12-bit mode	f_{C12} CC	–	–	$f_{ADC} / 33$	–	1 sample pending
		–	–	$f_{ADC} / 53$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	20			1 / f_{ADC}	²⁾
Maximum sample rate in 10-bit mode	f_{C10} CC	–	–	$f_{ADC} / 31$	–	1 sample pending
		–	–	$f_{ADC} / 49$	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	18			1 / f_{ADC}	²⁾

Electrical Parameter

Table 11 ADC Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode	f_{C8} CC	–	–	$f_{ADC} / 29$	–	1 sample pending
		–	–	$f_{ADC} / 45$	–	2 samples pending
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00 _B (calibrated)
Gain error with internal reference	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = 1X _B (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = 1X _B (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±6.0	–	LSB 12	Calibrated

- 1) Not subject to production test, verified by design/characterization.
- 2) No pending samples assumed, excluding sampling time and calibration.

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference (V_{AREF}) on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 12 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP} = 3.0\text{ V} - 5.5\text{ V}$)

Parameter	Symbol	CC	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	60	-	120	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	25	-	V_{ODC}	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	-	-	ns	$V_{AIN} \geq V_{AREF} + 150\text{ mV}$
			88	-	-	ns	$V_{AIN} \geq V_{AREF} + 350\text{ mV}$
Never detected Overvoltage Pulse	t_{OPDN}	CC	-	-	21	ns	$V_{AIN} \geq V_{AREF} + 150\text{ mV}$
			-	-	11	ns	$V_{AIN} \geq V_{AREF} + 350\text{ mV}$
Detection Delay	t_{ODD}	CC	39	-	132	ns	$V_{AIN} \geq V_{AREF} + 150\text{ mV}$
			31	-	121	ns	$V_{AIN} \geq V_{AREF} + 350\text{ mV}$
Release Delay	t_{ORD}	CC	44	-	240	ns	$V_{AIN} \leq V_{AREF}; V_{DDP} = 5\text{ V}$
			57	-	340	ns	$V_{AIN} \leq V_{AREF}; V_{DDP} = 3.3\text{ V}$
Enable Delay	t_{OED}	CC	-	-	300	ns	ORCCTRL.ENORCx = 1

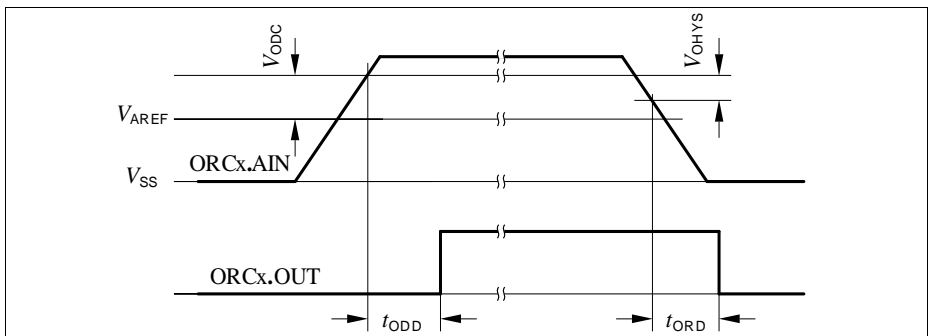


Figure 5 ORCx.OUT Trigger Generation

3.2.4 Analog Comparator Characteristics

Table 13 below shows the Analog Comparator characteristics.

Table 13 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	$V_{DDP} + 0.05$	V	
Input Offset ¹⁾	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode
			–	+/-8	–	mV	Low power mode ³⁾
Propagation Delay ²⁾³⁾	t_{PDELAY}	CC	–	25	–	ns	High power mode, $\Delta V_{CMP} = 100$ mV
			–	80	–	ns	High power mode, $\Delta V_{CMP} = 25$ mV
			–	250	–	ns	Low power mode, $\Delta V_{CMP} = 100$ mV
			–	700	–	ns	Low power mode, $\Delta V_{CMP} = 25$ mV
Current Consumption ³⁾	I_{ACMP}	CC	–	100	–	μ A	First active ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			–	66	–	μ A	Each additional ACMP in high power mode, $\Delta V_{CMP} > 30$ mV
			–	10	–	μ A	First active ACMP in low power mode
			–	6	–	μ A	Each additional ACMP in low power mode
Input Hysteresis ³⁾	V_{HYS}	CC	–	15	–	mV	
Filter Delay ²⁾³⁾	t_{FDELAY}	CC	–	5	–	ns	

1) The comparator accuracy depends on the environment. In particular, the following cases may reduce the accuracy of the comparator and must be avoided:

- Negative current injection on I/O pads close to the comparator input pads
- Switching I/Os close to the comparator inputs
- Switching with a high dV/dt on not used comparator inputs.

This is getting more critical when a big external serial resistance or inductance is added on the inputs.

2) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

3) Not subject to production test, verified by design.

3.2.5 Temperature Sensor Characteristics

Table 14 Temperature Sensor Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy	T_{TSAL} CC	-16	–	16	°C	$T_J = -40\text{ °C}$
		-12	–	12	°C	$T_J = -25\text{ °C}$
		-5	–	5	°C	$T_J = 0\text{ °C}$
		-2	–	2	°C	$T_J = 25\text{ °C}$ (calibrated)
		-4	–	4	°C	$T_J = 70\text{ °C}$
		-2	–	2	°C	$T_J = 115\text{ °C}$ (calibrated)

1) Not subject to production test, verified by design/characterization.

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Table 15 Power Supply Parameters¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ. ²⁾	Max.		
Active mode current ³⁾	I_{DDPA} CC	–	9.2	12	mA	$f_{MCLK} = 32$ MHz $f_{PCLK} = 64$ MHz
		–	4	–	mA	$f_{MCLK} = 1$ MHz $f_{PCLK} = 1$ MHz
Sleep mode current Peripherals clock enabled ⁴⁾	I_{DDPSE} CC	–	6.6	–	mA	$f_{MCLK} = 32$ MHz $f_{PCLK} = 64$ MHz
Sleep mode current Peripherals clock disabled ⁵⁾	I_{DDPSD} CC	–	1.2	–	mA	$f_{MCLK} = 1$ MHz $f_{PCLK} = 1$ MHz
Deep Sleep mode current ⁶⁾	I_{DDPDS} CC	–	0.24	–	mA	
Wake-up time from Sleep to Active mode ⁷⁾	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode ⁸⁾	t_{DSA} CC	–	280	–	μsec	

1) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

2) The typical values are measured at $T_A = +25$ °C and $V_{DDP} = 5$ V.

3) CPU and all peripherals clock enabled, Flash is in active mode.

4) CPU is sleep, all peripherals clock enabled and Flash is in active mode.

5) CPU is sleep, Flash is powered down and code executed from RAM after wake-up.

6) CPU is sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.

7) CPU is sleep, Flash is in active mode during sleep mode.

8) CPU is sleep, Flash is in power down mode during deep sleep mode.

Electrical Parameter

Table 16 provides the active current consumption of some modules operating at 5 V power supply at 25 °C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 16 Typical Active Current Consumption¹⁾

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP ²⁾
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1 ³⁾
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1 ⁴⁾
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1 ⁵⁾
CCU80	$I_{CCU80DDC}$	0.42	mA	Set CGATCLR0.CCU80 to 1 ⁶⁾
POSIF0	$I_{PIF0DDC}$	0.26	mA	Set CGATCLR0.POSIF0 to 1 ⁷⁾
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1 ⁸⁾
MATH	$I_{MATHDDC}$	0.35	mA	Set CGATCLR0.MATH to 1 ⁹⁾
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1 ¹⁰⁾
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1 ¹¹⁾

- 1) Not subject to production test, verified by design/characterisation.
- 2) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
- 3) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode
- 4) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms
- 5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle
- 6) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%
- 7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode
- 8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s
- 9) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11
- 10) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s
- 11) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page	t_{ERASE} CC	6.8	7.1	7.6	ms	
Write time per block	t_{PSE} CC	102	152	204	μ s	
Wake-Up time	t_{WU} CC	–	32.2	–	μ s	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	
Erase Cycles per page	N_{ECYC} CC	–	–	$5 \cdot 10^4$	cycles	
Total Erase Cycles	N_{TECYC} CC	–	–	$2 \cdot 10^6$	cycles	

3.3 AC Parameters

3.3.1 Testing Waveforms

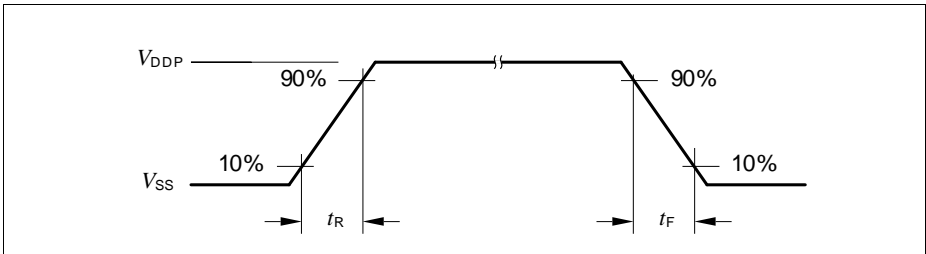


Figure 6 Rise/Fall Time Parameters

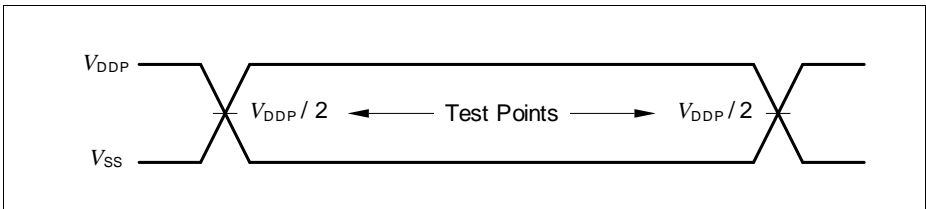


Figure 7 Testing Waveform, Output Delay

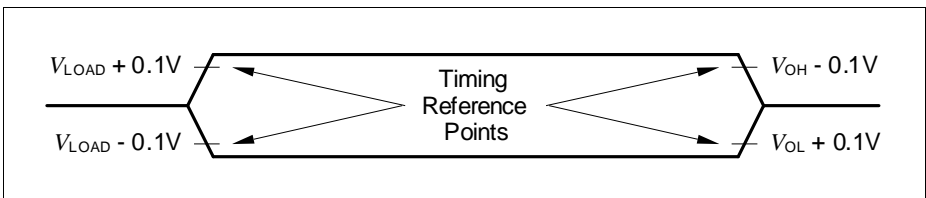


Figure 8 Testing Waveform, Output High Impedance

3.3.2 Output Rise/Fall Times

Table 18 provides the characteristics of the output rise/fall times in the XMC1300. **Figure 6** describes the rise time and fall time parameters.

Table 18 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min.	Max.		
Rise/fall times on High Current Pad ¹⁾²⁾	t_{HCPR}	–	9	ns	50 pF @ 5 V ³⁾
	t_{HCPF}	–	12	ns	50 pF @ 3.3 V ⁴⁾
		–	25	ns	50 pF @ 1.8 V ⁵⁾
Rise/fall times on Standard Pad ¹⁾²⁾	$t_{\text{R}}, t_{\text{F}}$	–	12	ns	50 pF @ 5 V ⁶⁾
		–	15	ns	50 pF @ 3.3 V ⁷⁾
		–	31	ns	50 pF @ 1.8 V ⁸⁾

1) Rise/Fall time parameters are taken with 10% - 90% of supply.

2) Not all parameters are 100% tested, but are verified by design/characterisation and test correlation.

3) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.150 ns/pF at 5 V supply voltage.

4) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.205 ns/pF at 3.3 V supply voltage.

5) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.445 ns/pF at 1.8 V supply voltage.

6) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.225 ns/pF at 5 V supply voltage.

7) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.288 ns/pF at 3.3 V supply voltage.

8) Additional rise/fall time valid for $C_L = 50 \text{ pF} - C_L = 100 \text{ pF}$ @ 0.588 ns/pF at 1.8 V supply voltage.

3.3.3 Power-Up and Supply Threshold Characteristics

Table 19 provides the characteristics of the supply threshold in XMC1300.

Table 19 Power-Up and Supply Threshold Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	$V_{DDP}/S_{VDDPrise}$	–	10^7	μs	¹⁾
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	$V/\mu s$	Slope during normal operation ¹⁾
	S_{VDDP10} SR	0	–	10	$V/\mu s$	Slope during fast transient within +/- 10% of V_{DDP} ¹⁾
	$S_{VDDPrise}$ SR	0	–	10	$V/\mu s$	Slope during power-on or restart after brownout event ¹⁾
	$S_{VDDPfall}$ ²⁾ SR	0	–	0.25	$V/\mu s$	Slope during supply falling out of the +/-10% limits ¹⁾³⁾
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00 _B ¹⁾
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01 _B ¹⁾
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10 _B ¹⁾
V_{DDP} brownout reset voltage	V_{DDPBO} CC	–	1.62	1.75	V	calibrated, before user code starts running
Start-up time from power-on reset	t_{SSW} SR	–	320	–	μs	Time to the first user code instruction ¹⁾⁴⁾

1) Not subject to production test, verified by design/characterization.

2) A capacitor of at least 100 nF has to be added between V_{DDP} and V_{SSP} to fulfill the requirement as stated for this parameter.

Electrical Parameter

- 3) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.
- 4) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

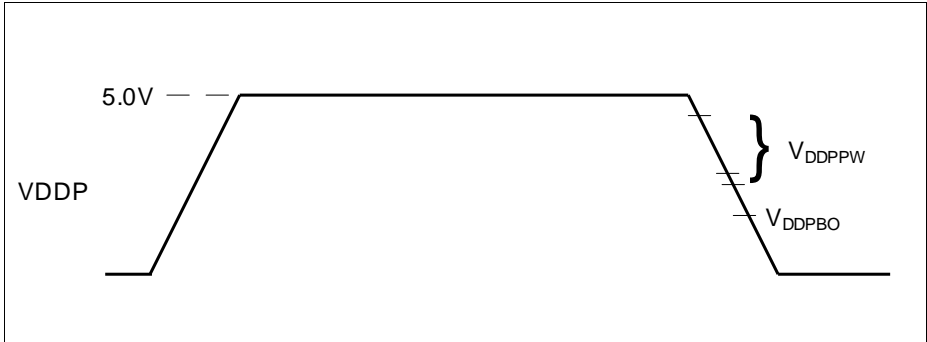


Figure 9 Supply Threshold Parameters

3.3.4 On-Chip Oscillator Characteristics

Table 20 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 20 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	63.5	64	64.5	MHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C) ²⁾
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C) ²⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DCC} and $T_{\text{A}} = +25$ °C.

2) Not subject to production test, verified by design/characterisation.

Table 21 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

Table 21 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	32.5	32.75	33	kHz	under nominal conditions ¹⁾ after trimming
Accuracy	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (0 °C to 85 °C) ²⁾
			-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature (-40 °C to 105 °C) ²⁾

1) The deviation is relative to the factory trimmed frequency at nominal V_{DCC} and $T_{\text{A}} = +25$ °C.

2) Not subject to production test, verified by design/characterisation.

3.3.5 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 22 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	–	500000	ns	–
SWDCLK low time	t_2 SR	50	–	500000	ns	–
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	–	–	ns	–
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	–	–	ns	–
SWDIO output skew after SWDCLK falling edge ¹⁾ (propagation delay)	t_5 CC	-	–	80	ns	–

1) The falling edge on SWDCLK is used to generate the SWDIO output timing.

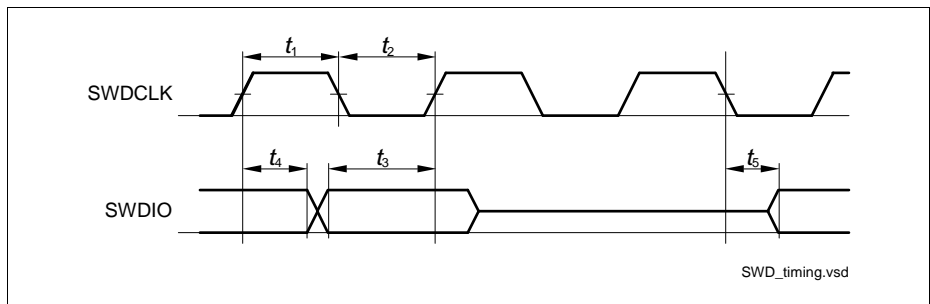


Figure 10 SWD Timing

3.3.6 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is $0.75 \mu\text{s}$. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles ($0.69 \mu\text{s}$).

Table 23 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time ¹⁾	Remark
8 MHz	4	1 to 5	6 to 12	$0.69 \mu\text{s}$	The other closest option ($0.81 \mu\text{s}$) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with $0.5 + (\text{max. number of } 0_B \text{ sample clocks})$

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between $0.69 \mu\text{s}$ and $0.75 \mu\text{s}$ (calculated with nominal sample frequency)

3.3.7 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.7.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 24 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	0	–	–	ns	

Table 25 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10} SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11} SR	10	–	–	ns	

Table 25 USIC SSC Slave Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12} SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13} SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

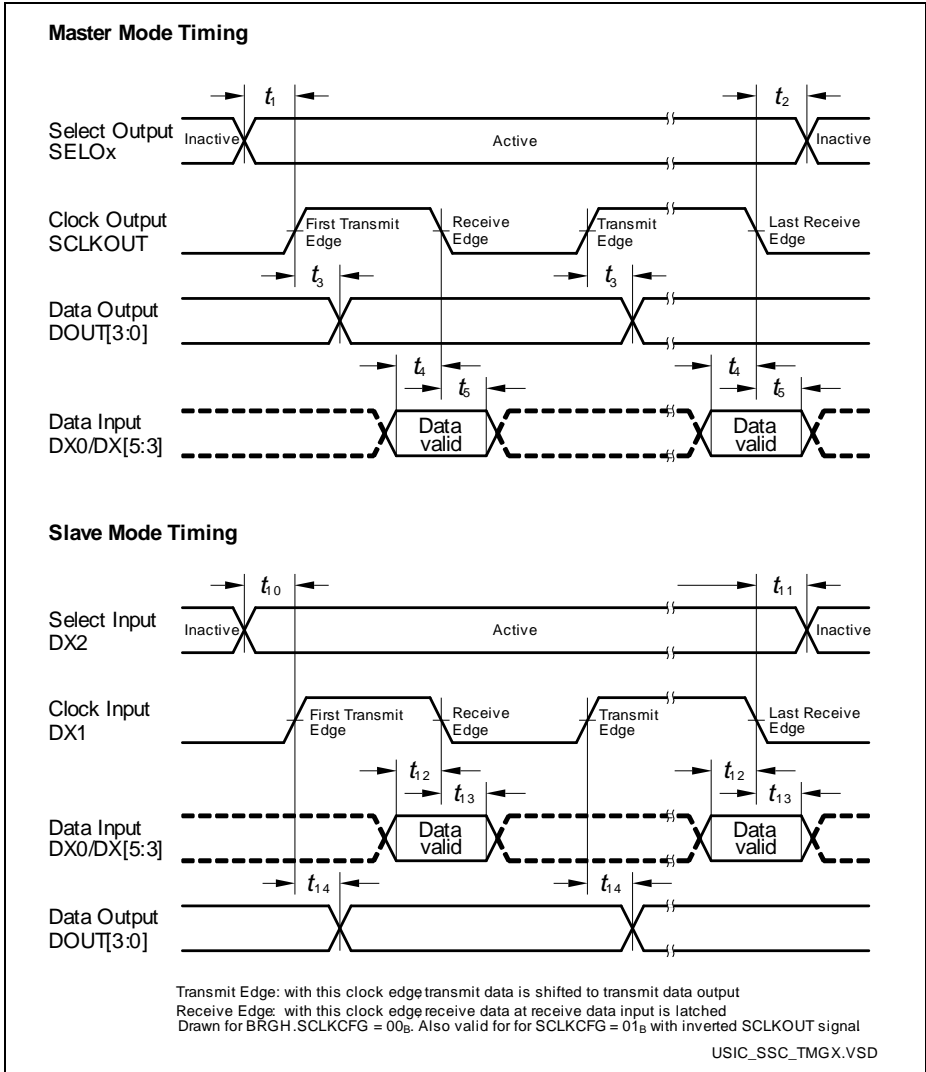


Figure 11 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.7.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 26 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 27 USIC IIC Fast Mode Timing ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1 * C_b ²⁾	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1 * C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

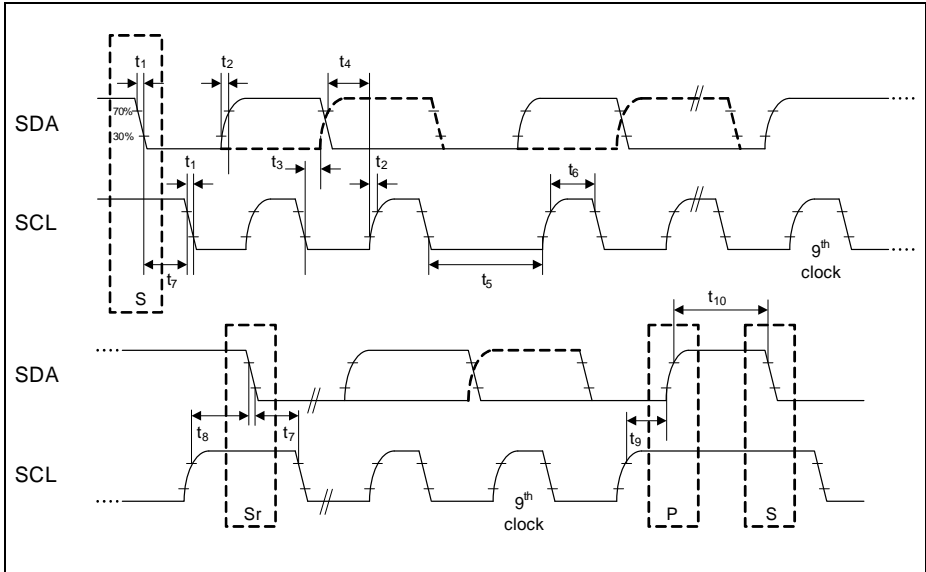


Figure 12 USIC IIC Stand and Fast Mode Timing

3.3.7.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 28 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	
Clock HIGH	t_2 CC	$0.35 \times t_{1min}$	-	-	ns	
Clock Low	t_3 CC	$0.35 \times t_{1min}$	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	$0.15 \times t_{1min}$	ns	

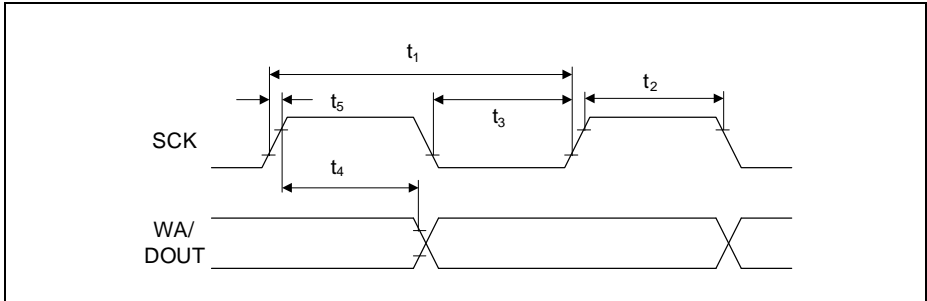


Figure 13 USIC IIS Master Transmitter Timing

Table 29 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t_7 SR	$0.35 \times t_{6min}$	-	-	ns	
Clock Low	t_8 SR	$0.35 \times t_{6min}$	-	-	ns	
Set-up time	t_9 SR	$0.2 \times t_{6min}$	-	-	ns	
Hold time	t_{10} SR	10	-	-	ns	

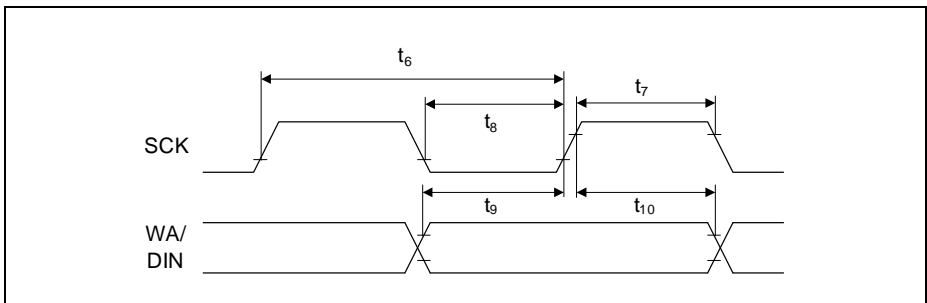


Figure 14 USIC IIS Slave Receiver Timing

4 Package and Reliability

The XMC1300 is a member of the XMC1000 Derivatives of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 30 provides the thermal characteristics of the packages used in XMC1300.

Table 30 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8 ¹⁾
		-	70.3	K/W	PG-TSSOP-38-9 ¹⁾

1) Device mounted on a 4-layer JEDEC board (JESD 51-5).

4.1.1 Thermal Considerations

When operating the XMC1300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$ " quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$$P_{INT} = V_{DDP} \times I_{DDP} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{IOSTAT} = \Sigma((V_{DDP} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system

- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

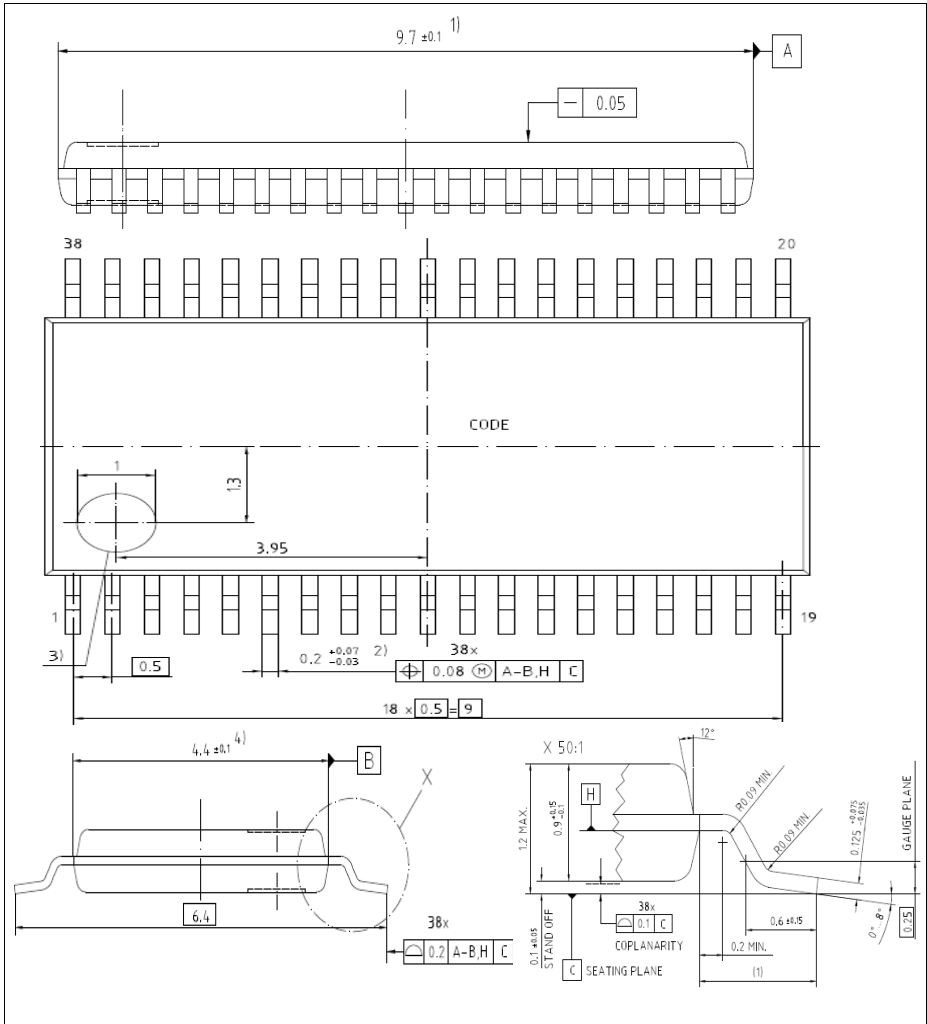


Figure 15 PG-TSSOP-38-9

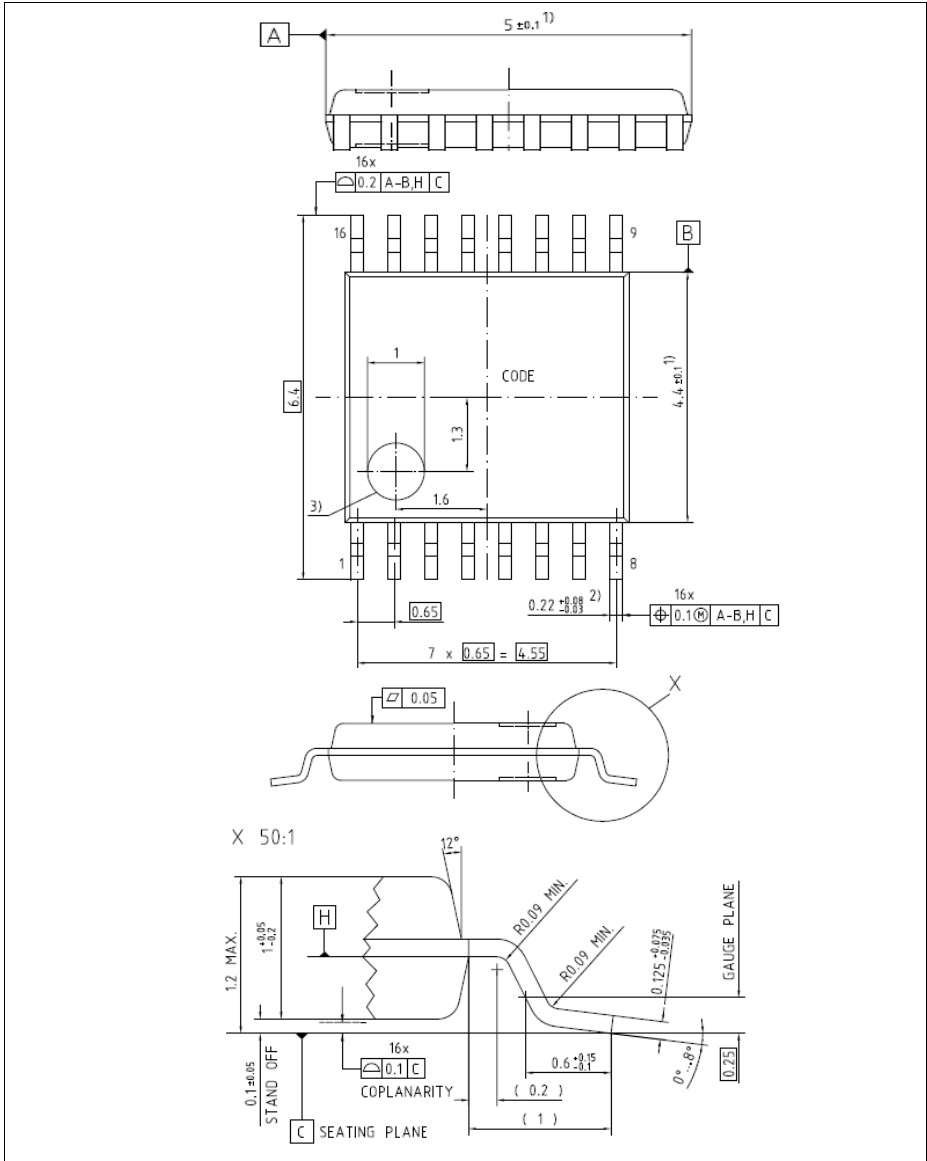


Figure 16 PG-TSSOP-16-8

All dimensions in mm.

5 Quality Declaration

Table 31 shows the characteristics of the quality parameters in the XMC1300.

Table 31 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020C

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