

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™5 Power-Transistor, 100 V
BSC070N10NS5

Data Sheet

Rev. 2.1
Final

1 Description

Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

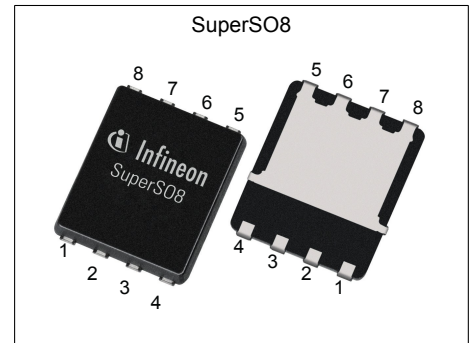
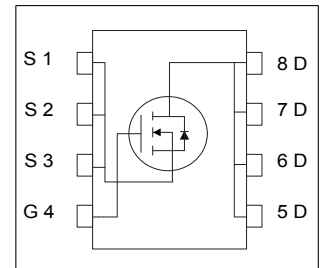


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	7.0	mΩ
I_D	80	A
Q_{oss}	41	nC
$Q_G(0V..10V)$	30	nC



Type / Ordering Code	Package	Marking	Related Links
BSC070N10NS5	PG-TDSON-8	070N10N5	-

¹⁾ J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	80 51 14	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$, $R_{thJA}=50\text{K/W}^1)$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	55	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	83 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.9	1.5	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ¹⁾	R_{thJA}	-	-	50	K/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}, I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ $V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.0 7.6	7.0 10.2	m Ω	$V_{GS}=10\text{ V}, I_D=40\text{ A}$ $V_{GS}=6\text{ V}, I_D=20\text{ A}$
Gate resistance ¹⁾	R_G	-	1.0	1.5	Ω	-
Transconductance	g_{fs}	38	77	-	S	$ V_{DS} >2 I_D /R_{DS(on)max}, I_D=40\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2100	2700	pF	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	340	440	pF	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	16	28	pF	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=40\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=40\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	24	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=40\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Fall time	t_f	-	6	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=40\text{ A},$ $R_{G,ext}=3\text{ }\Omega$

¹⁾ Defined by design. Not Subject to production test.

Table 6 Gate charge characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ²⁾	Q_{gd}	-	6	10	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	11	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ²⁾	Q_g	-	30	38	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	26	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ²⁾	Q_{oss}	-	41	55	nC	$V_{DD}=50\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	76	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	320	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.1	V	$V_{GS}=0\text{ V}$, $I_F=40\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ²⁾	t_{rr}	-	53	106	ns	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ²⁾	Q_{rr}	-	89	179	nC	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ See "Gate charge waveforms" for parameter definition

²⁾ Defined by design. Not Subject to production test.

5 Electrical characteristics diagrams

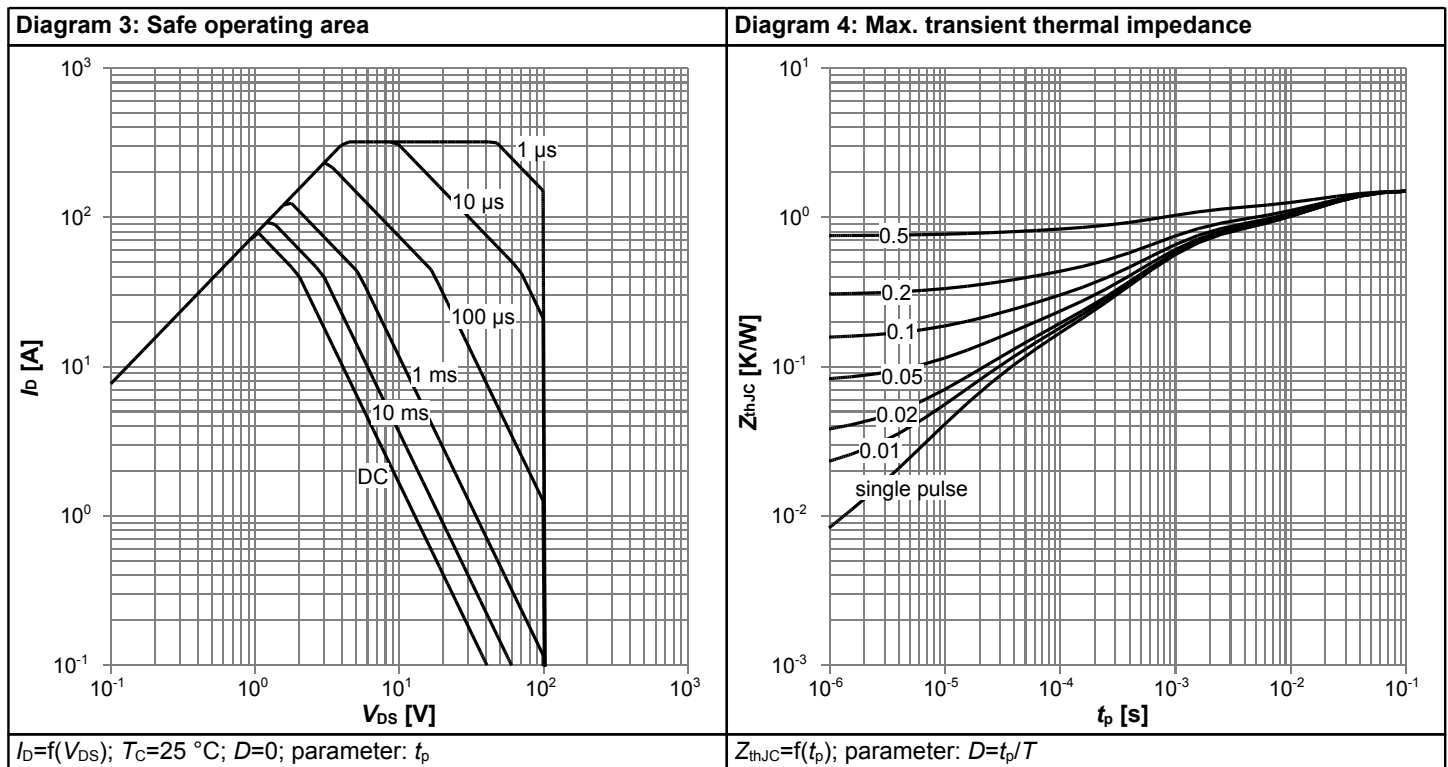
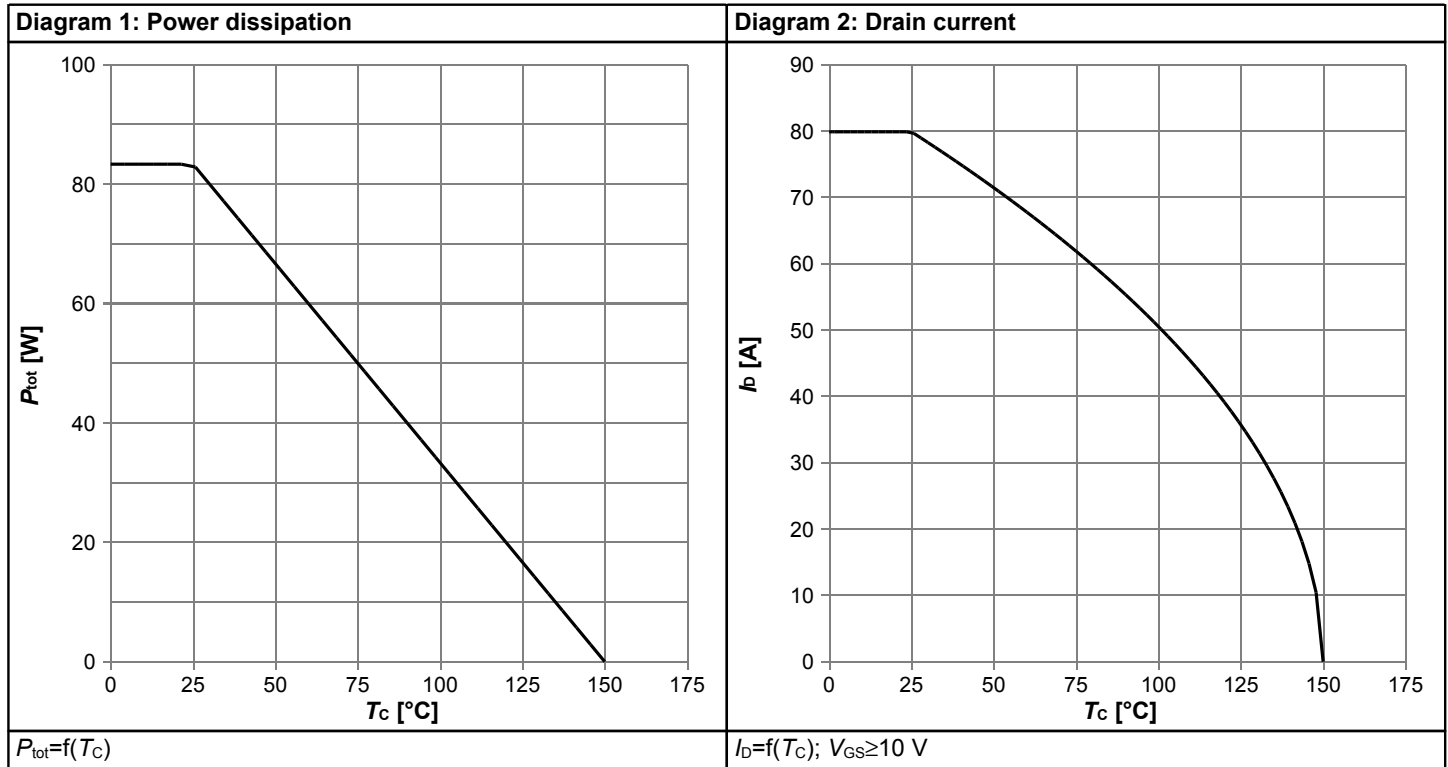
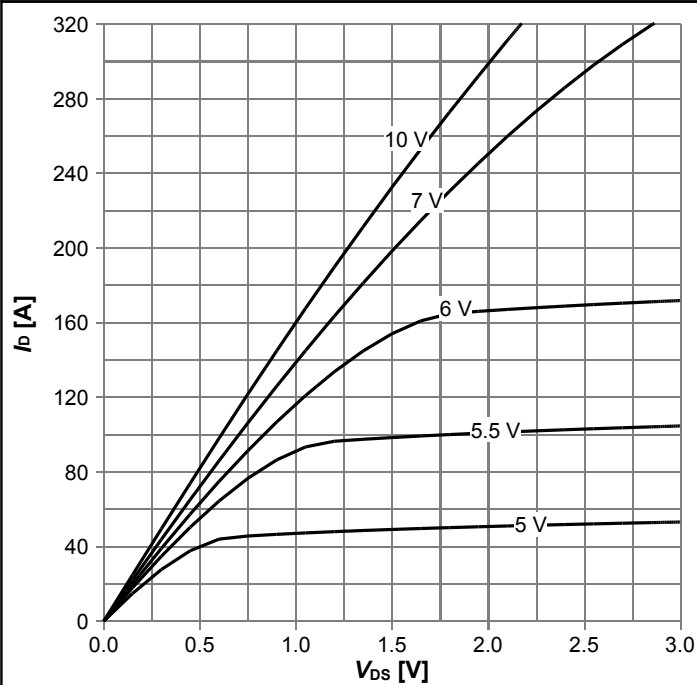
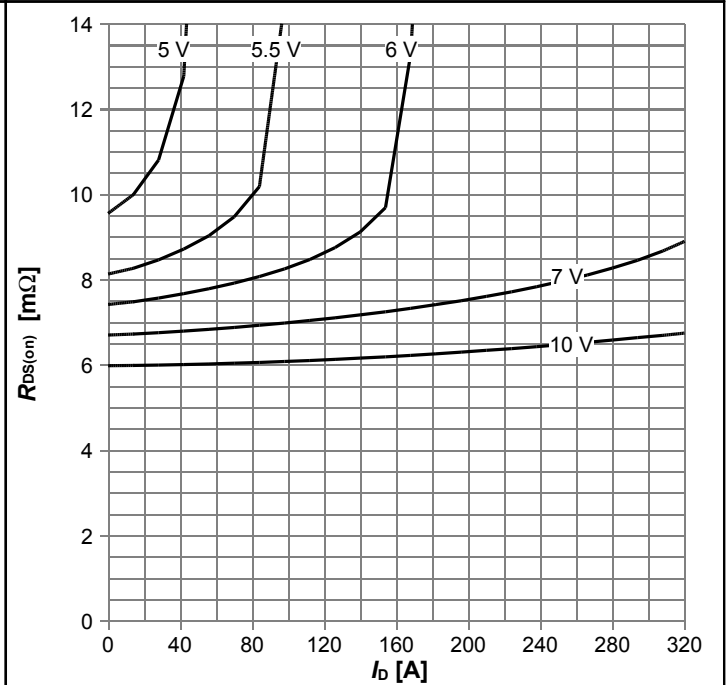


Diagram 5: Typ. output characteristics



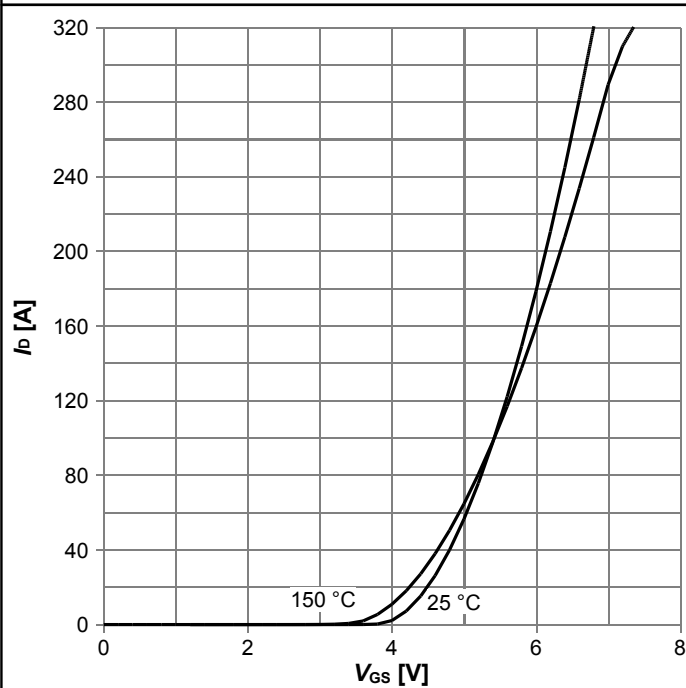
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



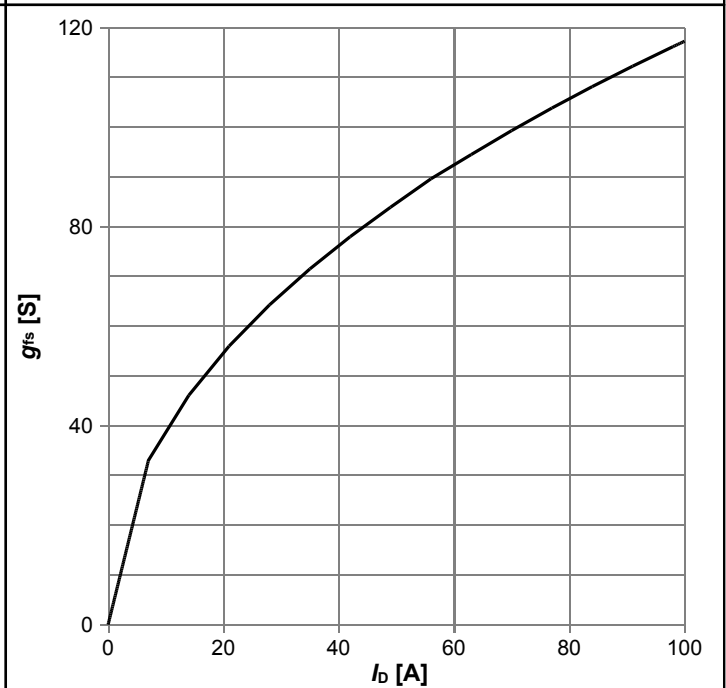
$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



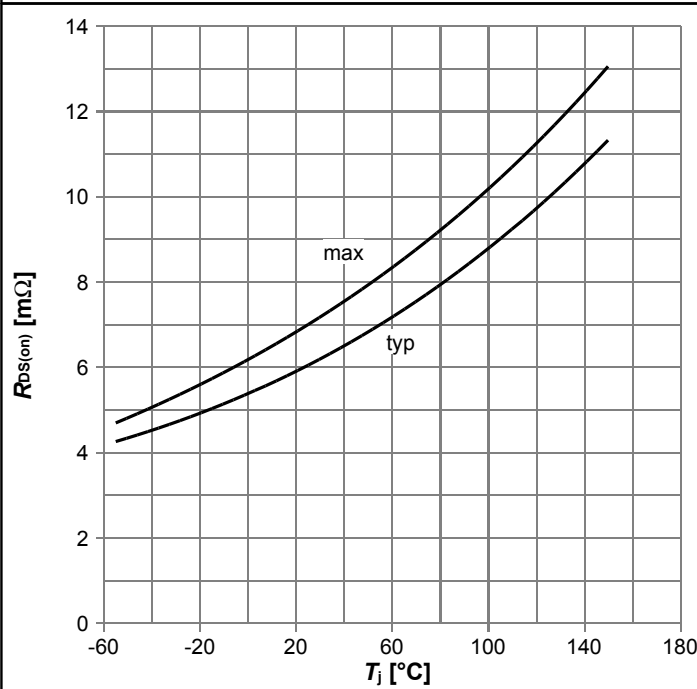
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. forward transconductance



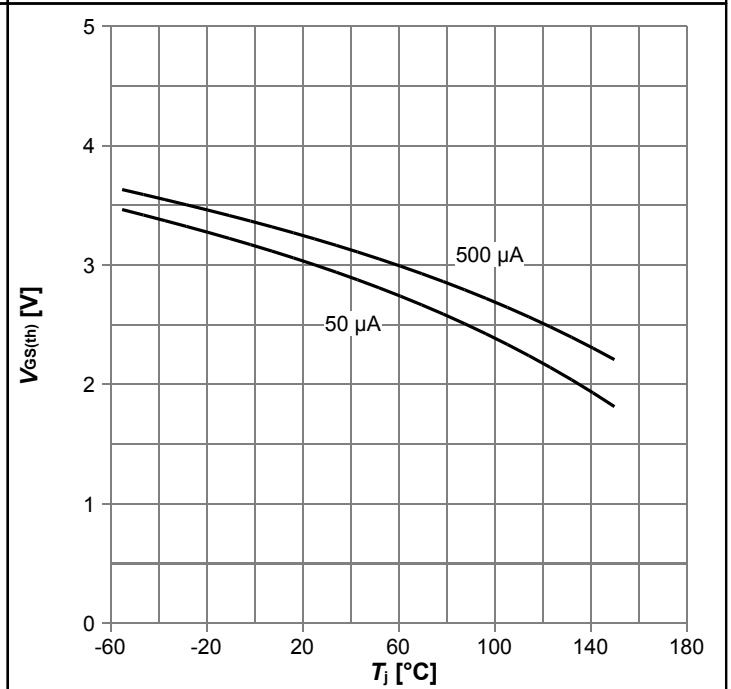
$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



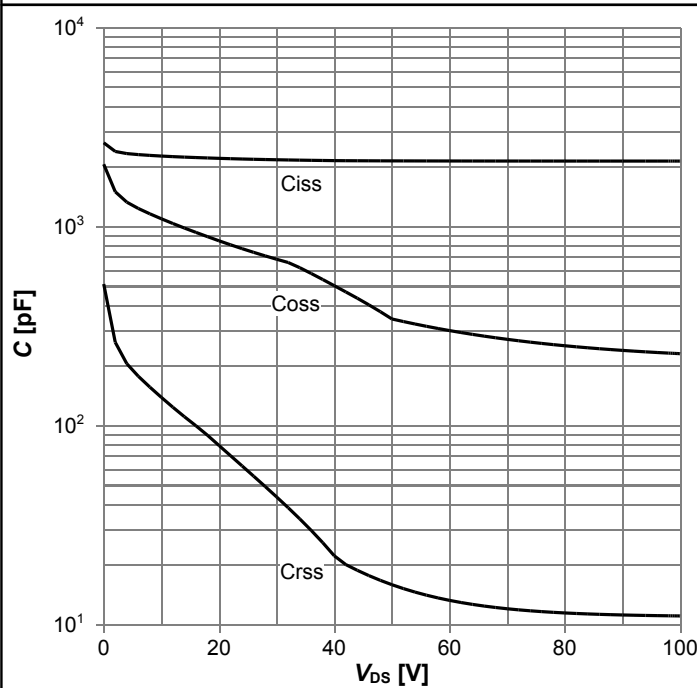
$R_{DS(on)}=f(T_j); I_D=40\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



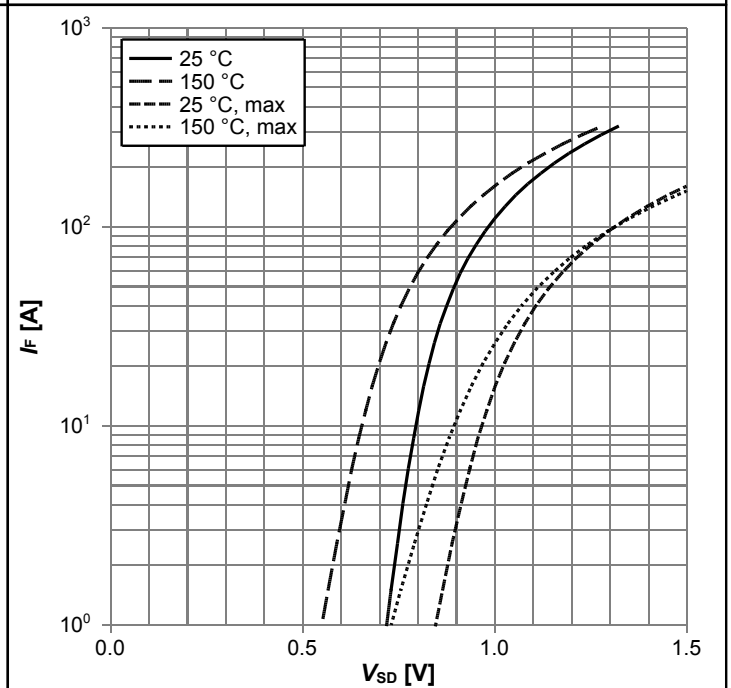
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



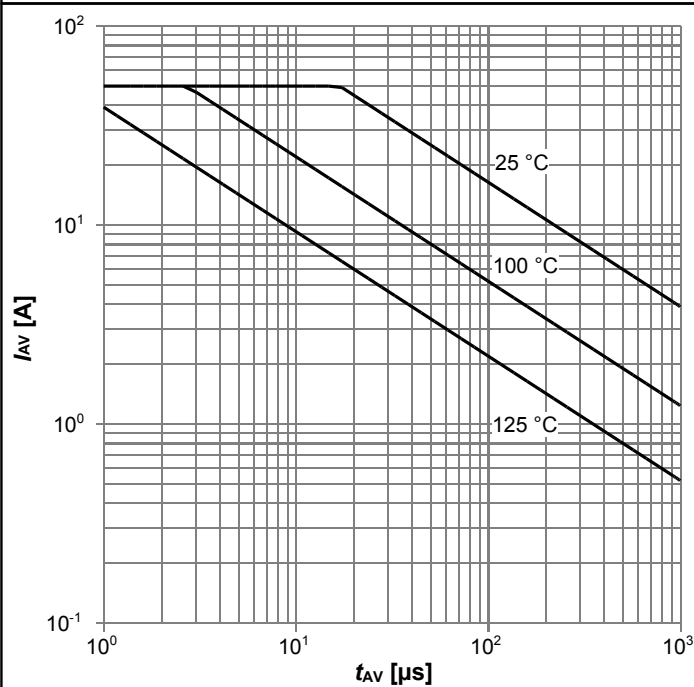
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



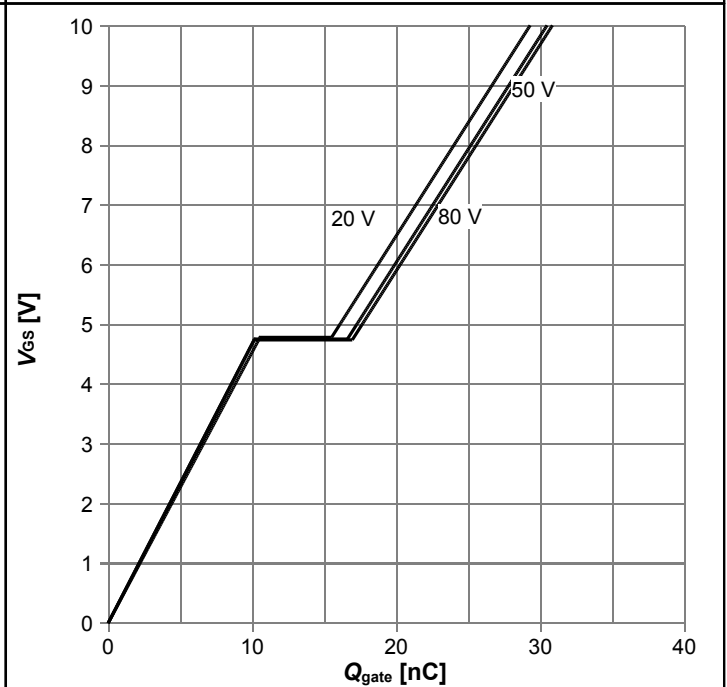
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



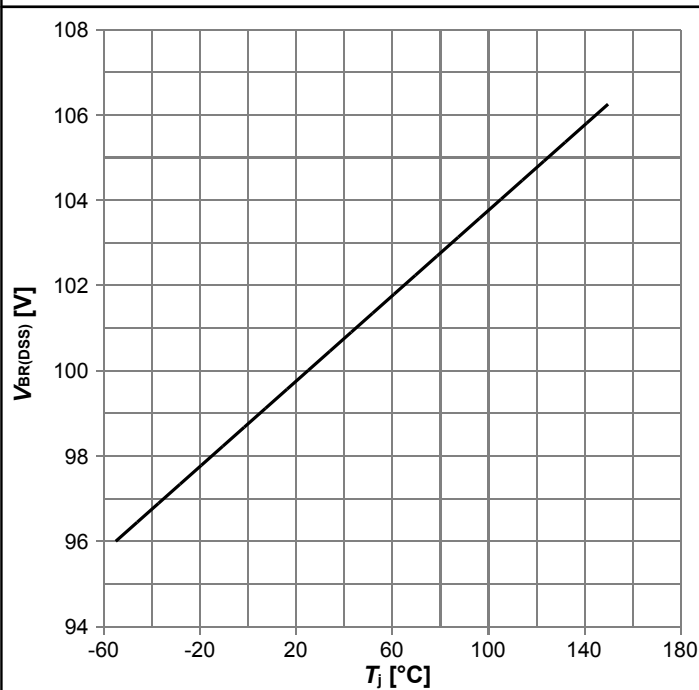
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



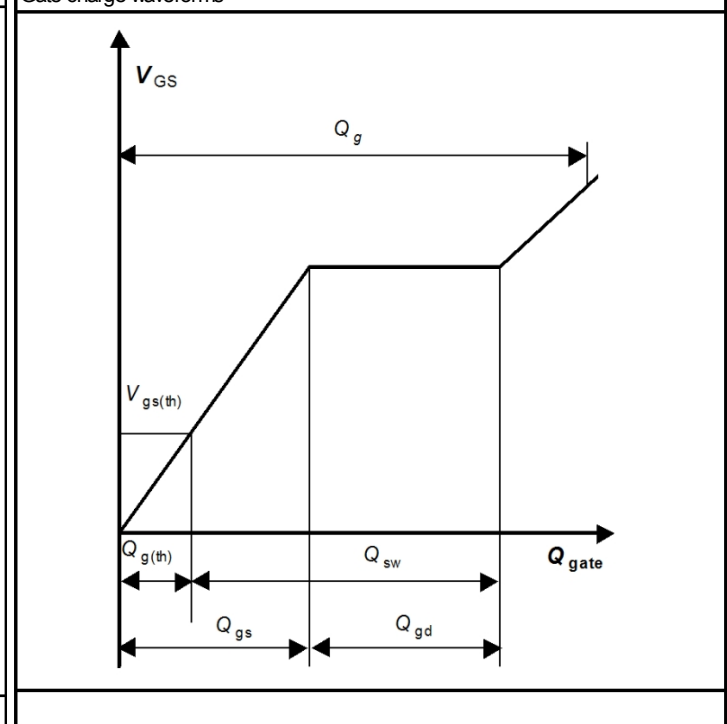
$V_{GS}=f(Q_{gate}); I_D=40$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

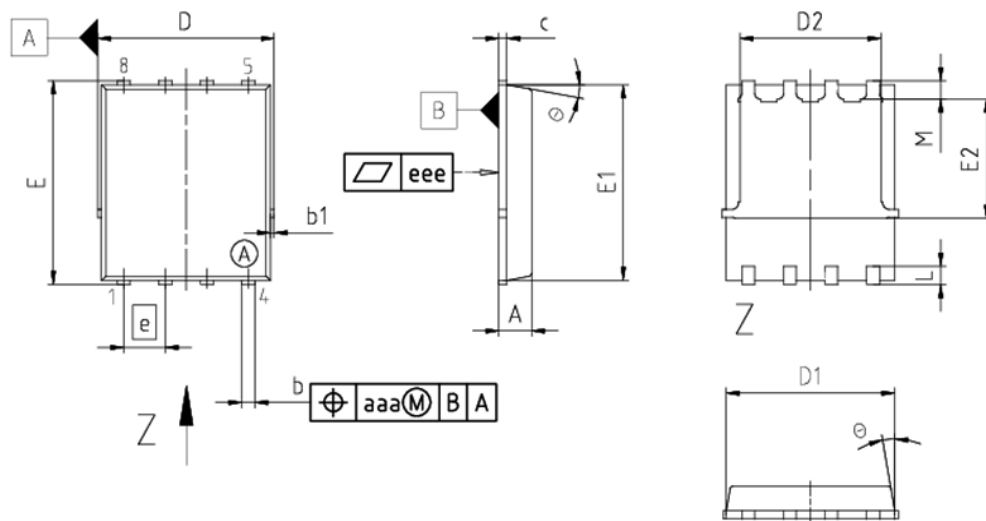


$V_{BR(DSS)}=f(T_j); I_D=1$ mA

Gate charge waveforms



6 Package Outlines



DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
ø	8.5°	12°
aaa	0.25	
eee	0.08	

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SCALE



EUROPEAN PROJECTION



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REVISION
04

Figure 1 Outline PG-TDSON-8, dimensions in mm

Revision History

BSC070N10NS5

Revision: 2015-07-13, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-11-26	Release of final version
2.1	2015-07-13	Update Marking

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