Dual, High Speed MOSFET Driver

ISL55110, ISL55111

The ISL55110 and ISL55111 are dual high speed MOSFET drivers intended for applications requiring accurate pulse generation and buffering. Target applications include ultrasound, CCD imaging, automotive piezoelectric distance sensing and clock generation circuits.

With a wide output voltage range and low ON-resistance, these devices can drive a variety of resistive and capacitive loads with fast rise and fall times, allowing high speed operation with low skew, as required in large CCD array imaging applications.

The ISL55110 and ISL55111 are compatible with 3.3V and 5V logic families and incorporate tightly controlled input thresholds to minimize the effect of input rise time on output pulse width. The ISL55110 has a pair of in-phase drivers while the ISL55111 has two drivers operating in antiphase.

The ISL55110 has a power-down mode for low power consumption during equipment standby times, making it ideal for portable products.

The ISL55110 and ISL55111 are available in 16 Ld Exposed pad QFN packaging and 8 Ld TSSOP. Both devices are specified for operation over the full -40°C to +85°C temperature range.

Features

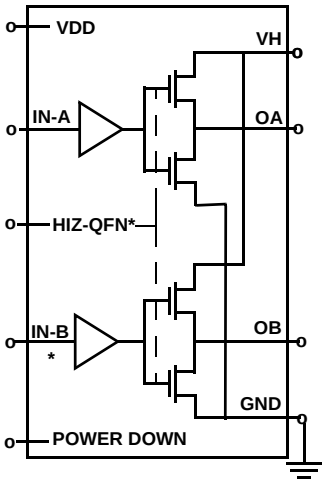
- 5V to 12V Pulse Magnitude
- High Current Drive 3.5A
- 6ns Minimum Pulse Width
- 1.5ns Rise and Fall Times, 100pF Load
- Low Skew
- 3.3V and 5V Logic Compatible
- In-Phase and Anti-Phase Outputs
- Small QFN and TSSOP Packaging
- Low Quiescent Current
- Pb-Free (RoHS Compliant)

Applications

- Ultrasound MOSFET Driver
- CCD Array Horizontal Driver
- Automotive Piezo Driver Applications
- Clock Driver Circuits

Functional Block Diagram

ISL55110 AND ISL55111 DUAL DRIVER

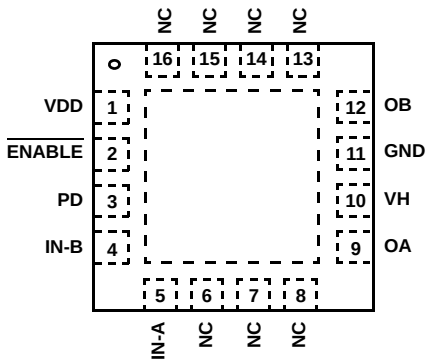


*HIZ AVAILABLE IN QFN PACKAGE ONLY

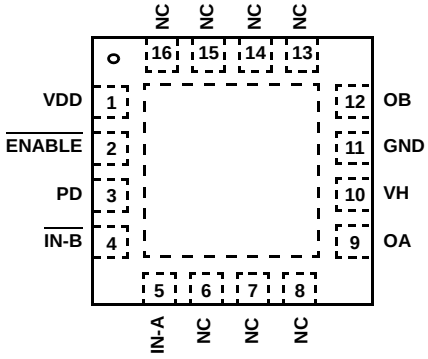
*ISL55111 IN-B IS INVERTING

Pin Configurations

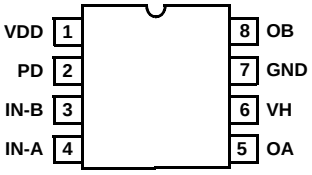
ISL55110
(16 LD QFN)
TOP VIEW



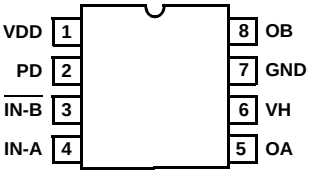
ISL55111
(16 LD QFN)
TOP VIEW



ISL55110
(8 LD TSSOP)
TOP VIEW



ISL55111
(8 LD TSSOP)
TOP VIEW



Pin Descriptions

16 LD QFN	8 LD TSSOP	PIN	FUNCTION
1	1	VDD	Logic Power.
10	6	VH	Driver High Rail Supply.
11	7	GND	Ground, Return for Both VH Rail and VDD Logic Supply.
3	2	PD	Power-Down. Active Logic High Places Part in Power-Down Mode.
2	-	$\overline{\text{ENABLE}}$	QFN Packages Only. When the $\overline{\text{ENABLE}}$ pin is low, the device will operate normally (outputs controlled by the inputs). When the $\overline{\text{ENABLE}}$ pin is tied high, the output will be tri-stated. In other words, it will act as if it is open or floating regardless of what is on the IN-x pins. This provides a High Speed HIZ Logic Control of Driver Outputs.
5	4	IN-A	Logic Level Input that Drives OA to VH Rail or Ground. Not Inverted.
4	3	IN-B, $\overline{\text{INB}}$	Logic Level Input that Drives OB to VH Rail or Ground. Not Inverted on ISL55110, Inverted on ISL55111.
9	5	OA	Driver Output Related to IN-A.
12	8	OB	Driver Output Related to IN-B.
6 through 8, 13 through 16	-	NC	No Connect.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55110IRZ	55110IRZ	-40 to +85	16 Ld QFN	L16.4x4A
ISL55110IVZ	55110 IVZ	-40 to +85	8 Ld TSSOP	M8.173
ISL55111IRZ	55111IRZ	-40 to +85	16 Ld QFN	L16.4x4A
ISL55111IVZ	55111 IVZ	-40 to +85	8 Ld TSSOP	M8.173
ISL55110EVAL1Z	Evaluation Board			
ISL55110EVAL2Z	Evaluation Board			
ISL55111EVAL1Z	Evaluation Board			
ISL55111EVAL2Z	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL55110, ISL55111. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

V_H+ to GND 14.0V
V_{DD} to GND 6.5V
$V_{IN_}$A, $V_{IN_}$V, PDN, $\overline{\text{ENABLE}}$. . . . . (GND - 0.5V) to (V_{DD} + 0.5V)
OA, OB . . . . . (GND - 0.5) to (VH + 0.5V)
Maximum Peak Output Current . . . . . (300mA)
ESD Rating
Human Body Model 3kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld (4x4) QFN Package (Notes 5, 6) . . .	45	3.0
8 Ld TSSOP Package (Notes 4, 7)	140	46

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Drive Supply Voltage (V_H) . . . . . 5V to 13.2V
Logic Supply Voltage (V_{DD}) . . . . . 2.7V to 5.5V
Ambient Temperature (T_A) . . . . . -40°C to +85°C
Junction Temperature (T_J) . . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_H = +12V, V_{DD} = 2.7V to 5.5V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
LOGIC CHARACTERISTICS						
VIX_LH	Logic Input Threshold - Low to High	I_{IH} = 1µA: VIN_A, VIN_B	1.32	1.42	1.52	V
VIX_HL	Logic Input Threshold - High to Low	I_{IL} = 1µA: VIN_A, VIN_B	1.12	1.22	1.32	V
VHYS	Logic Input Hysteresis	VIN_A, VIN_B		0.2		V
VIH	Logic Input High Threshold	PDN	2.0		VDD	V
VIL	Logic Input Low Threshold	PDN	0		0.8	V
VIH	Logic Input High Threshold	$\overline{\text{ENABLE}}$ - QFN only	2.0		VDD	V
VIL	Logic Input Low Threshold	$\overline{\text{ENABLE}}$ - QFN only	0		0.8	V
IIX_H	Input Current Logic High	VIN_A,VIN_B = VDD		10	20	nA
IIX_L	Input Current Logic Low	VIN_A, VIN_B = 0V		10	20	nA
II_H	Input Current Logic High	PDN = VDD		10	20	nA
II_L	Input Current Logic Low	PDN = 0V		10	15	nA

DC Electrical Specifications V_H = +12V, V_{DD} = 2.7V to 5.5V, T_A = +25°C, unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
II_H	Input Current Logic High	$\overline{ENABLE}$ = VDD (QFN only)			12	µA
II_L	Input Current Logic Low	$\overline{ENABLE}$ = 0V (QFN only)	-25			nA
DRIVER CHARACTERISTICS						
r_{DS}	Driver Output Resistance	OA, OB		3	6	Ω
I_{DC}	Driver Output DC Current (>2s)			100		mA
I_{AC}	Peak Output Current	Design Intent verified via simulation.		3.5		A
VOH to VOL	Driver Output Swing Range	VH voltage to Ground	3		13.2	V
SUPPLY CURRENTS						
I_{DD}	Logic Supply Quiescent Current	PDN = Low		4.0	6.0	mA
I_{DD-PDN}	Logic Supply Power-Down Current	PDN = High			12	µA
IH	Driver Supply Quiescent Current	PDN = Low, No resistive load D_{OUT}			15	µA
IH_PDN	Driver Supply Power-Down Current	PDN = High			2.5	µA

AC Electrical Specifications V_H = +12V, V_{DD} = +3.6, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
SWITCHING CHARACTERISTICS						
t_R	Driver Rise Time	OA, OB: CL = 100pF/1k 10% to 90%, VOH - VOL = 12V		1.2		ns
t_F	Driver Fall Time	OA, OB: CL = 100pF/1k 10% to 90%, VOH - VOL = 12V		1.4		ns
t_R	Driver Rise Time	OA, OB CL = 1nF 10% to 90%, VOH - VOL = 12V		6.2		ns
t_F	Driver Fall Time	OA, OB CL = 1nF 10% to 90%, VOH - VOL = 12V		6.9		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 100pF/1k		10.9		ns
tpdF	Input to Output Propagation Delay			10.7		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 330pF		12.8		ns
tpdF	Input to Output Propagation Delay			12.5		ns
tpdR	Input to Output Propagation Delay	Figure 2, Load 680pF		14.5		ns
tpdF	Input to Output Propagation Delay			14.1		ns
tSkewR	Channel-to-Channel tpdR Spread with Same Loads Both Channels	Figure 2, All Loads		<0.5		ns
tSkewF	Channel-to-Channel tpdF Spread with Same Loads Both Channels.	Figure 2, All Loads		<0.5		ns

AC Electrical Specifications V_H = +12V, V_{DD} = +3.6, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
FMAX	Maximum Operating Frequency		70			MHz
TMIN	Minimum Pulse Width		6			ns
PD_{EN}	Power-down to Power-on Time			650		ns
PD_{DIS}	Power-on to Power-down Time			40		ns
t_{EN}	ENABLE to $\overline{\text{ENABLE}}$ Time (HIZ Off)			40		ns
t_{DIS}	$\overline{\text{ENABLE}}$ to ENABLE TIme (HIZ On)			40		ns

NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

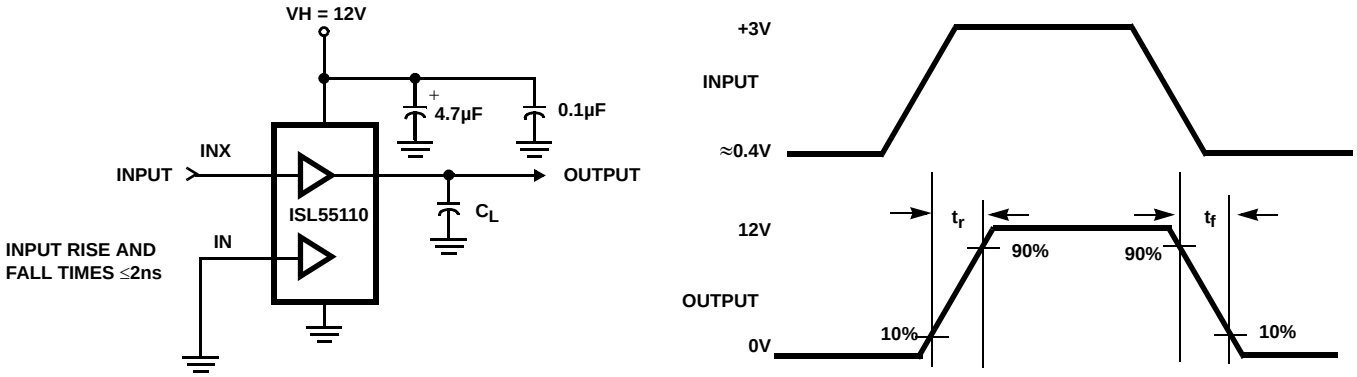
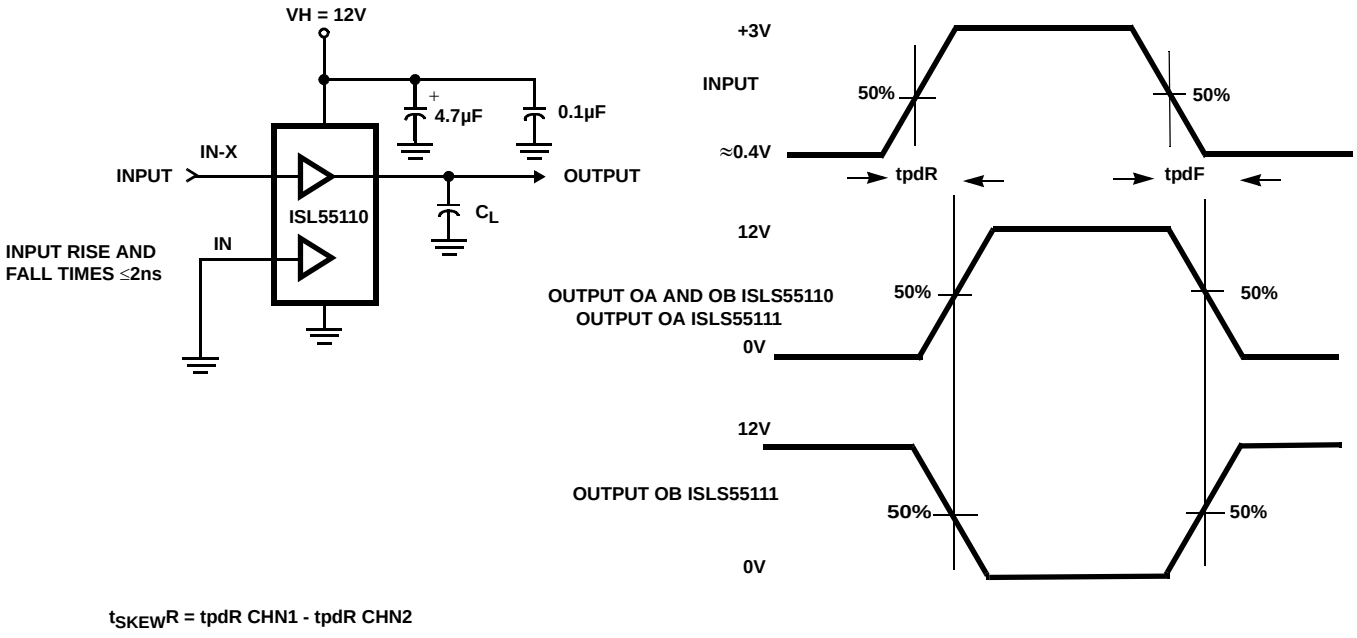


FIGURE 1. TEST CIRCUIT RISE (t_R)/FALL(t_F) THRESHOLDS



$t_{SKEW}R$ = tpdR CHN1 - tpdR CHN2

FIGURE 2. TEST CIRCUIT PROPAGATION TPD DELAY

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12)

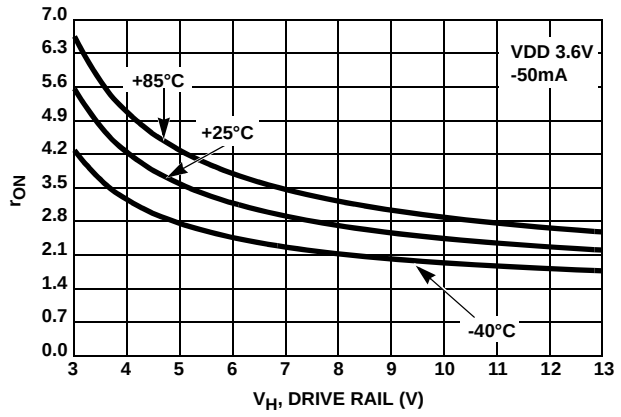


FIGURE 3. DRIVER r_{ON} vs VH SOURCE RESISTANCE

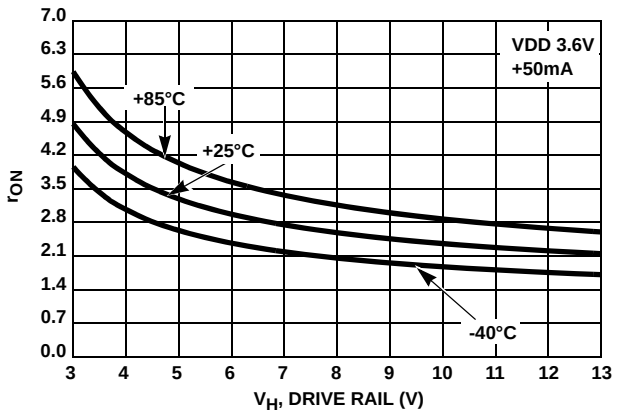


FIGURE 4. DRIVER r_{ON} vs VH SINK RESISTANCE

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12) (Continued)

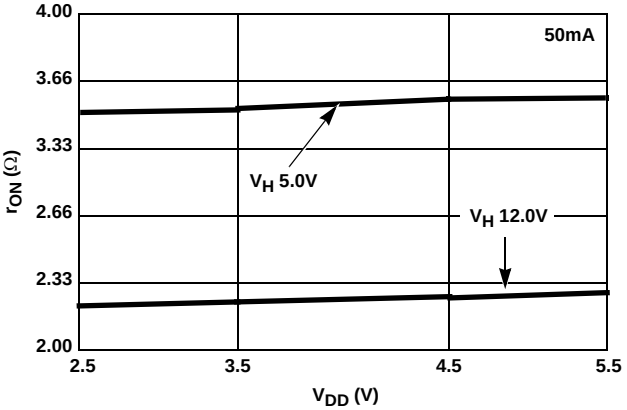


FIGURE 5. r_{ON} vs V_{DD} SOURCE RESISTANCE

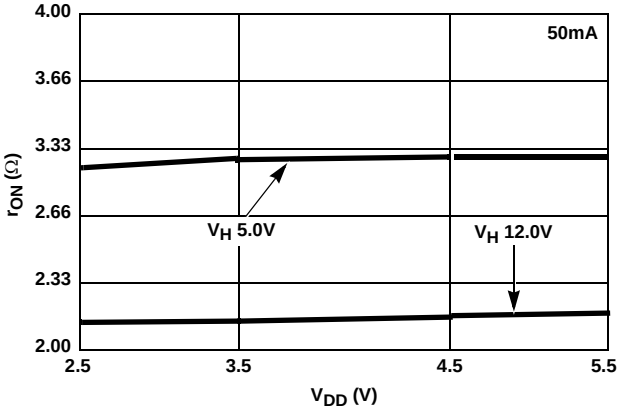


FIGURE 6. r_{ON} vs V_{DD} SINK RESISTANCE

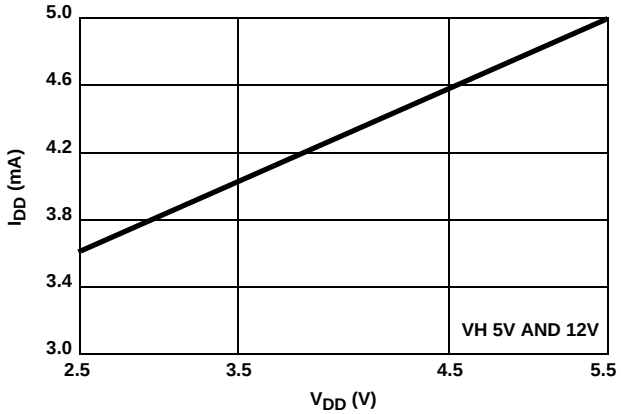


FIGURE 7. I_{DD} vs V_{DD} QUIESCENT CURRENT

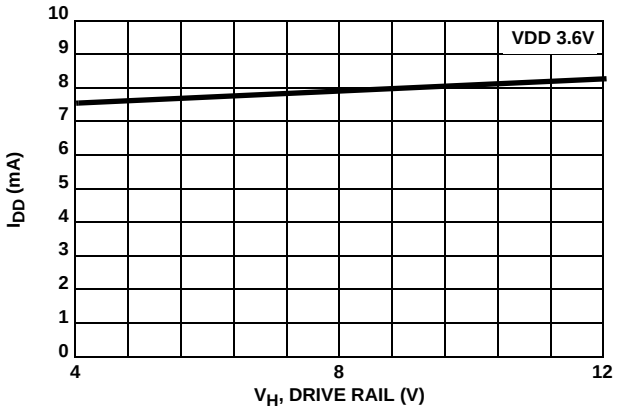


FIGURE 8. I_{DD} vs V_H @ 50MHz (NO LOAD)

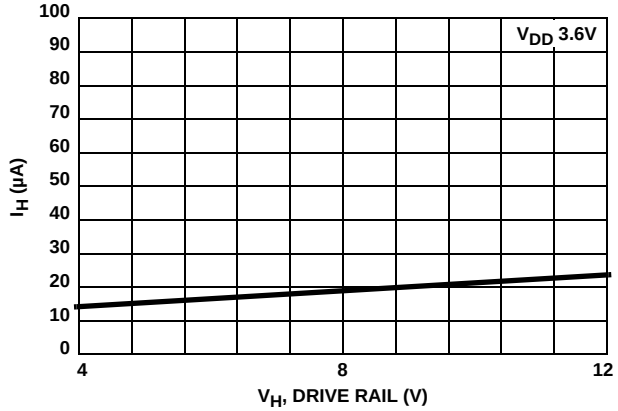


FIGURE 9. QUIESCENT I_H vs V_H

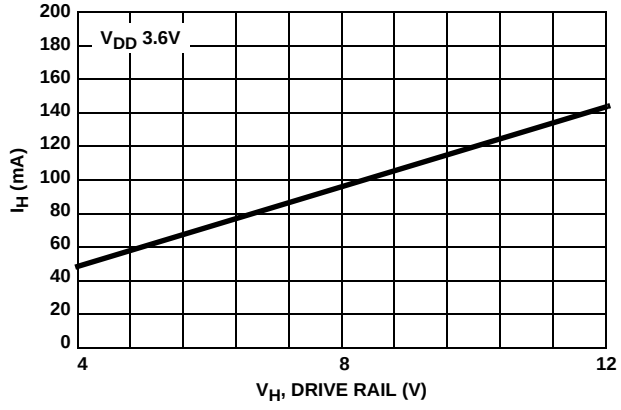


FIGURE 10. I_H vs V_H @ 50MHz (NO LOAD)

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12) (Continued)

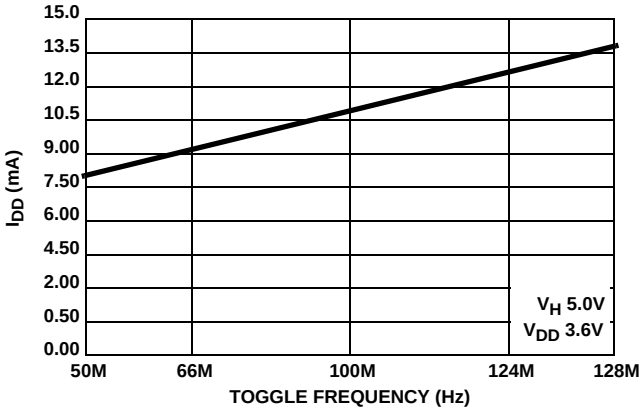


FIGURE 11. I_{DD} vs FREQUENCY (DUAL CHANNEL, NO LOAD)

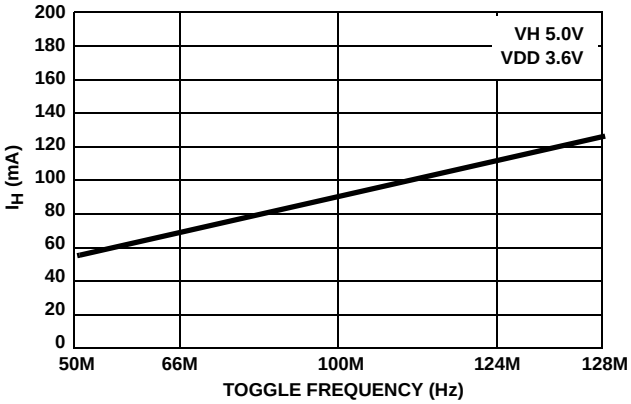


FIGURE 12. IH vs FREQUENCY (DUAL CHANNEL, NO LOAD)

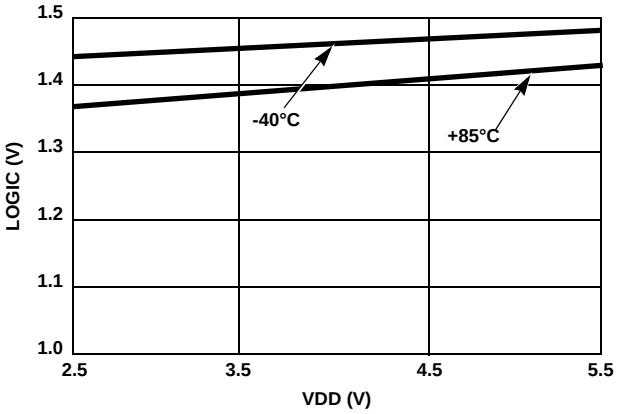


FIGURE 13. VIH LOGIC THRESHOLDS

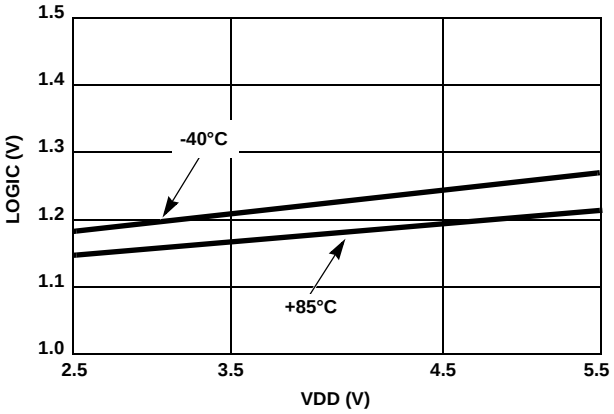


FIGURE 14. VIL LOGIC THRESHOLDS

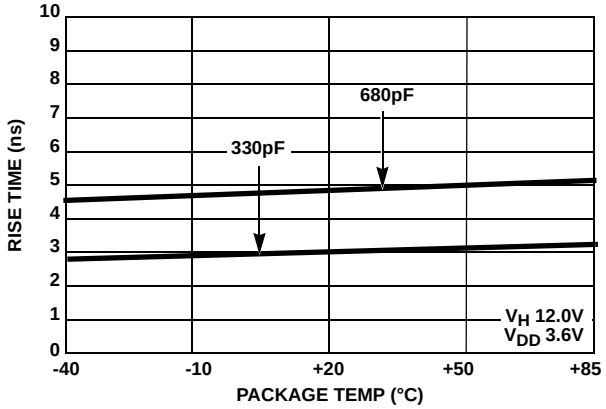


FIGURE 15. t_R vs TEMPERATURE

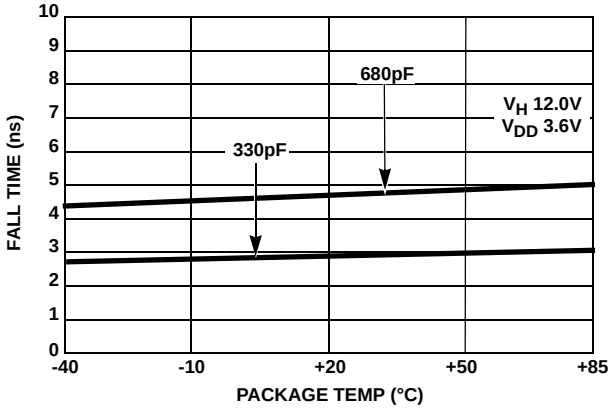


FIGURE 16. t_F vs TEMPERATURE

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12) (Continued)

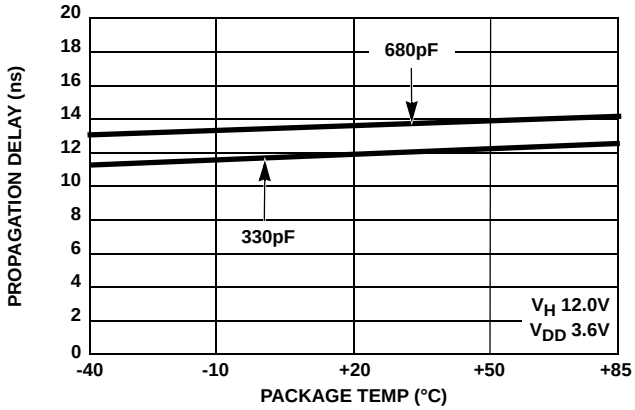


FIGURE 17. tpdR vs TEMPERATURE

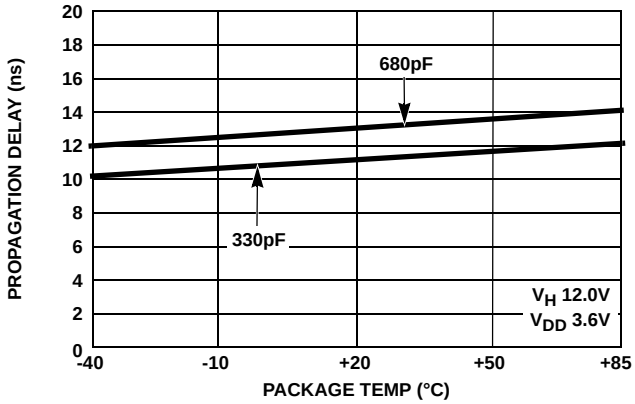


FIGURE 18. tpdF vs TEMPERATURE

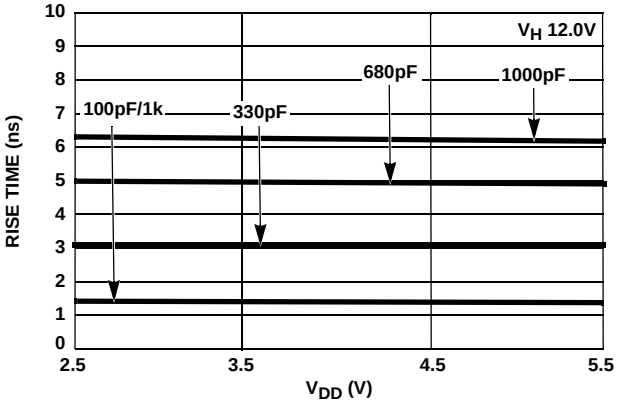


FIGURE 19. t_R vs V_{DD}

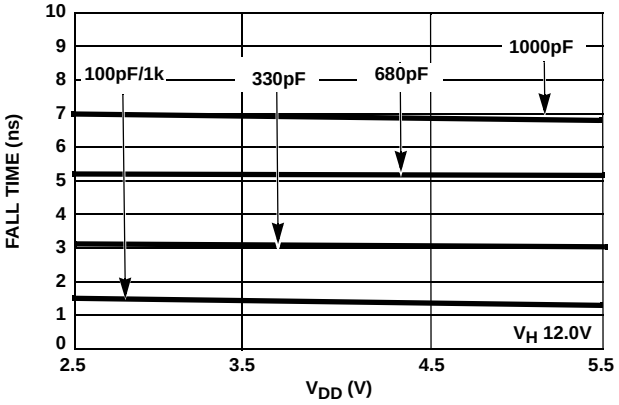


FIGURE 20. t_F vs V_{DD}

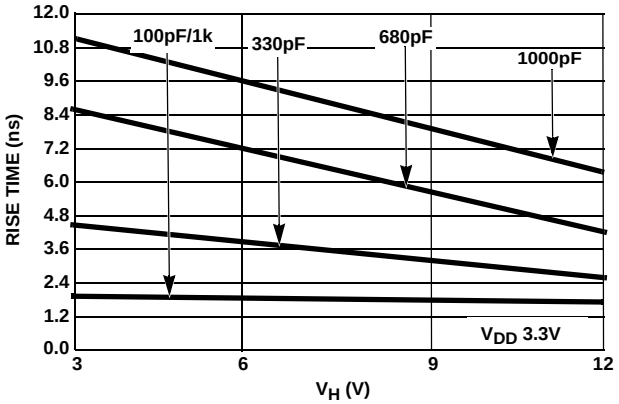


FIGURE 21. t_R vs V_H

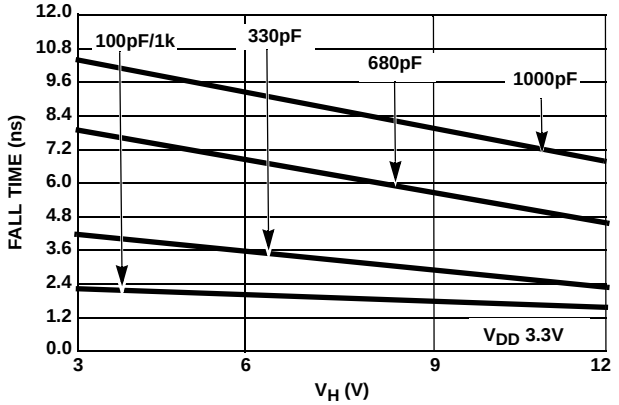


FIGURE 22. t_F vs V_H

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12) (Continued)

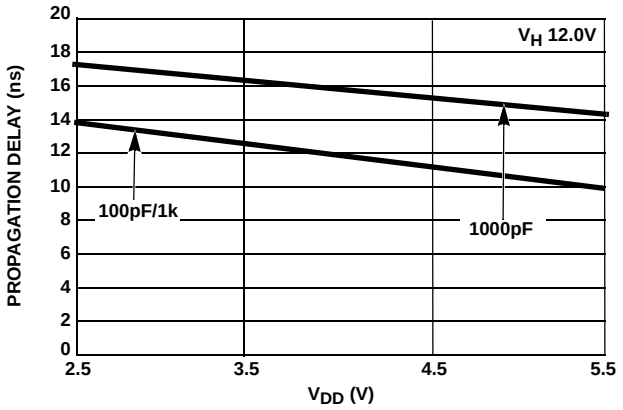


FIGURE 23. tpdR vs V_{DD}

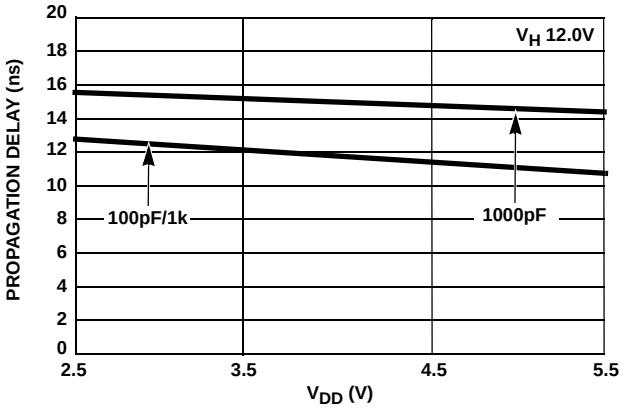


FIGURE 24. tpdF vs V_{DD}

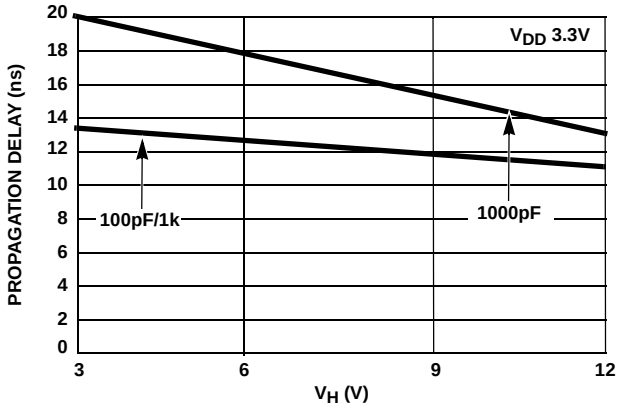


FIGURE 25. tpdR vs V_H

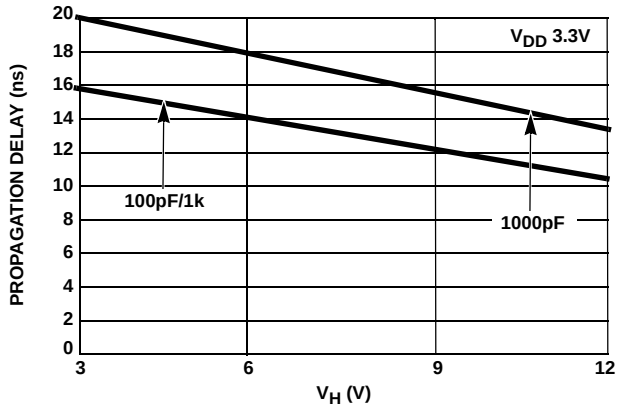


FIGURE 26. tpdF vs V_H

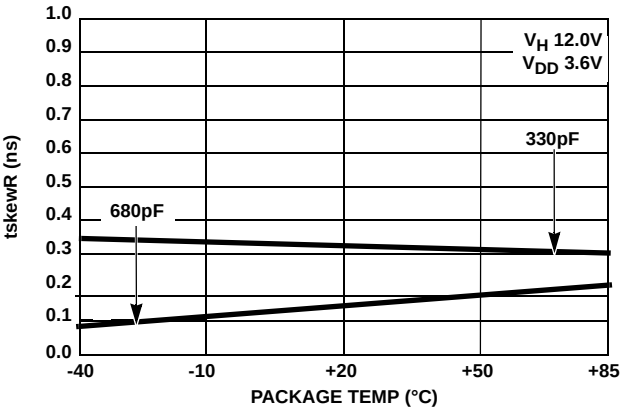


FIGURE 27. tSkewR vs TEMPERATURE

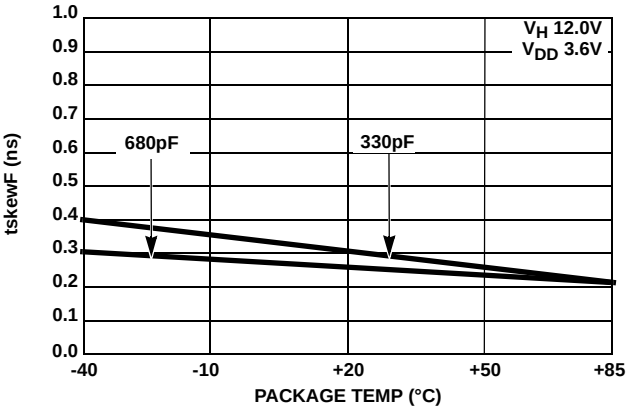


FIGURE 28. tSkewF vs TEMPERATURE

Typical Performance Curves (See "Typical Performance Curves Discussion" on page 12) (Continued)

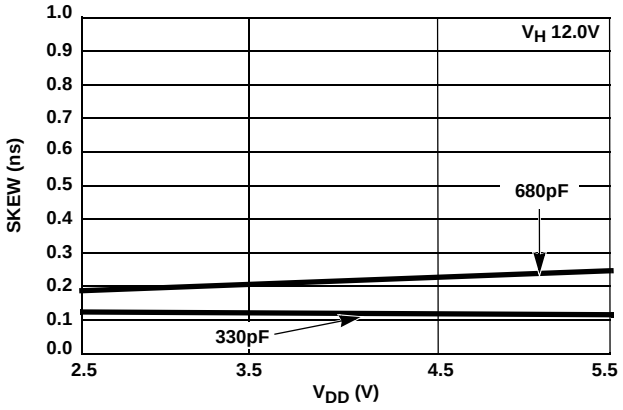


FIGURE 29. tSkewR vs V_{DD}

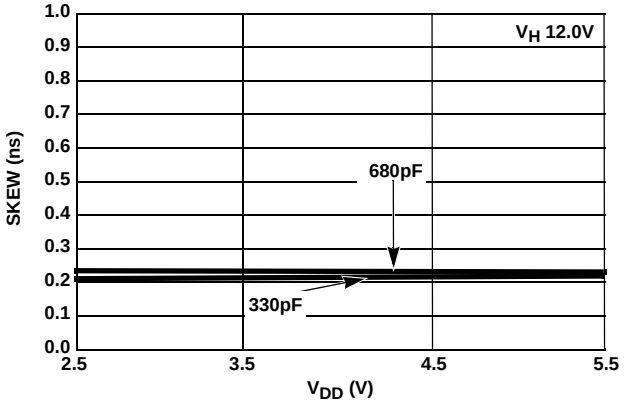


FIGURE 30. tSkewF vs V_{DD}

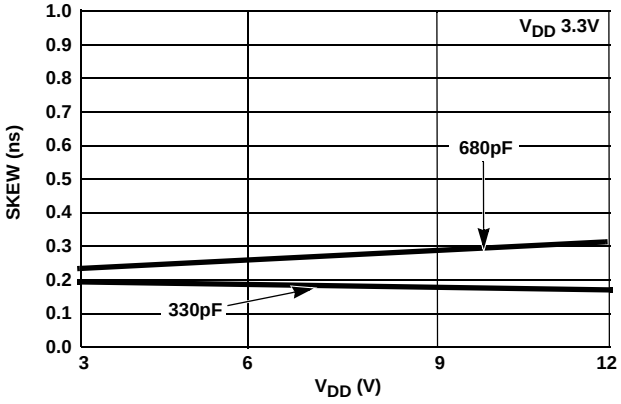


FIGURE 31. tSkewR vs V_H

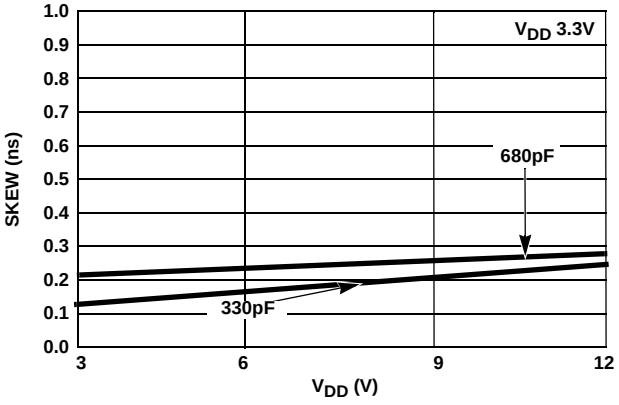


FIGURE 32. tSkewF vs V_H

Typical Performance Curves Discussion

r_{ON}

The r_{ON} Source is tested by placing the device in constant drive high Condition and connecting -50mA constant current source to the driver output. The voltage drop is measured from V_H to driver output for r_{ON} calculations.

The r_{ON} sink is tested by placing the device in constant driver Low Condition and connecting a +50mA constant current source. The voltage drop from driver out to ground is measured for r_{ON} calculations.

Dynamic Tests

All dynamic tests are conducted with ISL55110 and ISL55111 evaluation board(s) (ISL55110_11EVAL2Z). Driver loads are soldered to the evaluation board. Measurements are collected with P6245 active FET Probes and TDS5104 oscilloscope. Pulse stimulus is provided by HP8131 pulse generator.

The ISL55110 and ISL55111 evaluation boards provide test point fields for leadless connection to either an active FET probe or differential probe. TP- IN fields are used for monitoring pulse input stimulus. TP- OA/B monitor driver output waveforms. C_6 and C_7 are the usual placement for driver loads. R_3 and R_4 are not populated and are provided for user-specified, more complex load characterization.

Pin Skew

Pin skew measurements are based on the difference in propagation delay of the two channels. Measurements are made on each channel from the 50% point on the stimulus point to the 50% point on the driver output. The difference in the propagation delay for channel A and channel B is considered to be Skew.

Both rising propagation delay and falling propagation delay are measured and report as tSkewR and tSkewF.

50MHz Tests

50MHz Tests reported as no load actually include evaluation board parasitics and a single TEK 6545 FET probe. However, no driver load components are installed and C_6 through C_9 and R_3 through R_6 are not populated.

General

The most dynamic measurements are presented in three ways:

1. Over-temperature with a V_{DD} of 3.6V and V_H of 12.0V.
2. At ambient with V_H set to 12V and V_{DD} data points of 2.5V, 3.5V, 4.5V and 5.50V.
3. The ambient tests are repeated with V_{DD} of 3.3V and V_H data points of 3V, 6V, 9V and 12V.

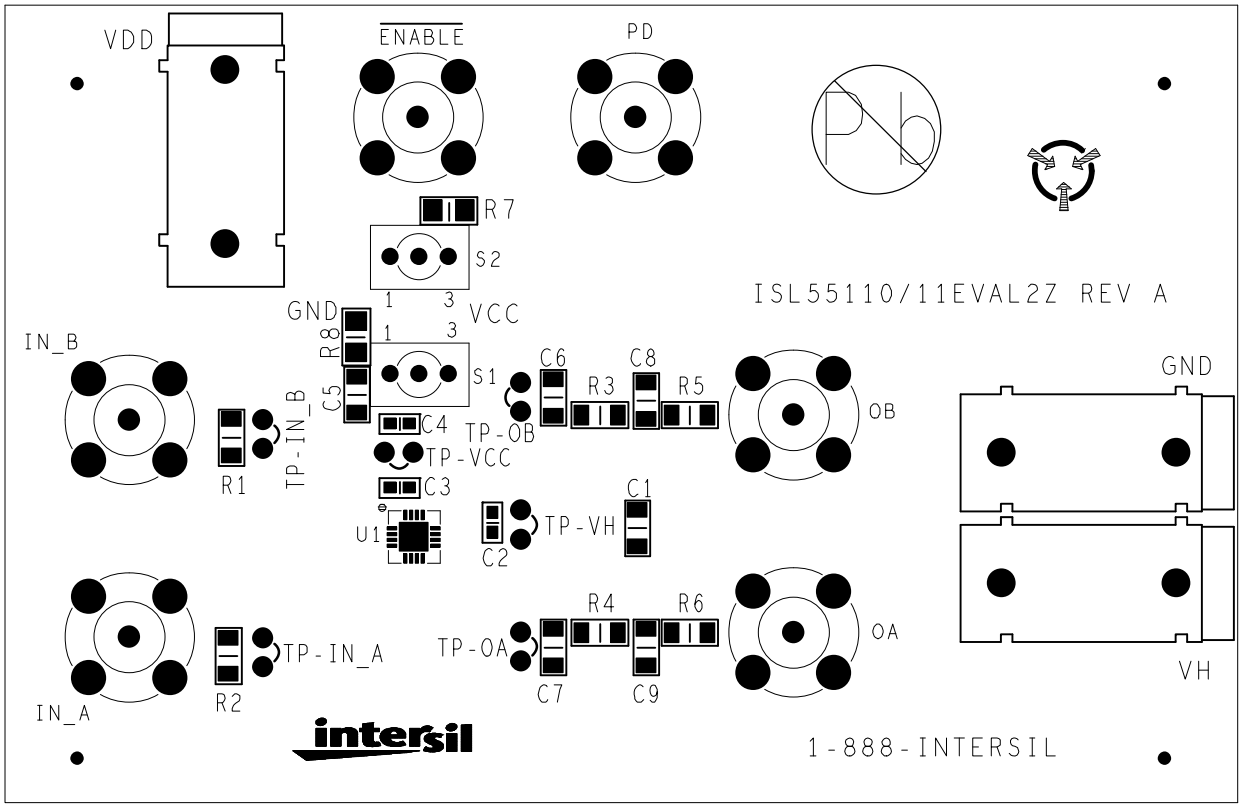


FIGURE 33. ISL55110_11EVAL2Z EVALUATION BOARD

Detailed Description

The ISL55110 and ISL55111 are dual high speed MOSFET drivers intended for applications requiring accurate pulse generation and buffering. Target applications include ultrasound, CCD imaging, automotive piezoelectric distance sensing and clock generation circuits.

With a wide output voltage range and low on-resistance, these devices can drive a variety of resistive and capacitive loads with fast rise and fall times, allowing high speed operation with low skew as required in large CCD array imaging applications.

The ISL55110 and ISL55111 are compatible with 3.3V and 5V logic families and incorporate tightly controlled input thresholds to minimize the effect of input rise time on output pulse width. The ISL55110 has a pair of in-phase drivers while the ISL55111 has two drivers operating in antiphase. Both inputs of the device have independent inputs to allow external time phasing if required.

In addition to power MOSFET drivers, the ISL55110 and ISL55111 are well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge pump voltage inverters.

Input Stage

The input stage is a high impedance input with rise/fall hysteresis. This means that the inputs will be directly compatible with both TTL and lower voltage logic over the entire V_{DD} range. The user should treat the inputs as high speed pins and keep rise and fall times to <2ns.

Output Stage

The ISL55110 and ISL55111 output are a high-power CMOS driver, swinging between ground and V_H. At V_H = 12V, the output impedance of the inverter is typically 3.0Ω. The high peak current capability of the ISL55110 and ISL55111 enables it to drive a 330pF load to 12V with a rise time of <3.0ns over the full temperature range. The output swing of the ISL55110 and ISL55111 comes within < 30mV of the V_H and Ground rails.

Application Notes

Although the ISL55110 and ISL55111 are simply a dual level shifting driver, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ISL55111 has one inverting input, any common impedance will generate negative feedback, and may degrade the delay times and rise and fall times. Use a ground plane if possible or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ISL55110 and ISL55111 as possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors, which have a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use small damping resistor in series with the output of the ISL55110 and ISL55111. Although this reduces ringing, it will also slightly increase the rise and fall times.
4. Use good bypassing techniques to prevent supply voltage ringing.

Power Dissipation Calculation

The Power dissipation equation has three components:

1. Quiescent Power Dissipation,
2. Power dissipation due to Internal Parasitics
3. Power Dissipation because of the Load Capacitor.

Power dissipation due to internal parasitics is usually the most difficult to accurately quantitize. This is primarily due to crowbar current which is a product of both the high and low drivers conducting effectively at the same time during driver transitions. Design goals always target the minimum time for this condition to exist. Given that how often this occurs is a product of frequency, crowbar effects can be characterized as internal capacitance.

Lab tests are conducted with driver outputs disconnected from any load. With design verification packaging, bond wires are removed to aid in the characterization process. Based on laboratory tests and simulation correlation of those results, Equation 1 defines the ISL55110 and ISL55111 Power Dissipation per channel:

$$P = V_{DD} \times 3.3e\text{-}3 + 10pF \times V_{DD}^2 \times f + 135pF \times VH^2 \times f + CL \times VH^2 \times f \quad \text{(Watts/Channel)} \qquad \text{(EQ. 1)}$$

- Where 3.3mA is the quiescent current from the V_{DD}. This forms a small portion of the total calculation. When figuring two channel power consumption, only include this current once.
- 10pF is the approximate parasitic Capacitor (Inverters, etc.), which the V_{DD} drives.
- 135pF is the approximate parasitic at the D_{OUT} and its Buffers. This includes the effect of the Crow-bar Current.
- C_L is the Load capacitor being driven.

Power Dissipation Discussion

Specifying continuous pulse rates, driver loads and driver level amplitudes are key in determining power supply requirements, as well as dissipation/cooling necessities. Driver output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

As detailed in the "Power Dissipation Calculation" on page 14, power dissipation of the device is calculated by taking the DC current of the V_{DD} (logic) and V_H current (driver rail) times the respective voltages and adding the product of both calculations. The average DC current measurements of I_{DD} and IH should be done while running the device with the planned V_{DD} and V_H levels and driving the required pulse activity of both channels at the desired operating frequency and driver loads.

Therefore, the user must address power dissipation relative to the planned operating conditions. Even with a device mounted per notes 4 or 5 under "Thermal Information", given the high speed pulse rate and amplitude capability of the ISL55110 and ISL55111, it is possible to exceed the +150°C "absolute maximum junction temperature". Therefore, it is important to calculate the maximum junction temperature for the application to determine if operating conditions need to be modified for the device to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 2:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 2)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on number of channels changing state and frequency of operation. The extent of continuous active pulse generation will greatly effect dissipation requirements.

The user should evaluate various heat sink/cooling options in order to control the ambient temperature part of the equation. This is especially true if the user's applications require continuous, high speed operation. A review of the θ_{JA} ratings of the TSSOP and QFN package clearly show the QFN package to have better thermal characteristics.

The reader is cautioned against assuming a calculated level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted. Great care must be taken to ensure die temperature does not exceed +150°C Absolute Maximum Thermal Limits.

Important Note: The ISL55110 and ISL55111 QFN package metal plane is used for heat sinking of the device. It is electrically connected to the negative supply potential ground.

Power Supply Sequencing

Apply V_{DD}, then V_H.

Power Up Considerations

Digital inputs should never be open. Do not apply slow analog ramps to the inputs. Again, place decoupling as close to the package as possible for both V_{DD} and especially V_H.

Special Loading

With most applications, the user will usually have a special load requirement. Please contact Intersil for evaluation boards or to request a device characterization to your requirements in our lab.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 8, 2013	FN6228.6	Page 5 In Electrical Spec Table changed units from mA to µA II_H Input Current Logic High ENABLE = VDD (QFN only)-
July 9, 2012	FN6228.5	Page 4- Removed “Recommended Operating Conditions table”, which was located above dc electrical spec. table and placed in the abs max ratings table to meet Intersil standards. Page 5 - DC Electrical Spec: Modified IH-PDN parameter (Driver Supply Power-Down Current) Max limit value from 1µ to 2.5µ. Added Revision History table on page 16.
February 9, 2011	FN6228.4	For 8 ld TSSOP, added theta JC value of 46C/W. Added foot note that for TSSOP package theta JC the case temp location is measured in the center of the top of the package.
February 4, 2011		Page 1: Added following sentence to 3rd paragraph: "Both inputs of the device have independent inputs to allow external time phasing if required.” Updated Tape & Reel note in Ordering Information from “Add "-T" suffix for tape and reel.” to new standard “Add "-T*" suffix for tape and reel.” The "*" covers all possible tape and reel options Added MSL note to Ordering Information Page 3: Updated over temp note in Min Max column of spec tables from “Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.” to new standard “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” Page 12: Changed Equation 1 from: P VDD?3.3e-= 3+10pF?VDD2?f+135pF?VH2?f+ (EQ. 1) CL?VH2?f (Watts/Channel) To P VDD 3.3e-= × 3+10pF × VDD2 × f+135pF × VH2 × f+ CL × VH2 (Watts/Channel) (EQ. 1) Page 13: Removed the following sentence from “Power Supply Sequencing”: “The ISL55110, ISL55111 references both VDD and the VH driver supplies with respect to Ground. Therefore, apply VDD, then VH.” Replaced with: “Apply VDD, then VH.” Added subsection “Power Up Considerations” and moved text that was in the “Power Supply Sequencing” section to this section. (“Digital Inputs should...especially VH.”) Page 15- Updated POD M8.173 as follows: Updated to new POD standards as follows: Moved dimensions from table onto drawing. Added Land Pattern. No dimension changes.
March 14, 2008	FN6228.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

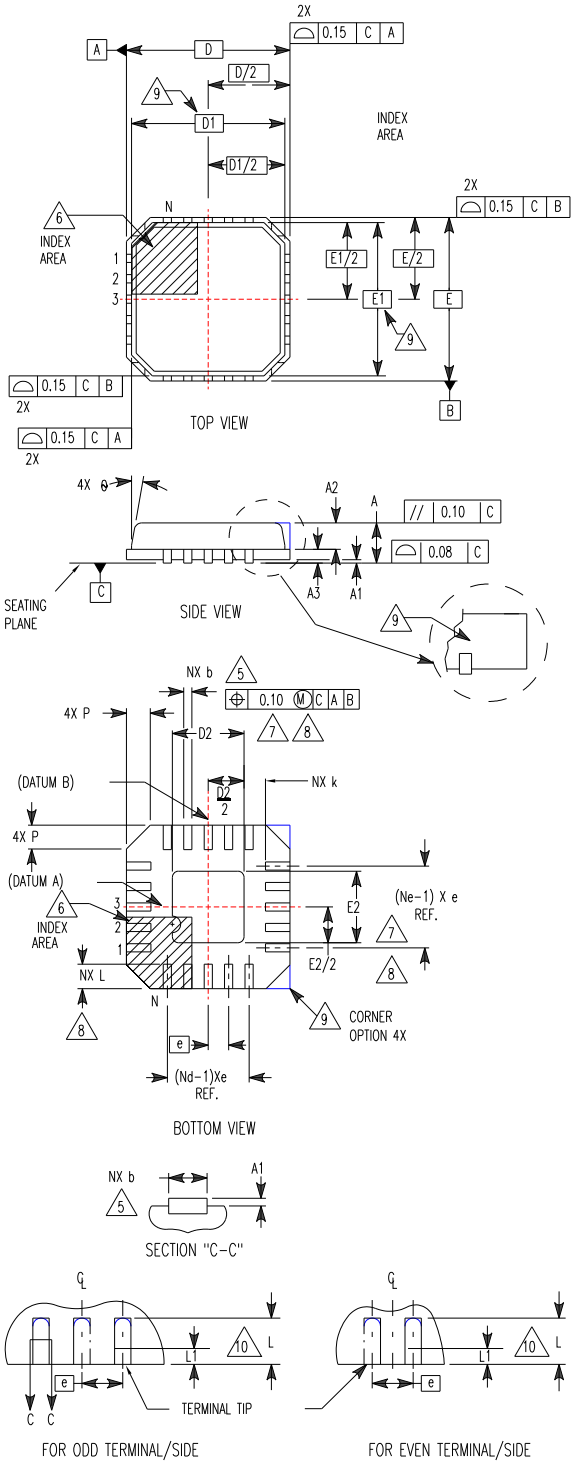
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGD-10)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.30	2.40	2.55	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.30	2.40	2.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
q	-	-	12	9

Rev. 2 3/06

NOTES:

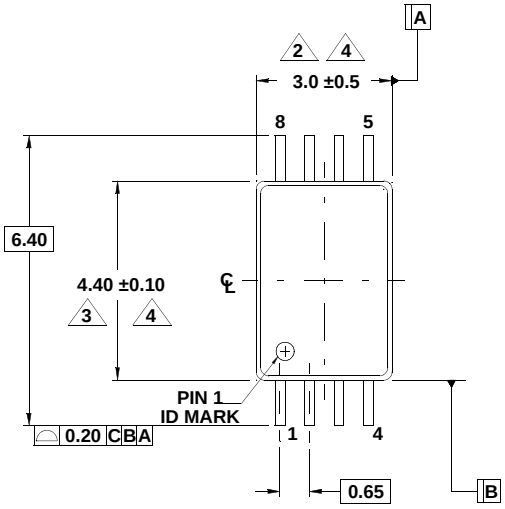
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & q are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Package Outline Drawing

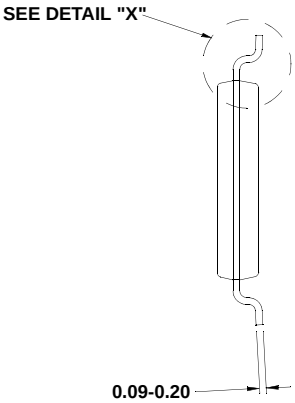
M8.173

8 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

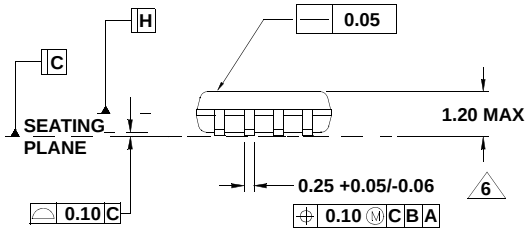
Rev 2, 01/10



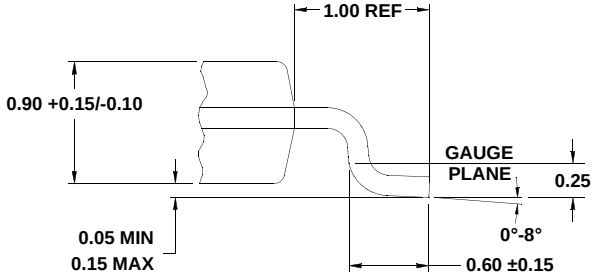
TOP VIEW



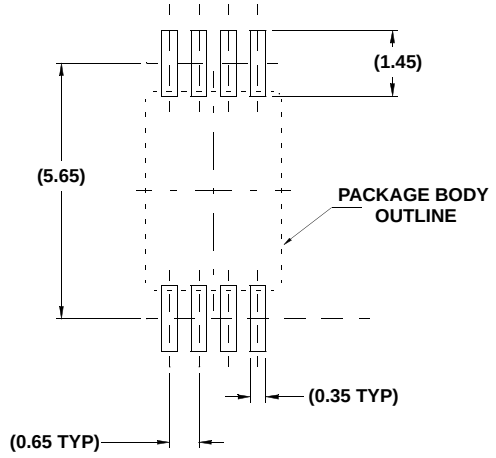
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 per side.
4. Dimensions are measured at datum plane H.
5. Dimensioning and tolerancing per ASME Y14.5M-1994.
6. Dimension on lead width does not include dambar protrusion. Allowable protrusion shall be 0.08 mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
7. Conforms to JEDEC MO-153, variation AC. Issue E