Data Sheet | May 22, 2008 | FN6339.3

Dual and Quad Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Op Amp

The ISL28288 and ISL28488 are dual and quad channel micropower operational amplifiers optimized for single supply operation over the 2.4V to 5.5V range. They can be operated from one lithium cell or two Ni-Cd batteries. For equivalent performance in a single channel op amp, reference EL8188.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages 10% above the positive supply rail and to 100mV below the negative supply. The output operation is rail-to-rail.

The ISL28288 and ISL28488 draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications. The ISL28288 (10 Ld MSOP only) contains a power-down enable pin that reduces the power supply current to typically less than 4µA in the disabled state.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28288FUZ	8288Z	10 Ld MSOP	MDP0043
ISL28288FUZ-T7*	8288Z	10 Ld MSOP Tape and Reel	MDP0043
ISL28288FBZ	28288 FBZ	8 Ld SOIC	MDP0027
ISL28288FBZ-T7*	28288 FBZ	8 Ld SOIC	MDP0027
ISL28488FAZ	28488 FAZ	16 Ld QSOP	MDP0040
ISL28488FAZ-T7*	28488 FAZ	16 Ld QSOP Tape and Reel	MDP0040
ISL28488FVZ	28488 FVZ	14 Ld TSSOP	M14.173
ISL28488FVZ-T7*	28488 FVZ	14 Ld TSSOP Tape and Reel	M14.173
ISL28288EVAL1Z	Evaluation Board - 10 Ld MSOP		
ISL28488EVAL1Z	Evaluation Board - 16 Ld QSOP		

*Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

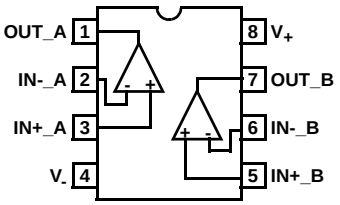
- Low power 120µA typical supply current
- 1.5mV max offset voltage
- 30pA max input bias current
- 300kHz typical gain-bandwidth product
- 105dB typical PSRR
- 100dB typical CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above V_+ and below V_- (ground sensing)
- Rail-to-rail input and output (RRIO)
- Enable Pin - ISL28288 10 Ld MSOP package option only
- Pb-free (RoHS compliant)

Applications

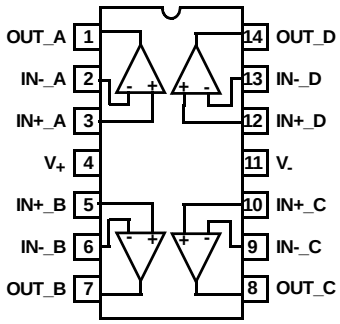
- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

Pinouts

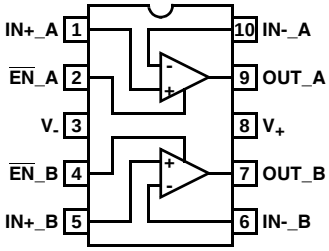
ISL28288
(8 LD SOIC)
TOP VIEW



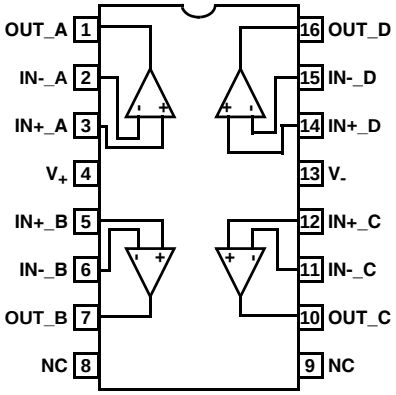
ISL28488
(14 LD TSSOP)
TOP VIEW



ISL28288
(10 LD MSOP)
TOP VIEW



ISL28488
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.75V
Supply Turn On Voltage Slew Rate 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V_- - 0.5V to V_+ + 0.5V
ESD Tolerance
Human Body Model 3kV
Machine Model 300V
Charged Device Model 1200V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
10 Ld MSOP Package	160
16 Ld QSOP Package	100
8 Ld SO Package	125
14 Ld TSSOP Package	115

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage		-1.5 **-2**	±0.05	1.5 **2**	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	ISL28288		1.2		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			0.9		µV/°C
I_{OS}	Input Offset Current	 -40°C to +85°C	-30 **-80**	±5	30 **80**	pA
I_B	Input Bias Current	 -40°C to +85°C	-30 **-80**	±10	30 **80**	pA
CMIR	Common-Mode Voltage Range	Guaranteed by CMRR	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5.5V	85 **80**	105		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	200 **190**	300		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		60		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6 **30**	mV
		Output low, R_L = 1kΩ		130	175 **225**	mV
		Output high, R_L = 100kΩ	4.990 **4.970**	4.996		V
		Output high, R_L = 1kΩ	4.800 **4.750**	4.880		V

Electrical Specifications V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. Temperature data established by characterization (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
$I_{S,ON}$	Quiescent Supply Current, Enabled	ISL28288, All channels enabled.		120	156 **175**	µA
		ISL28488, All channels enabled.		240	315 **350**	µA
$I_{S,OFF}$	Quiescent Supply Current, Disabled (ISL28288)	All channels disabled.		4	7 **9**	µA
I_O+	Short Circuit Sourcing Capability	R_L = 10Ω	24 **20**	31		mA
I_O-	Short Circuit Sinking Capability	R_L = 10Ω		-26	-24 **-20**	mA
V_{SUPPLY}	Supply Operating Range	V_+ to V_-	**2.4**		**5.5**	V
$V_{\overline{ENH}}$	$\overline{EN}$ Pin High Level (ISL28288 10 ld. MSOP)		**2**			V
$V_{\overline{ENL}}$	$\overline{EN}$ Pin Low Level (ISL28288 10 ld. MSOP)				**0.8**	V
$I_{\overline{ENH}}$	$\overline{EN}$ Pin Input High Current (ISL28288 10 ld. MSOP)	$V\overline{EN}$ = V_+		0.8	1 **1.5**	µA
$I_{\overline{ENL}}$	$\overline{EN}$ Pin Input Low Current (ISL28288 10 ld. MSOP)	$V\overline{EN}$ = V_-		0	**+0.1**	µA
AC SPECIFICATIONS						
GBW	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		300		kHz
e_n	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		3		$µV_{P-P}$
	Input Noise Voltage Density	f_O = 1kHz		48		nV/√Hz
i_n	Input Noise Current Density	f_O = 1kHz		9		fA/√Hz
CMRR @ 60Hz	Input Common Mode Rejection Ratio	V_{CM} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-70		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio (V_+)	V_+, V_- = ±1.2V and ±2.5V, V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-80		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio (V_-)	V_+, V_- = ±1.2V and ±2.5V V_{SOURCE} = $1V_{P-P}$, R_L = 10kΩ to V_{CM}		-60		dB
TRANSIENT RESPONSE						
SR	Slew Rate		±0.12 ±**0.09**	±0.14	±0.16 ±**0.21**	V/µs
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% Vout (ISL28288 10 ld. MSOP)	$V\overline{EN}$ = 5V to 0V, A_V = -1, R_G = R_F = R_L = 1k to V_{CM}		2		µs
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% Vout (ISL28288 10 ld. MSOP)	$V\overline{EN}$ = 0V to 5V, A_V = -1, R_G = R_F = R_L = 1k to V_{CM}		0.1		µs

NOTE:

2. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Typical Performance Curves $V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, R_L = Open$

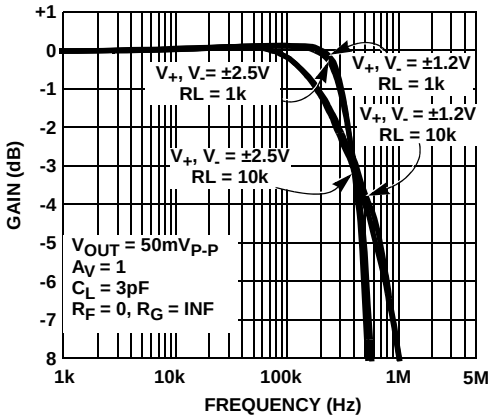


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

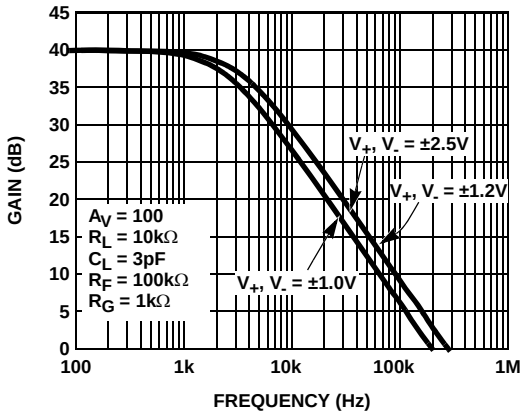


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

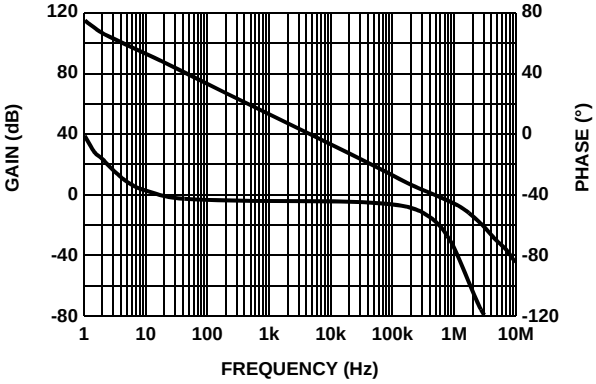


FIGURE 3. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

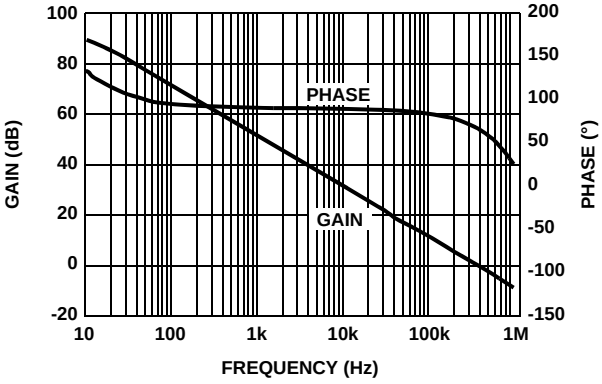


FIGURE 4. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

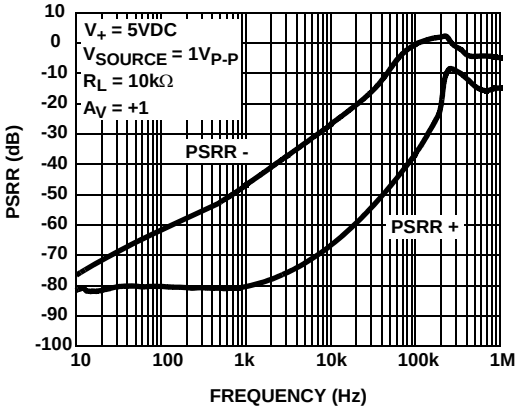


FIGURE 5. PSRR vs FREQUENCY

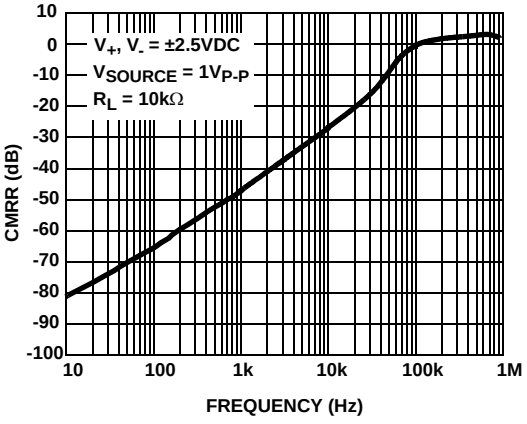


FIGURE 6. CMRR vs FREQUENCY

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

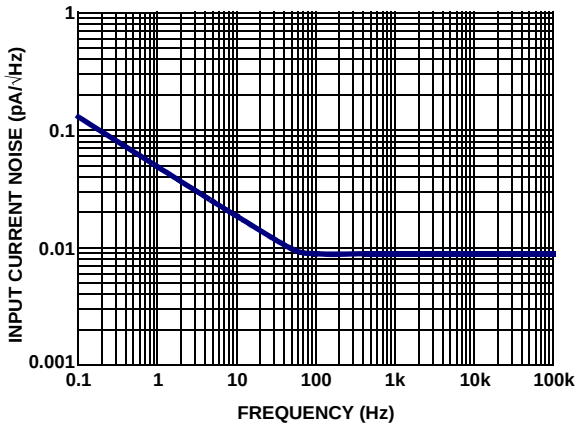


FIGURE 7. CURRENT NOISE vs FREQUENCY

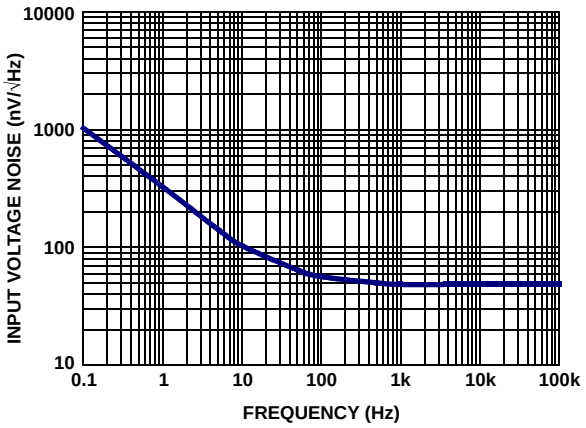


FIGURE 8. VOLTAGE NOISE vs FREQUENCY

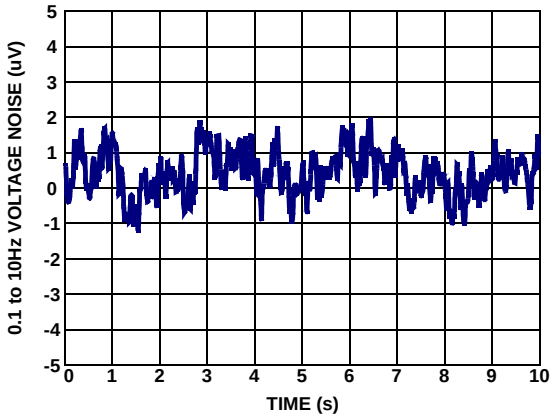


FIGURE 9. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

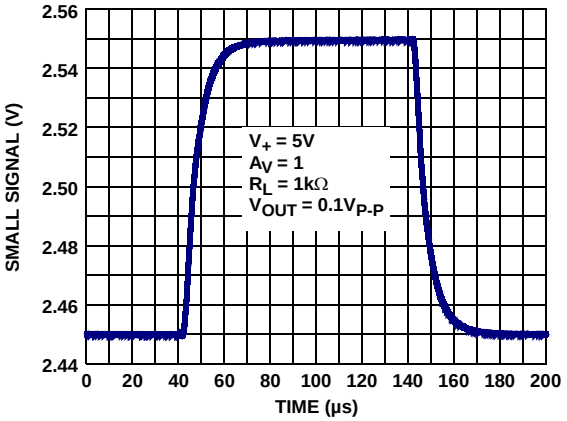


FIGURE 10. SMALL SIGNAL TRANSIENT RESPONSE

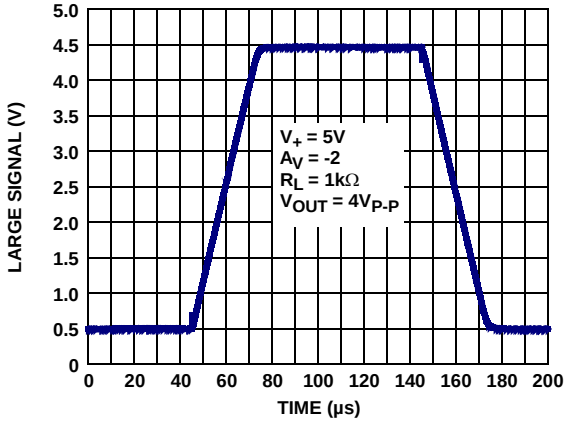


FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE

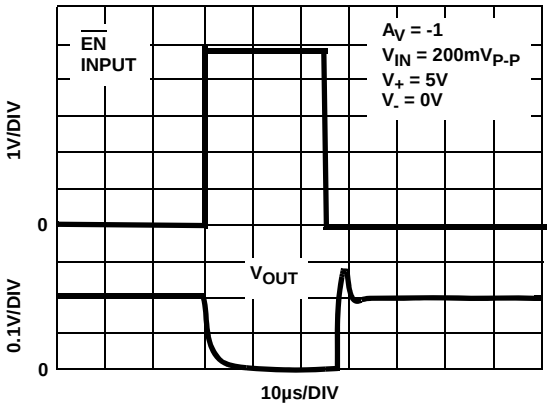


FIGURE 12. ENABLE TO OUTPUT DELAY TIME

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

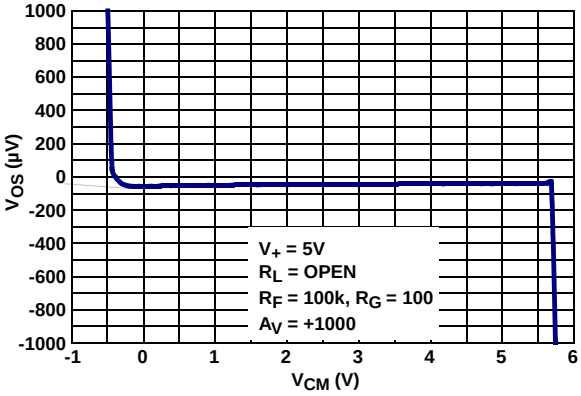


FIGURE 13. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

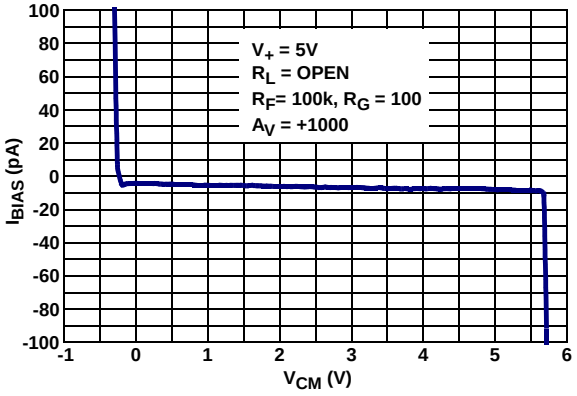


FIGURE 14. INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

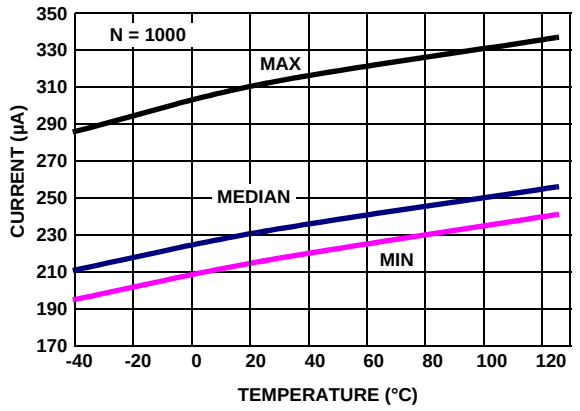


FIGURE 15. ISL28488 SUPPLY CURRENT vs TEMPERATURE V_+, V_- = ±2.5V ENABLED, R_L = INF

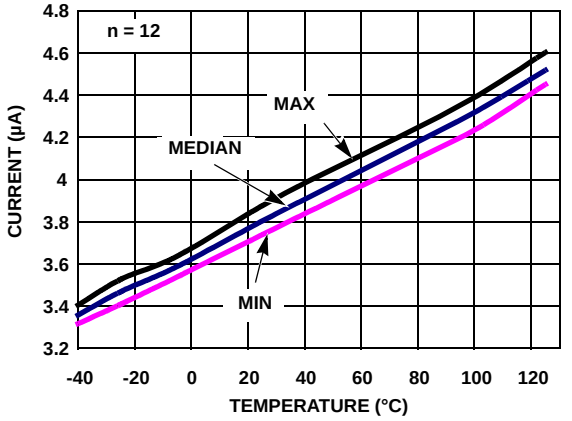


FIGURE 16. ISL28288 SUPPLY CURRENT vs TEMPERATURE V_+, V_- = ±2.5V DISABLED, R_L = INF

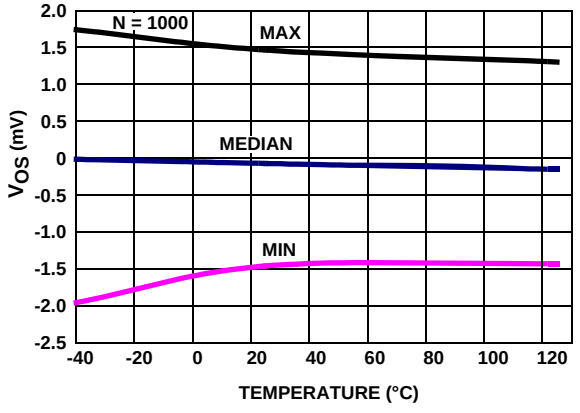


FIGURE 17. V_{OS} vs TEMPERATURE, V_{IN} = 0V, V_+, V_- = ±2.5V

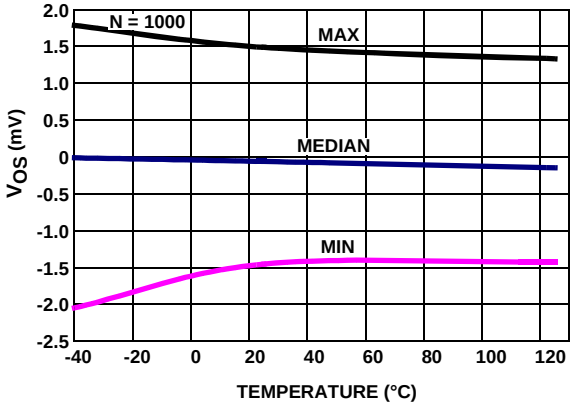


FIGURE 18. V_{OS} vs TEMPERATURE V_{IN} = 0V, V_+, V_- = ±1.2V

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

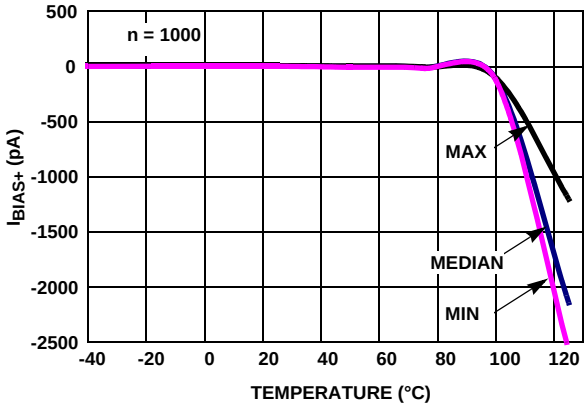


FIGURE 19. I_{BIAS+} vs TEMPERATURE V_+, V_- = ±2.5V

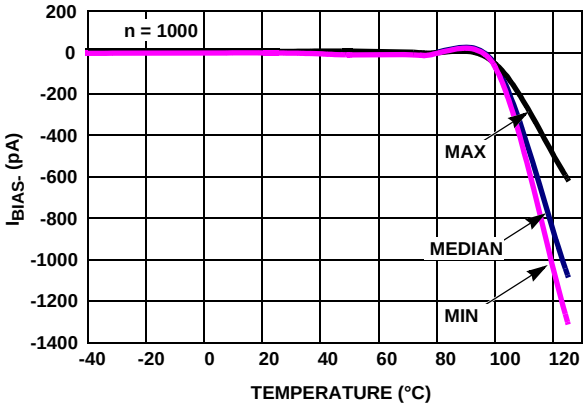


FIGURE 20. I_{BIAS-} vs TEMPERATURE V_+, V_- = ±2.5V

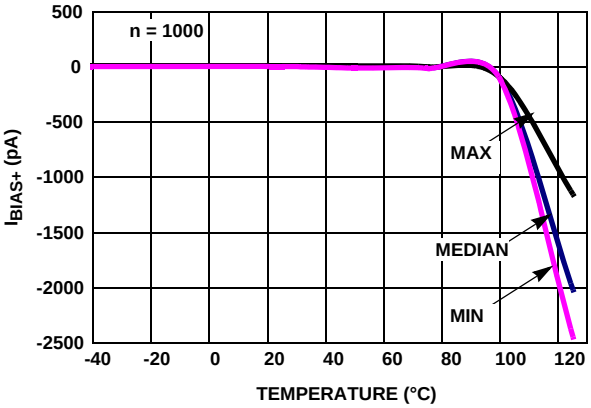


FIGURE 21. I_{BIAS+} vs TEMPERATURE V_+, V_- = ±1.2V

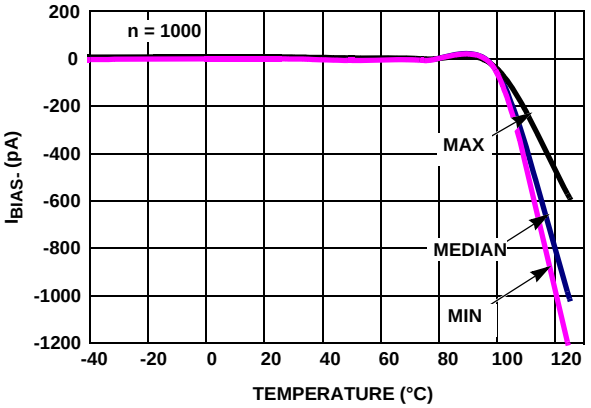


FIGURE 22. I_{BIAS-} vs TEMPERATURE V_+, V_- = ±-1.2V

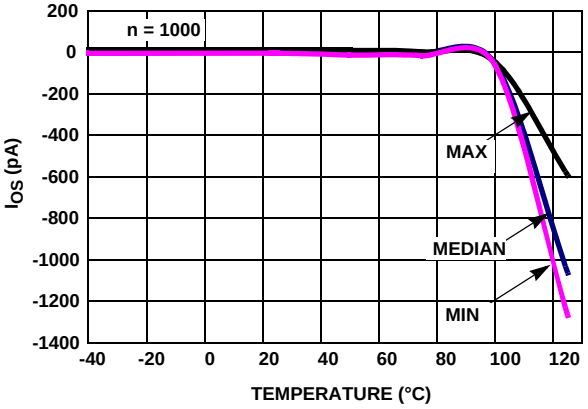


FIGURE 23. I_{OS} vs TEMPERATURE V_+, V_- = ±2.5V

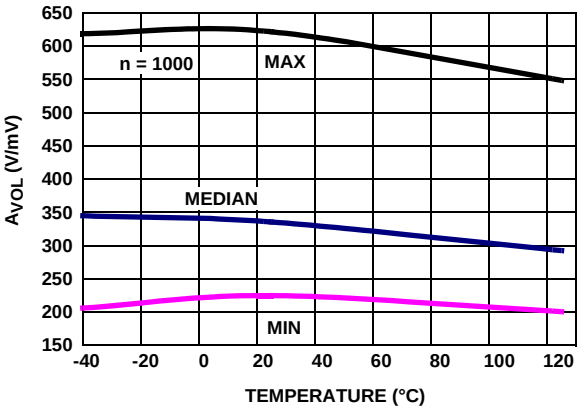


FIGURE 24. A_{VOL} vs TEMPERATURE V_+, V_- = ±2.5V, R_L = 100k

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

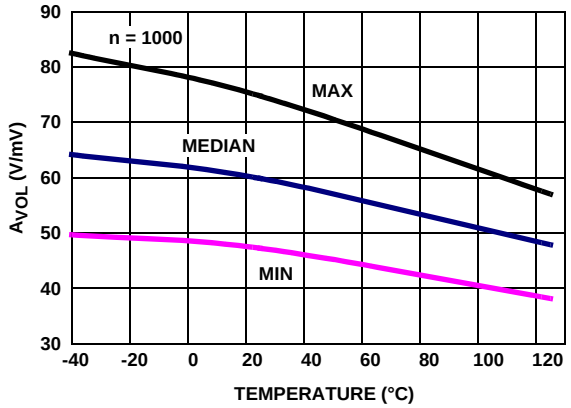


FIGURE 25. A_{VOL} vs TEMPERATURE, V_+, V_- = ±2.5V, R_L = 1k

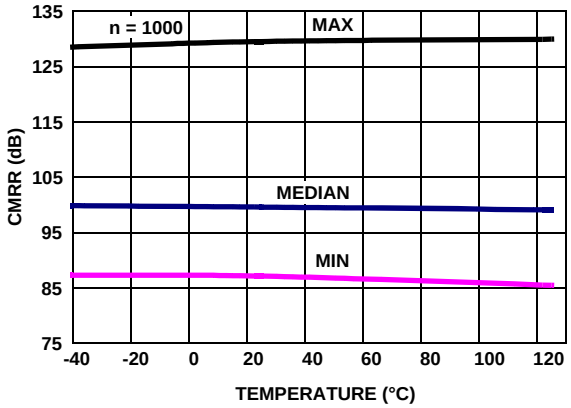


FIGURE 26. CMRR vs TEMPERATURE V_{CM} = +2.5V TO -2.5V, V_+, V_- = ±2.5V

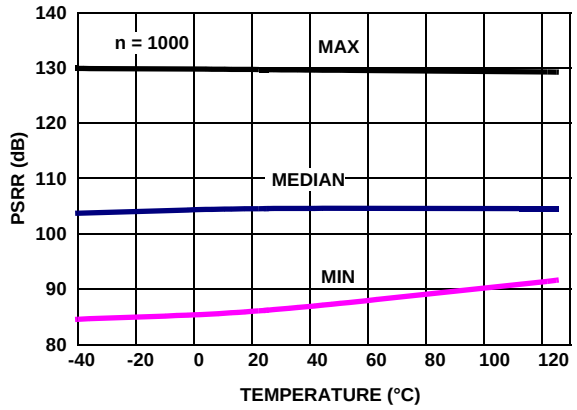


FIGURE 27. PSRR vs TEMPERATURE, V_+, V_- = ±1.2V TO ±2.75V

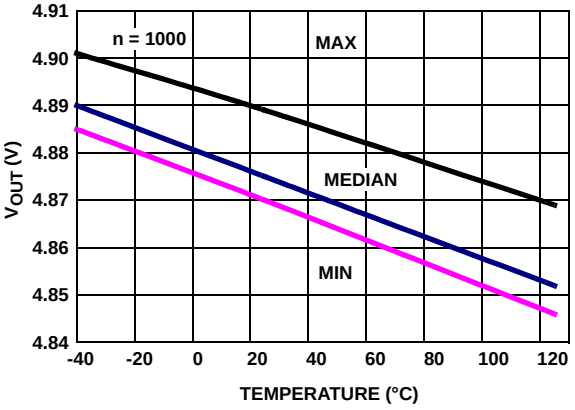


FIGURE 28. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 1k

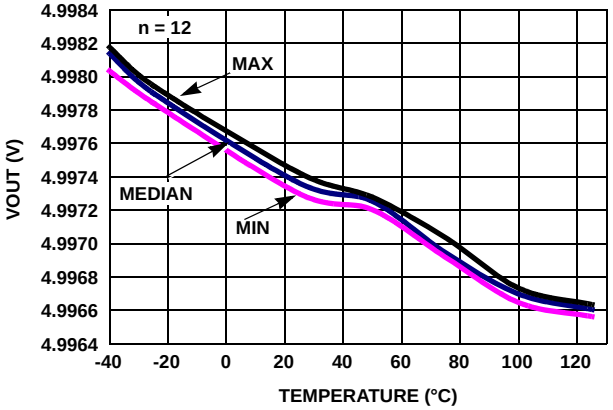


FIGURE 29. V_{OUT} HIGH vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 100k

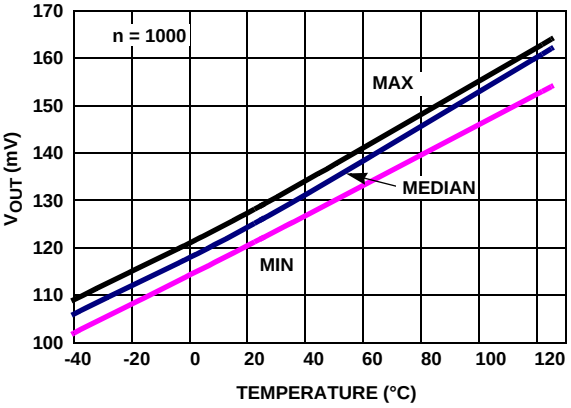


FIGURE 30. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 1k

Typical Performance Curves $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, R_L = Open **(Continued)**

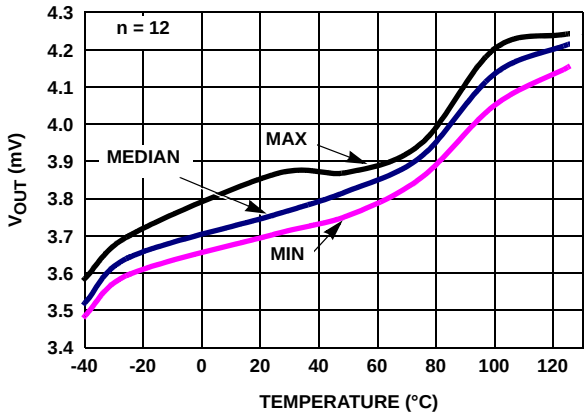


FIGURE 31. V_{OUT} LOW vs TEMPERATURE, V_+, V_- = ±2.5V, R_L= 100k

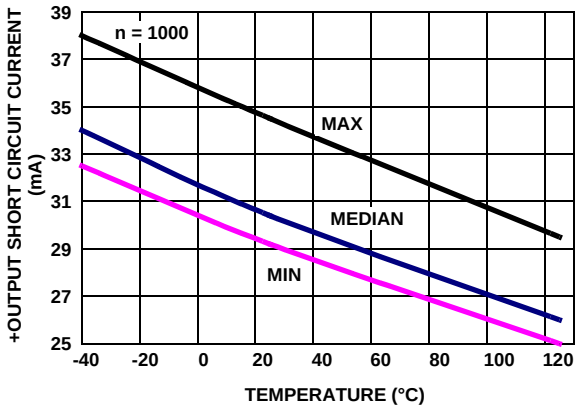


FIGURE 32. +OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE V_{IN} = +2.5V, R_L = 10, V_+, V_- = ±2.5V

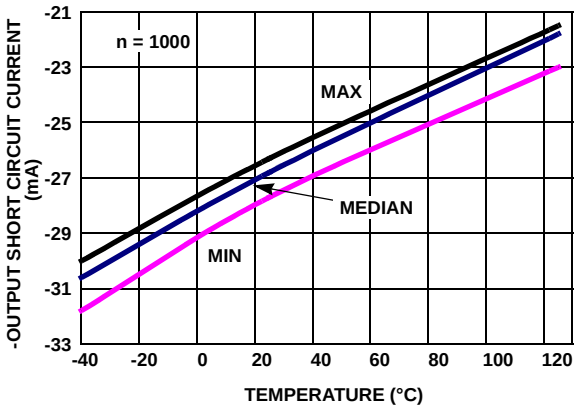


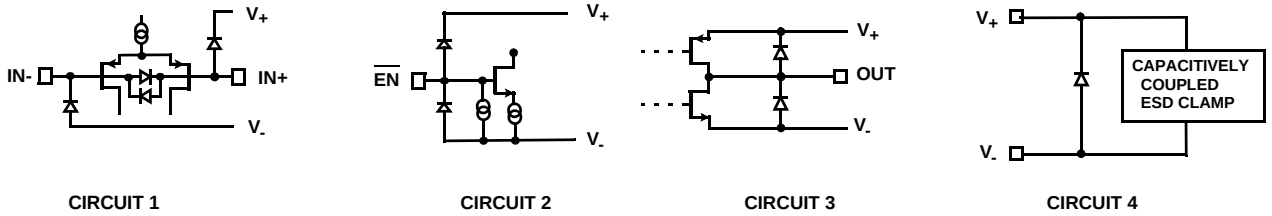
FIGURE 33. -OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE V_{IN} = -2.5V, R_L = 10, V_+, V_- = ±2.5V

Pin Descriptions

ISL28288 (8 LD SOIC)	ISL28288 (10 LD MSOP)	ISL28488 (14 LD TSSOP)	ISL28488 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	1	3	3	IN+_A	Circuit 1	Amplifier A non-inverting input
-	2	-	-	$\overline{EN}$_A	Circuit 2	Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
4	3	11	13	V_-	Circuit 4	Negative power supply
-	4	-	-	$\overline{EN}$_B	Circuit 2	Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
5	5	5	5	IN+_B	Circuit 1	Amplifier B non-inverting input
6	6	6	6	IN-_B	Circuit 1	Amplifier B inverting input
7	7	7	7	OUT_B	Circuit 3	Amplifier B output
8	8	4	4	V_+	Circuit 4	Positive power supply
1	9	1	1	OUT_A	Circuit 3	Amplifier A output

Pin Descriptions (Continued)

ISL28288 (8 LD SOIC)	ISL28288 (10 LD MSOP)	ISL28488 (14 LD TSSOP)	ISL28488 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
2	10	2	2	IN-_A	Circuit 1	Amplifier A inverting input
-	-	8	10	OUT_C	Circuit 3	Amplifier C output
-	-	9	11	IN-_C	Circuit 1	Amplifier C inverting input
-	-	10	12	IN+_C	Circuit 1	Amplifier C non-inverting input
-	-	12	14	IN+_D	Circuit 1	Amplifier D non-inverting input
-	-	13	15	IN-_D	Circuit 1	Amplifier D inverting input
-	-	14	16	OUT_D	Circuit 3	Amplifier D output
-	-	-	8, 9	NC	-	No internal connection



CIRCUIT 1 CIRCUIT 2 CIRCUIT 3 CIRCUIT 4

Applications Information

Introduction

The ISL28288 and ISL28488 are dual and quad CMOS rail-to-rail input, output (RRIO) micropower operational amplifiers. These devices are designed to operate from a single supply (2.4V to 5.5V) or dual supplies (±1.2V to ±2.75V) while drawing only 120µA of supply current. This combination of low power and precision performance makes these devices suitable for solar and battery power applications.

Rail-to-Rail Input

Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

These amplifiers achieve rail-to-rail input operation without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current vs the common-mode voltage range gives us an undistorted behavior from typically 100mV below the negative rail and 10% higher than the V_+ rail (0.5V higher than V_+ when V_+ equals 5.5V).

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. There is an additional pair of back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA.

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. With a 100kΩ load they will swing to within 4mV of the positive supply rail and within 3mV of the negative supply rail.

Enable/Disable Feature

The ISL28288 (only MSOP package option), offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 4µA. By disabling the part, multiple ISL28288 parts can be connected together as a MUX. In this configuration, the outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. The $\overline{EN}$ pin also has an internal pull-down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

Using Only One Channel

If the application only requires one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 34).

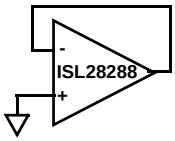


FIGURE 34. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 35 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

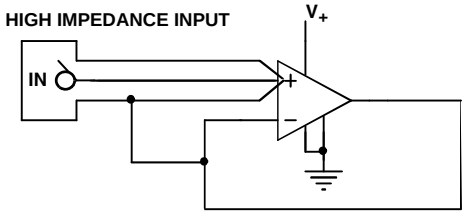


FIGURE 35. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Current Limiting

The ISL28288 has no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} x PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier is calculated in Equation 2:

$$PD_{MAX} = 2*V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Supply voltage (Magnitude of V_+ and V_-)
- I_{MAX} = Maximum supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

Application Circuits

THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28x88 (see Figure 36) is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The amplifier's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the amplifier to run from a single 5V supply.

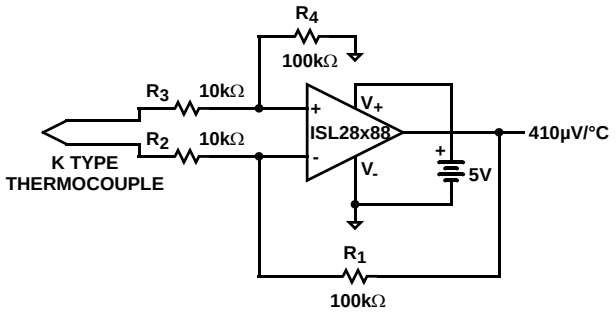


FIGURE 36. THERMOCOUPLE AMPLIFIER

ECG AMPLIFIER

ECG amplifiers must extract millivolt low frequency AC signals from the skin of the patient while rejecting AC common mode interference and static DC potentials created at the electrode-to-skin interface. In Figure 37, the ISL28288 (U1) forms one of the multiple high gain AC band-pass amplifiers using active feedback. Amplifier U1B and RC RF1, CF1 form a high gain LP filtered amplifier with the corner frequency given by Equation 3:

$$f\text{-}HPF_{-3dB} = \frac{1}{2 \times Pi \times RF1 \times CF1} \quad \text{(EQ. 3)}$$

Inserting the low pass amplifier, U1B, in U1A's feedback loop results in an overall high-pass frequency response. Voltage divider pairs R1-R2 and R3-R4 set the overall amplifier pass-band gain. The DC input offset is cancelled by U1B at U1A's inverting input. Resistor divider pair, R3-R4 define the maximum input DC level that is cancelled, and is given by Equation 4:

$$V_{IN}DC = V_+ \times \left(\frac{R_4}{R_3 + R_4}\right) \quad \text{(EQ. 4)}$$

In the passband range, U1B's gain is +1 and the total signal gain is defined by the divider ratios according to Equation 5:

$$V_{OUT}U1\ GAIN = \frac{V_{OUT}}{V_{IN}} = \left(\frac{R_1 + R_2}{R_2}\right) \times \left(\frac{R_3 + R_4}{R_4}\right) \quad \text{(EQ. 5)}$$

At frequencies greater than the LPF corner, the R1-C1 and R3-C3 networks roll off U1A's gain to unity. Setting both R-C time constants to the same value simplifies to Equation 6:

$$f\text{-}LPF_{-3dB} = \frac{1}{2 \times Pi \times R_1 \times C_1} \quad \text{(EQ. 6)}$$

Right leg drive and reference amplifiers U2A and U2B form a DC feedback loop that applies a correction voltage at the Right Leg electrode to cancel out DC and low frequency body interference. The voltage at the V_{CM} sense electrode is maintained at the reference voltage set by RF1-RF2.

With the values shown in Figure 37, the ECG circuit performance parameters are:

1. Supply Voltage Range = +2.4V to +5.5V
2. Total Supply Current Draw @ +5V = 500µA (typ)
3. Common-Mode Reference Voltage (V_{CM}) = $V_+/2$
4. Max DC Input Offset Voltage = V_{CM} ±0.18V to ±0.41V
5. Passband Gain = 425V/V
6. Lower -3dB Frequency = 0.05Hz
7. Upper -3dB Frequency = 159Hz

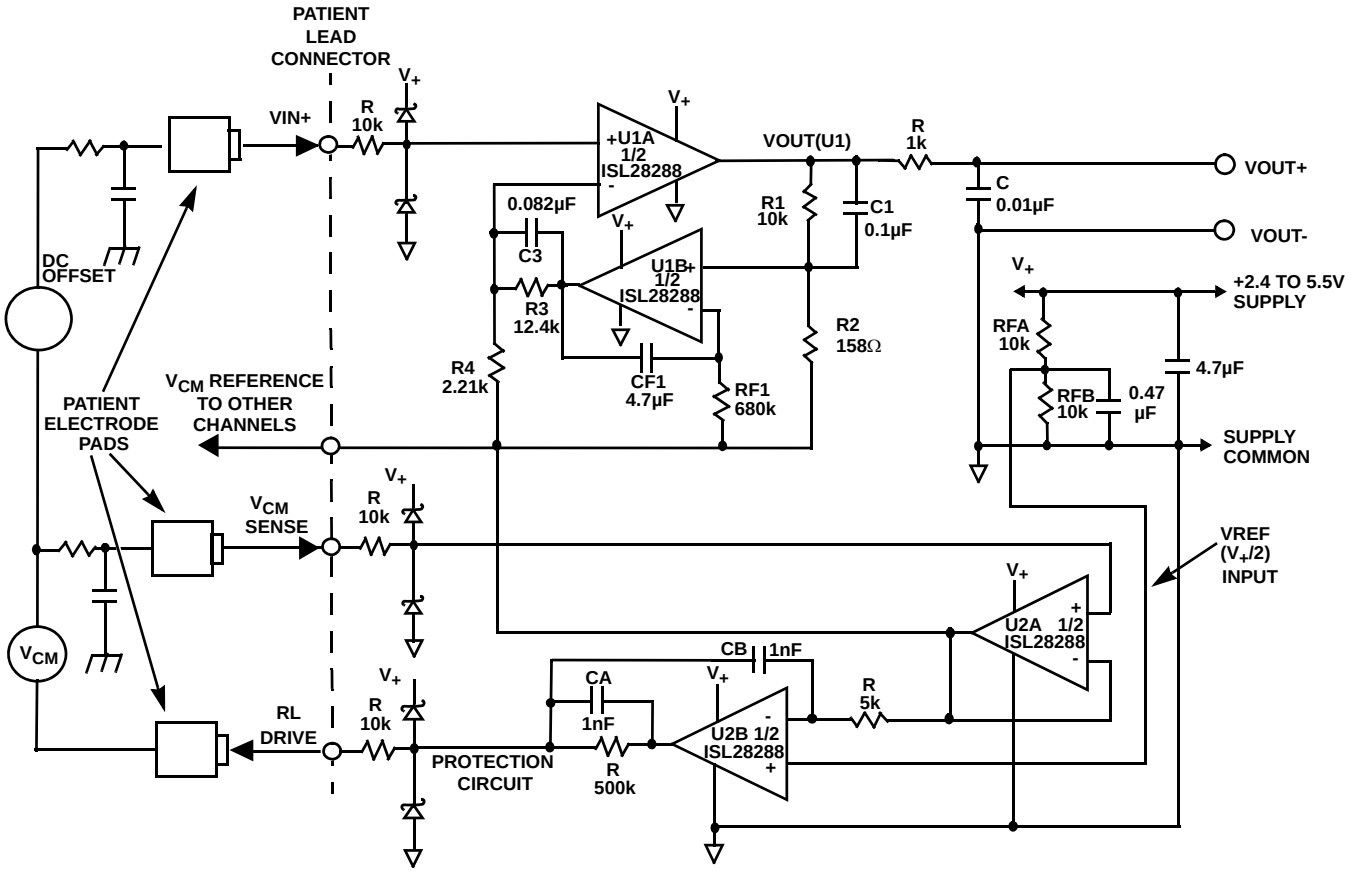
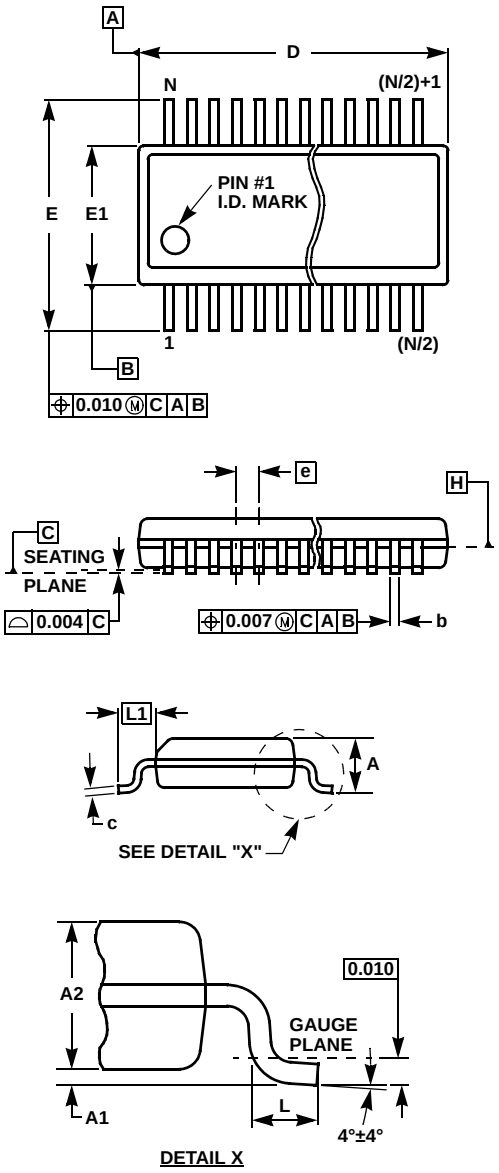


FIGURE 37. ECG AMPLIFIER

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

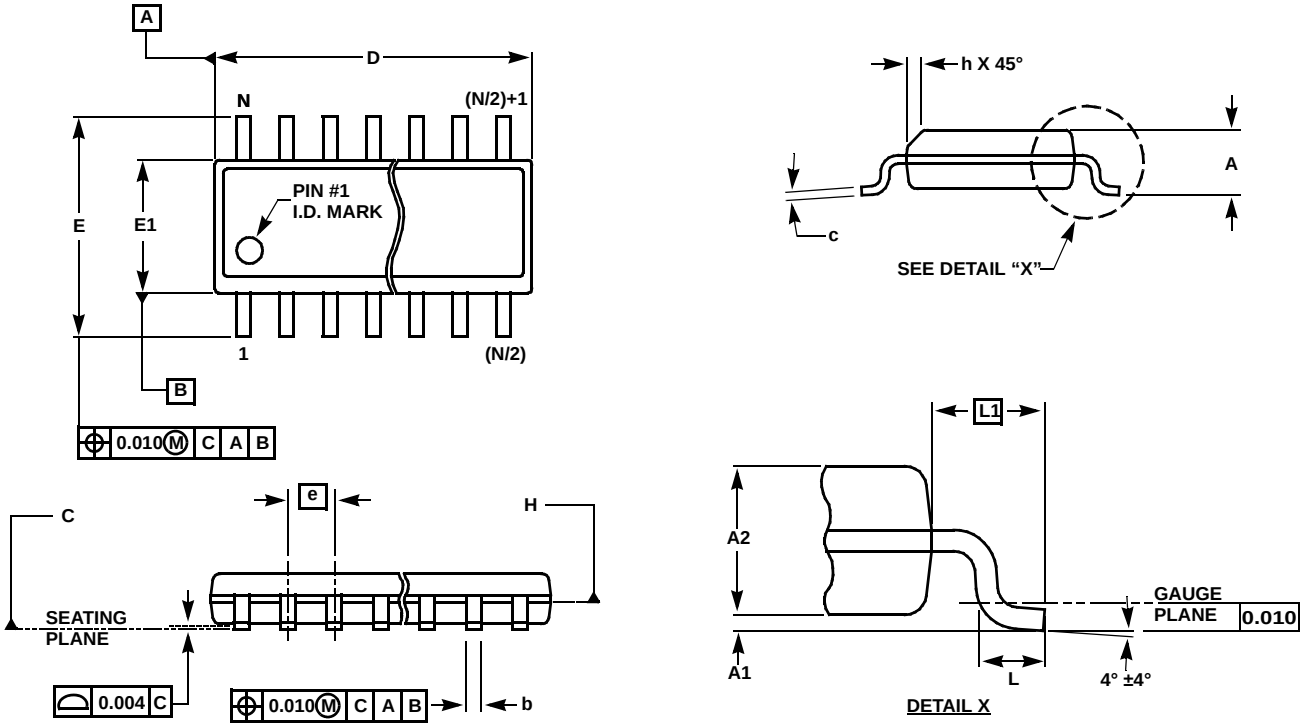
SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

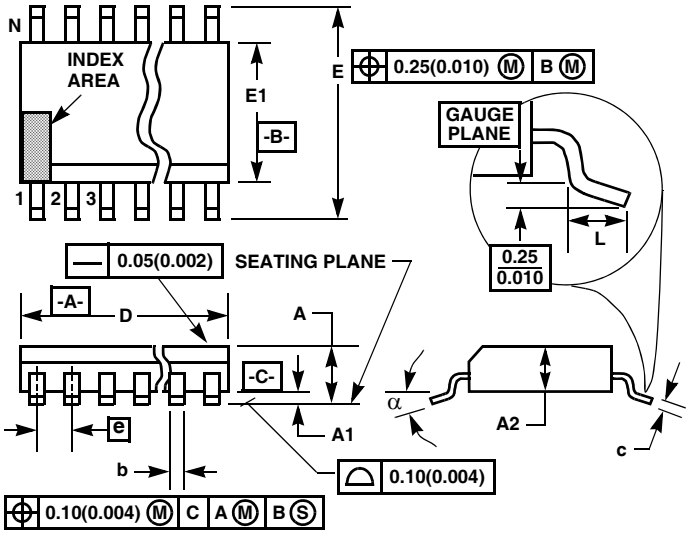
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

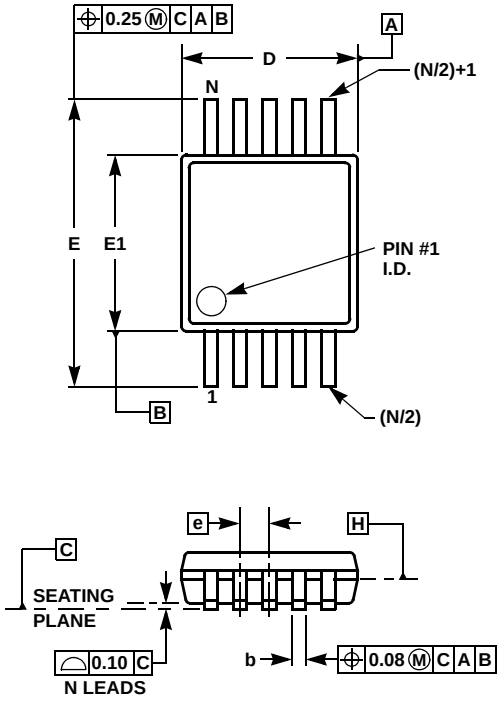
M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.