25AA320

32K 1.8V SPI™ Bus Serial EEPROM

FEATURES

- SPI modes 0,0 and 1,1
- 3.0 MHz Clock Rate
- Single supply with Programming Operation down to 1.8V
- Low Power CMOS Technology
  - Max Write Current: 5.0 mA
  - Read Current: 1.0 mA@ 5.5V 3 Mhz
  - Standby Current: 1 μA typical
- 4096 x 8 Organization
- 32-Byte Page
- Sequential Read
- Self-timed ERASE and WRITE Cycles
- Block Write Protection
  - Protect none, 1/4, 1/2, or all of Array
- Built-in Write Protection
  - Power On/Off Data Protection Circuitry
  - Write Enable Latch
  - Write Protect Pin
- High Reliability
  - Endurance: 1M cycles (guaranteed)
  - Data Retention: >200 years
  - ESD protection: >4000V
- 8-pin PDIP/SOIC, 14-pin TSSOP
- Temperature ranges supported:
  - Commercial (C): 0°C to +70°C
  - Industrial (I) -40°C to +85°C

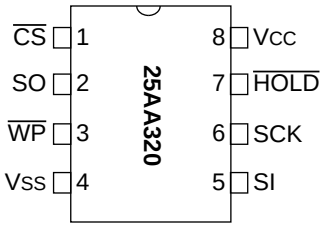
DESCRIPTION

The Microchip Technology Inc. 25AA320 is a 32K-bit serial Electrically Erasable PROM (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

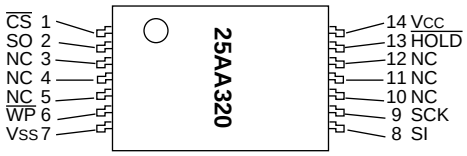
There are two other inputs that provide the end user with additional flexibility. Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of chip select, allowing the host to service higher priority interrupts. Also, write operations to the Status Register can be disabled via the write protect pin ($\overline{WP}$).

PACKAGE TYPES

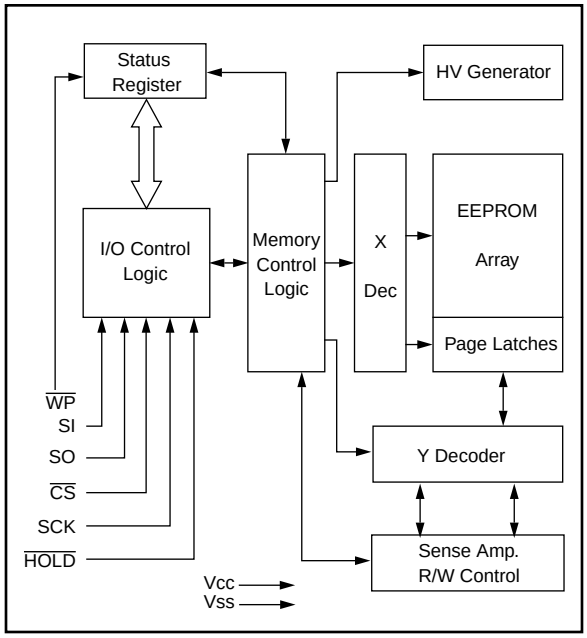
DIP/SOIC



TSSOP



BLOCK DIAGRAM



SPI is a trademark of Motorola.

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

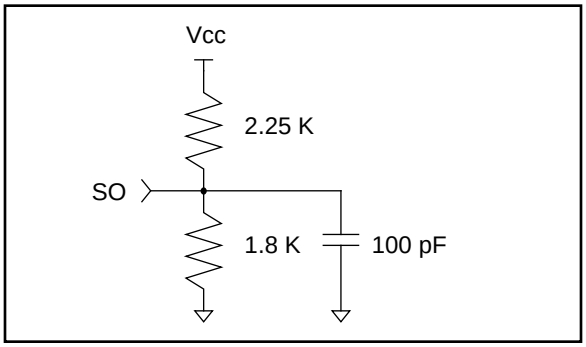
VCC.....7.0V
All inputs and outputs w.r.t. VSS.....-0.6V to V_{CC}+1.0V
Storage temperature .....-65°C to 150°C
Ambient temperature under bias.....-65°C to 125°C
Soldering temperature of leads
(10 seconds) .....+300°C
ESD protection on all pins.....4 kV

***Notice:** Stresses above those listed under 'Maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended period of time may affect device reliability

FIGURE 1-1: PIN FUNCTION TABLE

Name	Function
$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Pin
VSS	Ground
VCC	Supply Voltage
$\overline{HOLD}$	Hold Input
NC	No Connect

FIGURE 1-2: AC TEST CIRCUIT



1.2 AC Test Conditions

AC Waveform:
VLO = 0.2V
VHI = Vcc - 0.2V (Note 1)
VHI = 4.0V (Note 2)

Timing Measurement Reference Level
Input 0.5 VCC
Output 0.5 VCC

Note 1: For VCC ≤ 4.0V
2: For VCC > 4.0V

TABLE 1-1: DC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
VCC = +1.8V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb =-40°C to +85°C

Parameter	Symbol	Min	Max	Units	Test Conditions
High level input voltage	VIH1	2.0	VCC+1	V	VCC ≥ 2.7V
	VIH2	0.7 VCC	VCC+1	V	VCC< 2.7V
Low level input voltage	VIL1	-0.3	0.8	V	VCC ≥ 2.7V
	VIL2	-0.3	0.3 VCC	V	VCC< 2.7V
Low level output voltage	VOL	—	0.4	V	IOL=2.1 mA
High level output voltage	VOH	VCC-0.5	—	V	IOH=-400 µA
Input leakage current	ILI	-10	10	µA	$\overline{CS}$=VIH, VIN=GND to VCC
Output leakage current	ILO	-10	10	µA	$\overline{CS}$=VIH, V_{OUT}=GND to VCC
Internal Capacitance (all inputs and outputs)	CINT	—	7	pF	Tamb=25°C, FCLK=1.0 MHz, VCC=5.5V (Note)
Operating Current	Icc Write	— —	5 3	mA mA	VCC=5.5V; SO=Open VCC=2.5V; SO=Open
	ICC Read	— —	1 500	mA µA	VCC=5.5V; SO=Open, FCLK=3.0 MHz VCC=2.5V; SO=Open, FCLK=2.0 MHz
Standby Current	ICCS	—	5 2	µA µA	$\overline{CS}$=VCC=5.5V; VIN=GND or VCC $\overline{CS}$=VCC=2.5V; VIN=GND or VCC

Note: This parameter is periodically sampled and not 100% tested.

FIGURE 1-3: SERIAL INPUT TIMING

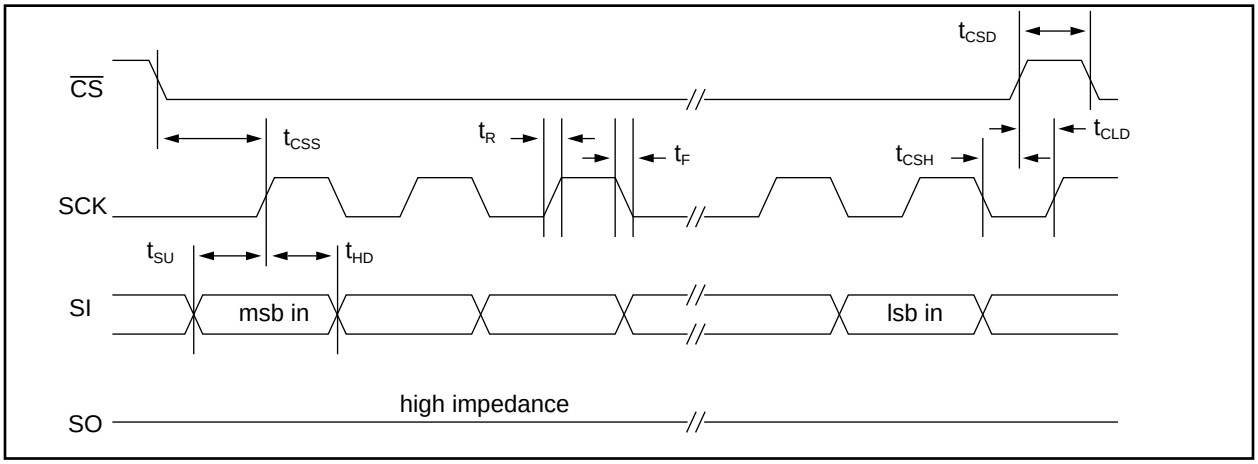


FIGURE 1-4: SERIAL OUTPUT TIMING

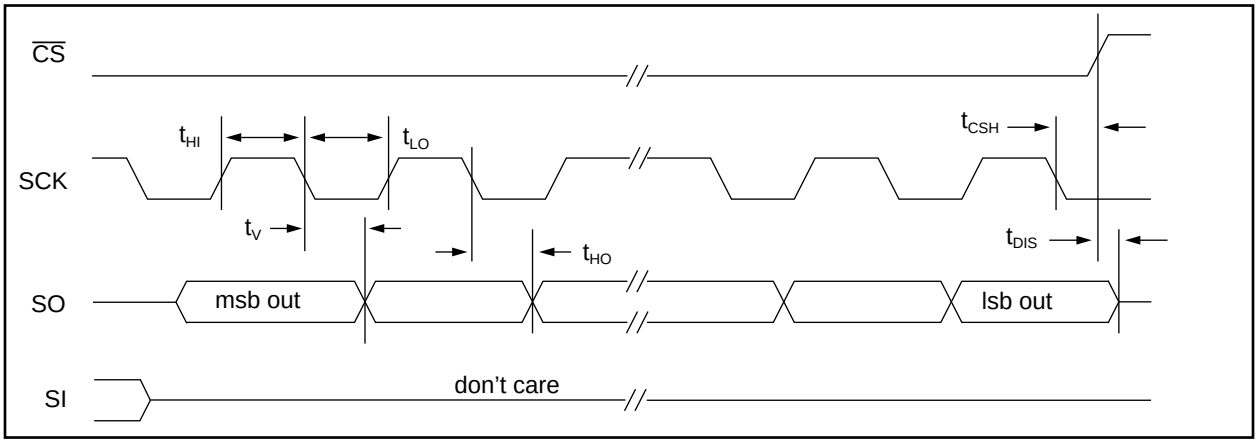


FIGURE 1-5: HOLD TIMING

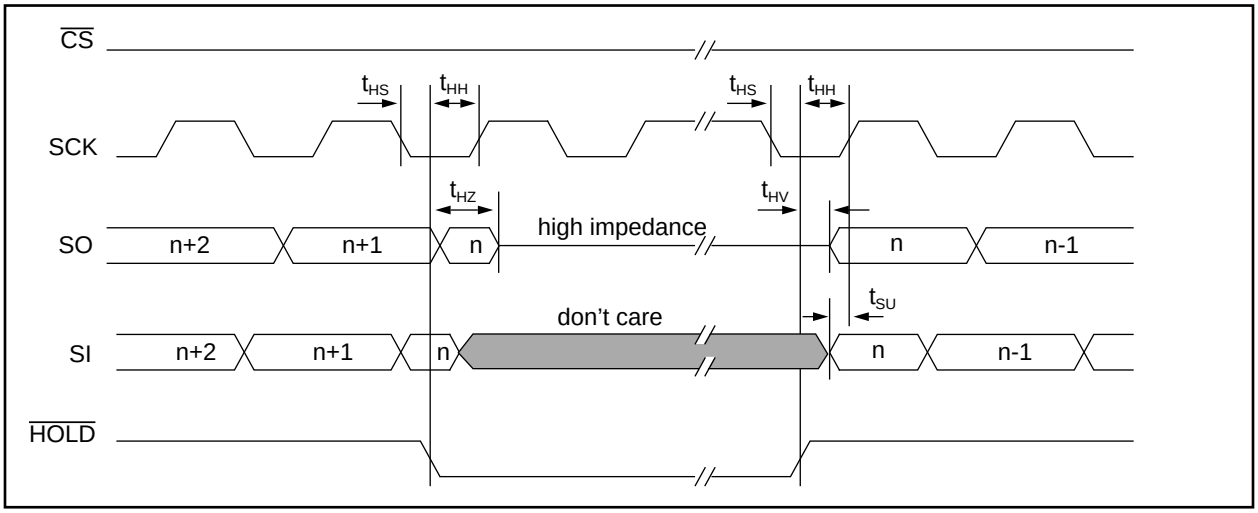


TABLE 1-2: AC CHARACTERISTICS

Applicable over recommended operating ranges shown below unless otherwise noted:
VCC = +1.8V to 5.5V
Commercial (C): Tamb = 0°C to +70°C
Industrial (I) Tamb = -40°C to +85°C

Symbol	Parameter	Min	Max	Units	Test Conditions
fSCK	Clock Frequency	—	3	MHz	VCC=4.5V to 5.5V
		—	2	MHz	VCC=2.5V to 4.5V
		—	1	MHz	VCC=1.8V to 2.5V
tCSS	CS Setup Time	100	—	ns	VCC=4.5V to 5.5V
		250	—	ns	VCC=2.5V to 4.5V
		500	—	ns	VCC=1.8V to 2.5V
tCSH	CS Hold Time	100	—	ns	VCC=4.5V to 5.5V
		250	—	ns	VCC=2.5V to 4.5V
		500	—	ns	VCC=1.8V to 2.5V
tCSD	CS Disable Time	250	—	ns	VCC=4.5V to 5.5V
		500	—	ns	VCC=2.5V to 4.5V
		500	—	ns	VCC=1.8V to 2.5V
tSU	Data Setup Time	30	—	ns	VCC=4.5V to 5.5V
		50	—	ns	VCC=2.5V to 4.5V
		50	—	ns	VCC=1.8V to 2.5V
tHD	Data Hold Time	50	—	ns	VCC=4.5V to 5.5V
		100	—	ns	VCC=2.5V to 4.5V
		100	—	ns	VCC=1.8V to 2.5V
tR	CLK Rise Time	—	2	µs	(Note 1)
tF	CLK Fall Time	—	2	µs	(Note 1)
tHI	Clock High Time	150	—	ns	VCC=4.5V to 5.5V
		250	—	ns	VCC=2.5V to 4.5V
		475	—	ns	VCC=1.8V to 2.5V
tLO	Clock Low Time	150	—	ns	VCC=4.5V to 5.5V
		250	—	ns	VCC=2.5V to 4.5V
		475	—	ns	VCC=1.8V to 2.5V
tCLD	Clock Delay Time	50	—	ns	
tV	Output Valid from Clock Low	—	150	ns	VCC=4.5V to 5.5V
		—	250	ns	VCC=2.5V to 4.5V
		—	475	ns	VCC=1.8V to 2.5V
tHO	Output Hold Time	0	—	ns	
tDIS	Output Disable Time	—	200	ns	VCC=4.5V to 5.5V (Note 1)
		—	250	ns	VCC=2.5V to 4.5V (Note 1)
		—	500	ns	VCC=1.8V to 2.5V (Note 1)
tHS	HOLD Setup Time	100	—	ns	VCC=4.5V to 5.5V
		100	—	ns	VCC=2.5V to 4.5V
		200	—	ns	VCC=1.8V to 2.5V
tHH	HOLD Hold Time	100	—	ns	VCC=4.5V to 5.5V
		100	—	ns	VCC=2.5V to 4.5V
		200	—	ns	VCC=1.8V to 2.5V
tHZ	HOLD Low to Output High-Z	100	—	ns	VCC=4.5V to 5.5V (Note 1)
		150	—	ns	VCC=2.5V to 4.5V (Note 1)
		200	—	ns	VCC=1.8V to 2.5V (Note 1)
tHV	HOLD High to Output Valid	100	—	ns	VCC=4.5V to 5.5V (Note 1)
		150	—	ns	VCC=2.5V to 4.5V (Note 1)
		200	—	ns	VCC=1.8V to 2.5V (Note 1)
tWC	Internal Write Cycle Time	—	5	ms	(Note 2)
—	Endurance	1M	—	E/W Cycles	25°C, Vcc = 5.0V, Block Mode (Note 3)

Note 1: This parameter is periodically sampled and not 100% tested.
2: tWC begins on the rising edge of CS after a valid write sequence and ends when the internal self-timed write cycle is complete.
3: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

2.0 PRINCIPLES OF OPERATION

The 25AA320 is a 4096 byte EEPROM designed to interface directly with the serial peripheral interface (SPI) port of many of today's popular microcontroller families, including Microchip's midrange PIC16CXX microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with software.

The 25AA320 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. If the WPEN bit in the status register is set, the $\overline{WP}$ pin must be held high to allow writing to the non-volatile bits in the status register.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the 25AA320 in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

2.1 Write Enable (WREN) and Write Disable (WRDI)

The 25AA320 contains a write enable latch. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch. The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

2.2 Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25AA320 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1' the latch allows writes to the array and status register, when set to a '0' the latch prohibits writes to the array and status register. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write protected. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

The **Write Protect Enable (WPEN)** bit is a non-volatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write Protect ($\overline{WP}$) pin and the Write Protect Enable (WPEN) bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write protected, only writes to non-volatile bits in the status register are disabled. See Table 2-2 for matrix of functionality on the WPEN bit and Figure 2-1 for a flowchart of Table 2-2.

See Figure 3-5 for RDSR timing sequence.

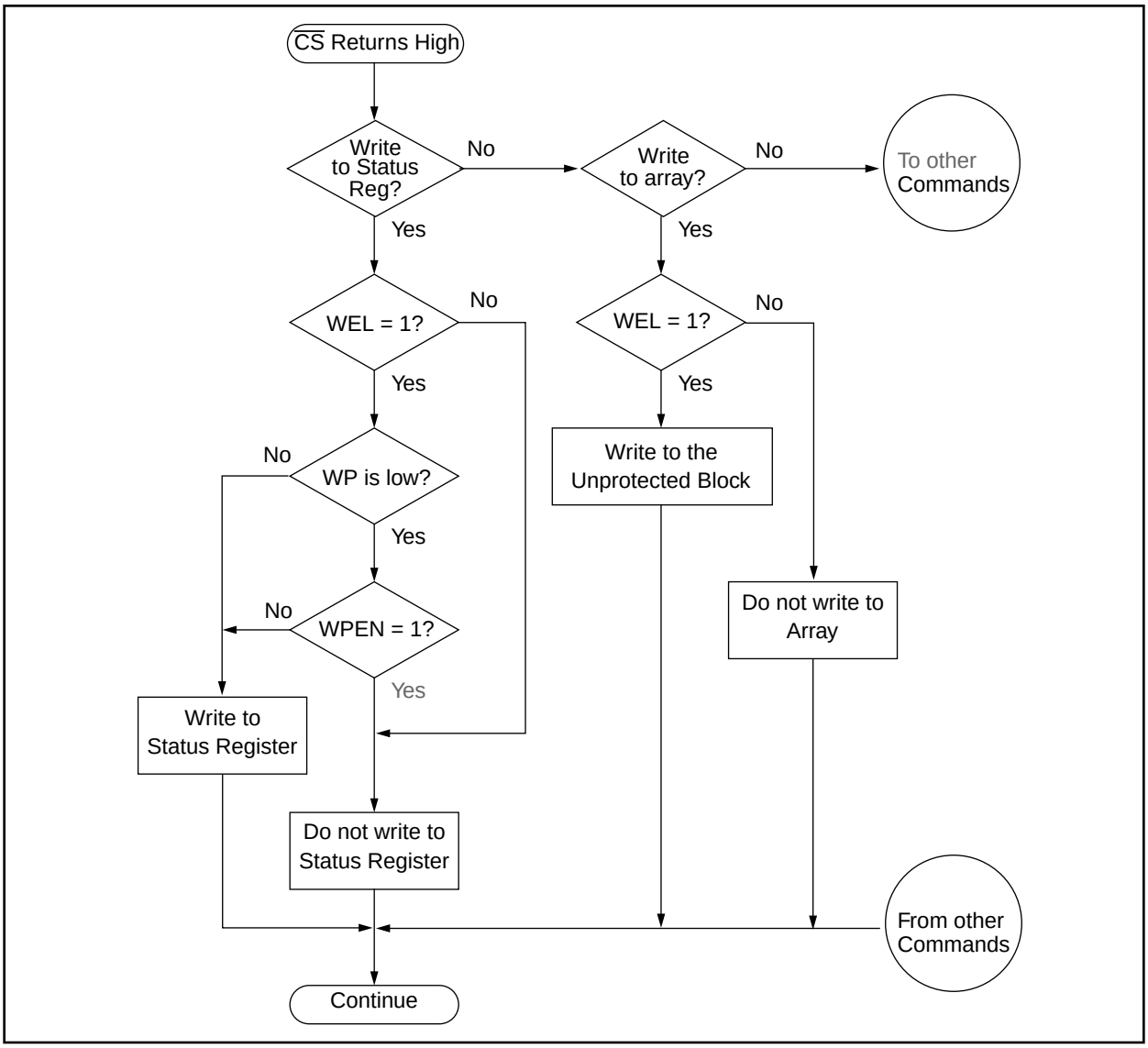
TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read status register
WRSR	0000 0001	Write status register (write protect enable and block write protection bits)
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address

TABLE 2-2: WRITE PROTECT FUNCTIONALITY MATRIX

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

FIGURE 2-1: WRITE TO STATUS REGISTER AND/OR ARRAY FLOWCHART



2.3 Write Status Register (WRSR)

The WRSR instruction allows the user to select one of four protection options for the array by writing to the appropriate bits in the status register. The array is divided up into four segments. The user has the ability to write protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 2-3.

See Figure 3-6 for WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write Protected
0	0	none
0	1	upper 1/4 0C00h - 0FFFh
1	0	upper 1/2 0800h - 0FFFh
1	1	all 0000h - 0FFFh

3.0 DEVICE OPERATION

3.1 Clock and Data Timing

Data input on the SI pin is latched on the rising edge of SCK. Data is output on the SO pin after the falling edge of SCK.

3.2 Read Sequence

The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25AA320 followed by the 16-bit address, with the four MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (0FFFh) the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by setting $\overline{CS}$ high (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25AA320, the write enable latch must be set by issuing the WREN instruction (Figure 3-2). This is done by setting $\overline{CS}$ low and then clocking the proper instruction into the 25AA320. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a write instruction, followed by the 16-bit address, with the four MSBs of the address being don't care bits, and then the data to be written. Up to 32 bytes of data can be sent to the 25AA320 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX XXXX XXX0 0000 and ends with XXXX XXXX XXX1 1111. If the internal address counter reaches XXXX XXXX XXX1 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-3 and Figure 3-4 for more detailed illustrations on the byte write sequence and the page write sequence respectively.

While the write is in progress, the status register may be read to check the status of the WPEN, WIP, WEL, BP1, and BP0 bits. A read attempt of a memory array location will not be possible during a write cycle. When a write cycle is completed, the write enable latch is reset.

3.4 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up.
- A write enable instruction must be issued to set the write enable latch.
- After a successful byte write, page write, or status register write, the write enable latch is reset.
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle.
- Access to the array during an internal write cycle is ignored and programming is continued.

3.5 Power On State

The 25AA320 powers on in the following state:

- The device is in low power standby mode ($\overline{CS}$=1).
- The write enable latch is reset.
- SO is in high impedance state.
- A low level on $\overline{CS}$ is required to enter active state.

FIGURE 3-1: READ SEQUENCE

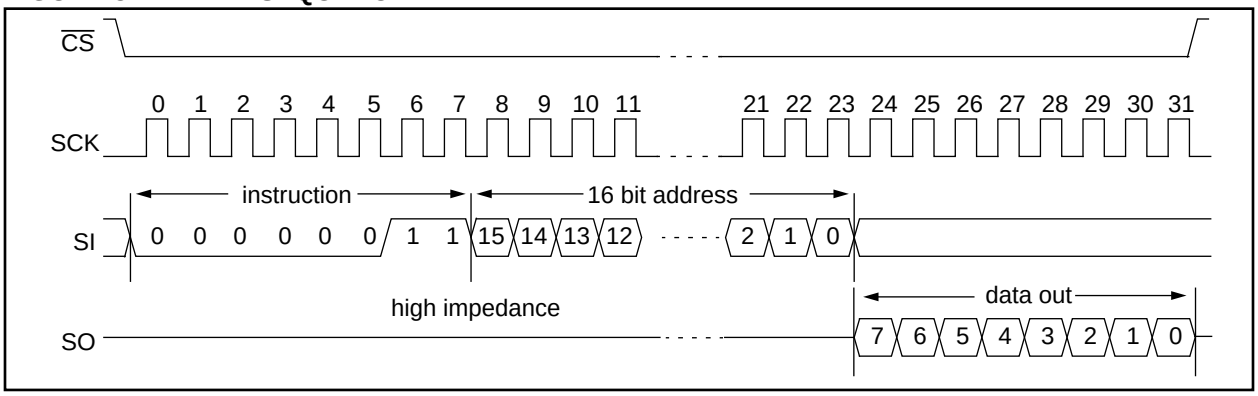


FIGURE 3-2: WRITE ENABLE SEQUENCE

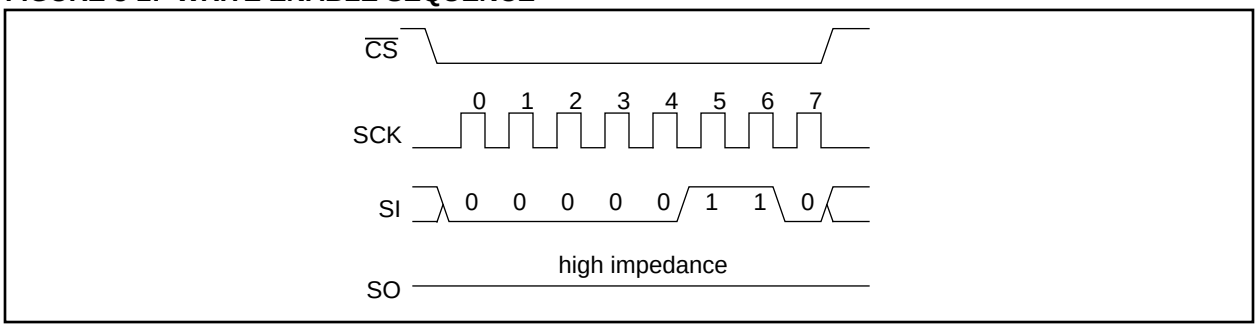


FIGURE 3-3: WRITE SEQUENCE

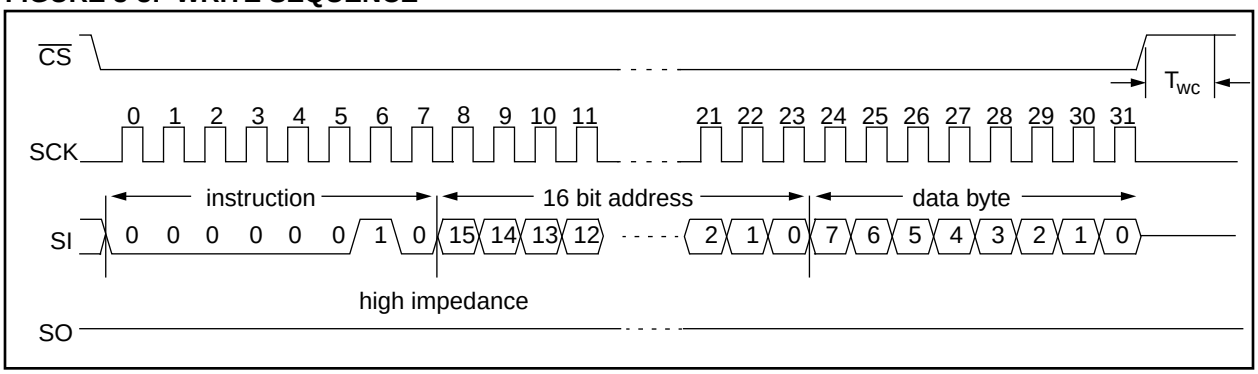


FIGURE 3-4: PAGE WRITE SEQUENCE

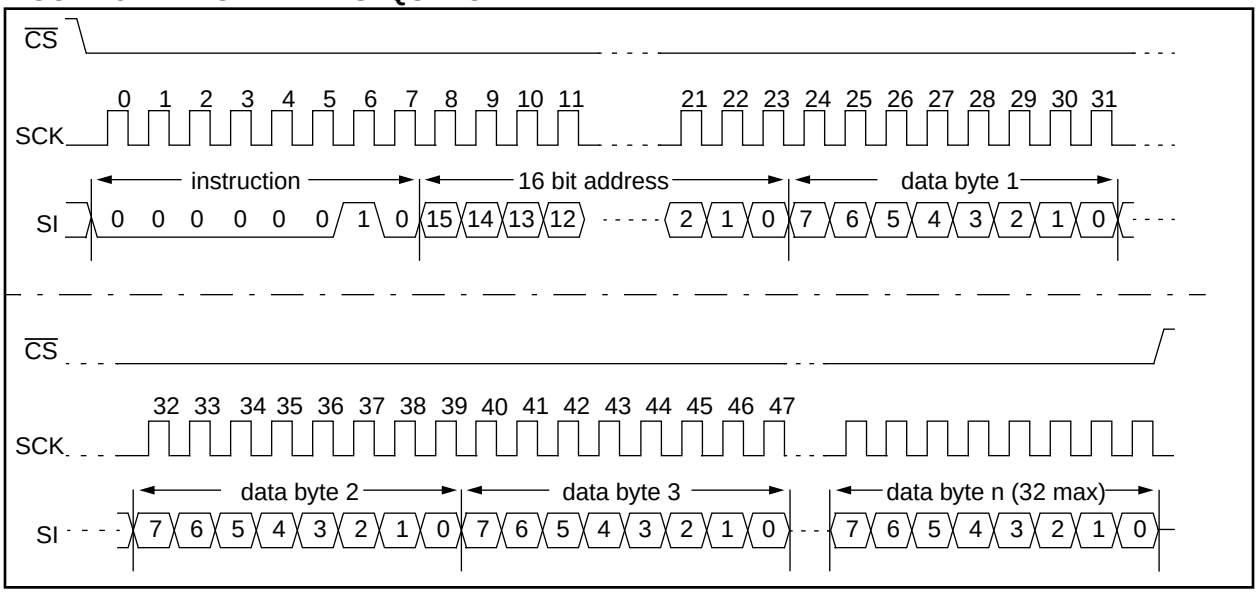


FIGURE 3-5: READ STATUS REGISTER SEQUENCE

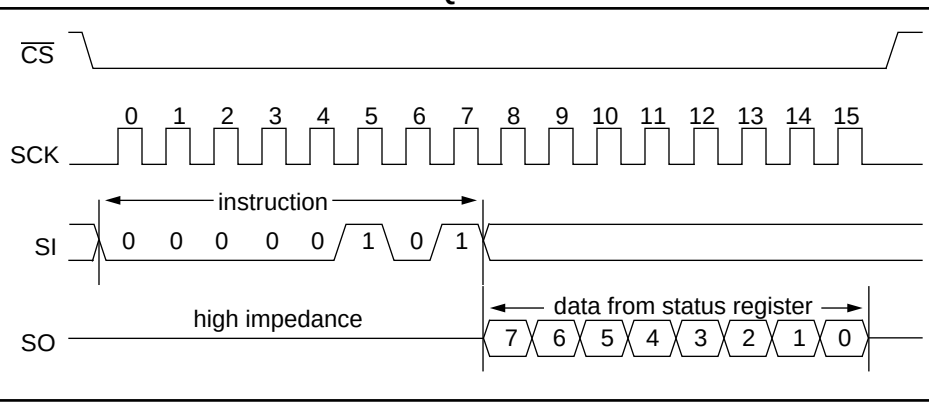
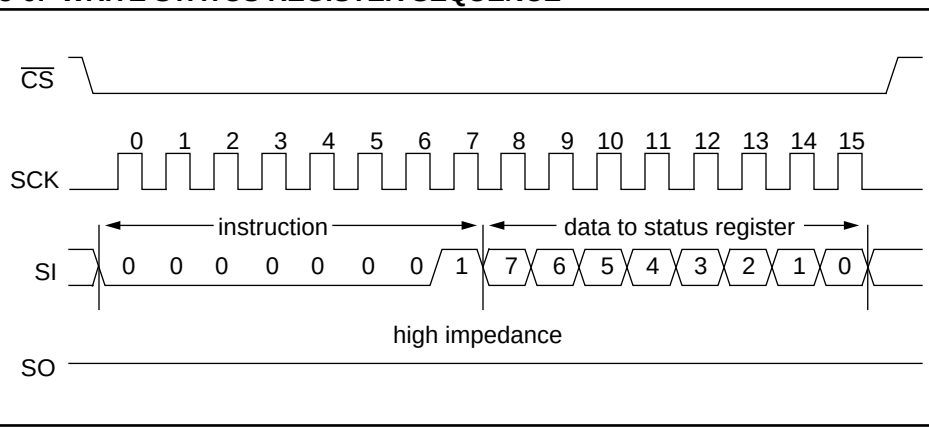


FIGURE 3-6: WRITE STATUS REGISTER SEQUENCE



4.0 PIN DESCRIPTIONS

4.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into standby mode. However, a programming cycle which is already in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into standby mode as soon as the programming cycle is complete. As soon as the device is deselected, SO goes to the high impedance state, allowing multiple parts to share the same SPI bus. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

4.2 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

It is possible for the SI pin and the SO pin to be tied together. With SI and SO tied together, two way communication of data can occur using only one microcontroller I/O line.

4.3 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA320. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

It is possible for the SI pin and the SO pin to be tied together. With SI and SO tied together, two-way communication of data can occur using only one microcontroller I/O line.

4.4 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA320. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

4.5 Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the 25AA320 in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set high.

4.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the 25AA320 while in the middle of a serial sequence without having to re-transmit the entire sequence over at a later time. It should be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the HOLD function will not be evoked until the next SCK high to low transition. The 25AA320 must remain selected during this sequence. The SI, SCK, and SO pins are in a high impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume.

25AA320 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.

25AA320 - __ /P

Package:		P =	PDIP (300 mil Body), 8-lead
		SN =	SOIC (150 mil Body), 8-lead
		ST =	TSSOP (4.4 mm Body), 14-lead
Temperature Range:		Blank =	0°C to +70°C
		I =	-40°C to +85°C
Device:	25AA320		32K SPI Bus Serial EEPROM
	25AA320T		32K SPI Bus Serial EEPROM (Tape and Reel)

Sales and Support

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office (see next page)
2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
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