Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro Cortex™-M0
NUC130 Product Data Sheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NUC130 series are 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications support CAN bus network. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent traditional 8-bit microcontroller.

The NUC130 series embeds Cortex™-M0 core running up to 50 MHz with 64K/128K-byte embedded flash and 8K/16K-byte embedded SRAM. It also equips with plenty of peripheral devices, such as Timers, Watchdog Timer, RTC, PDMA, UART, SPI/SSP, I^2C, I^2S, PWM Timer, GPIO, LIN, CAN, 12-bit ADC, Analog Comparator, Low Voltage Detector and Brown-out detector.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 50 MHz.
  - One 24-bit system timer.
  - Supports low power sleep-mode.
  - Single-cycle 32-bit hardware multiplier.
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints.
- Wide operating voltage ranges from 2.5V to 5.5V
- Flash EPROM Memory
  - 64K/128K bytes Flash EPROM for program code.
  - 4KB flash for ISP loader
  - Support In-system program(ISP) and In-application program(IAP) application code update
  - 512 byte page erase for flash
  - Configurable data flash address and size for 128KB system, fixed 4KB data flash for 64KB system.
  - Support 2 wire ICP update from ICE interface
  - Support fast parallel programming mode by external programmer.
- SRAM Memory
  - 8K/16k bytes embedded SRAM.
  - Support PDMA mode
- PDMA (Peripheral DMA)
  - Support 9 channels PDMA for automatic data transfer between SRAM and peripherals.
- Clock Control
  - Flexible selection for different applications.
  - Build-in 22 MHz OSC (Trimmed to 1%) for system operation, and low power 10 kHz OSC for watchdog and wakeup sleep operation.
  - Support one PLL, up to 50 MHz, for high performance system operation.
  - External 4~24MHz crystal input for precise timing operation.
  - External 32 kHz crystal input for RTC function and low power system operation.
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable.
  - I/O pin can be configured as interrupt source with edge/level setting.
  - High driver and high sink IO mode support.

- Timers
  - 4 sets of 24-bit timer with 8-bit prescaler.
  - Counter auto reload.
- Watch Dog Timer
  - Default ON/OFF by configuration setting
  - Multiple clock sources
  - 8 selectable time out period from 6ms ~ 3.0sec (depends on clock source)
  - WDT can wake up power down/sleep.
  - Interrupt or reset selectable on watchdog time-out.
- RTC
  - Support software compensation by setting frequency compensate register (FCR)
  - Support RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Support Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Support time tick interrupt
  - Support wake up function.
- PWM/Capture
  - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs.
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM.
  - PWM interrupt synchronous to PWM period.
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs.
  - Support Capture interrupt
- UART
  - Three compatible 16550 UART devices.
  - UART ports with flow control (TX, RX, CTS and RTS)
  - UART0 with 64-byte FIFO is for high speed
  - UART1/2 with 16-byte FIFO for standard device
  - Support IrDA (SIR) and LIN function
  - Programmable baud-rate generator up to 1/16 system clock
  - Support PDMA mode
- SPI
  - Up to four sets of SPI device.
  - Master up to 16 Mbps / Slave up to 10 Mbps.
  - Support MICROWIRE/SPI master/slave mode (SSP)
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - 2 slave/device select lines when it is as the master, and 1 slave/device select line when it is as the slave
  - Byte Sleeping mode in 32-bit transmission
  - Support PDMA mode

- I^2C
  - Two sets of I^2C device.
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master).
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate vian one serial bus.
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
  - Programmable clocks allow versatile rate control.
  - I2C-bus controllers support multiple address recognition (two slave address with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operate as either master or slave mode
  - Capable of handling 8, 16, and 32 bit word sizes
  - Mono and stereo audio data supported
  - I^2S and MSB justified data format supported
  - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Support two DMA requests, one for transmit and one for receive
- CAN 2.0
  - CAN 2.0B protocol compatible device
  - Support 11-bit identifier as well as 29-bit identifier
  - Bit rates up to 1Mbits/s
  - NRZ bit Coding/ Encoding
  - Error Detection & Status Report
    - Bit error, Form error, Stuffing error, 15-bit CRC detection, and Acknowledge error Interrupt
    - Each CAN-bus error and Transmission/Receive Done.
  - Bit Timing Synchronization
  - Acceptance filter extension
  - Sleep mode wake up
- ADC
  - 12-bit SAR ADC with 800ksps
  - Up to 8-ch single-end mode or 4-ch differential mode
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Scan on enabled channels
  - Threshold voltage detection
  - Conversion start by S/W, external pins
  - Support PDMA Mode
- Analog Comparator
  - Two analog comparator modules
  - External input or internal bandgap voltage selectable at negative node
  - Interrupt when compare result change
  - Power down wake up

- One built-in temperature sensor with 1℃ resolution.
- Brown-out detector
  - With 4 levels: 4.5V/3.8V/2.7V/2.2V
  - Support Brownout Interrupt and Reset option
- One built-in LDO
- Low Voltage Reset
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
    - LQFP 100-pin / 64-pin / 48-pin

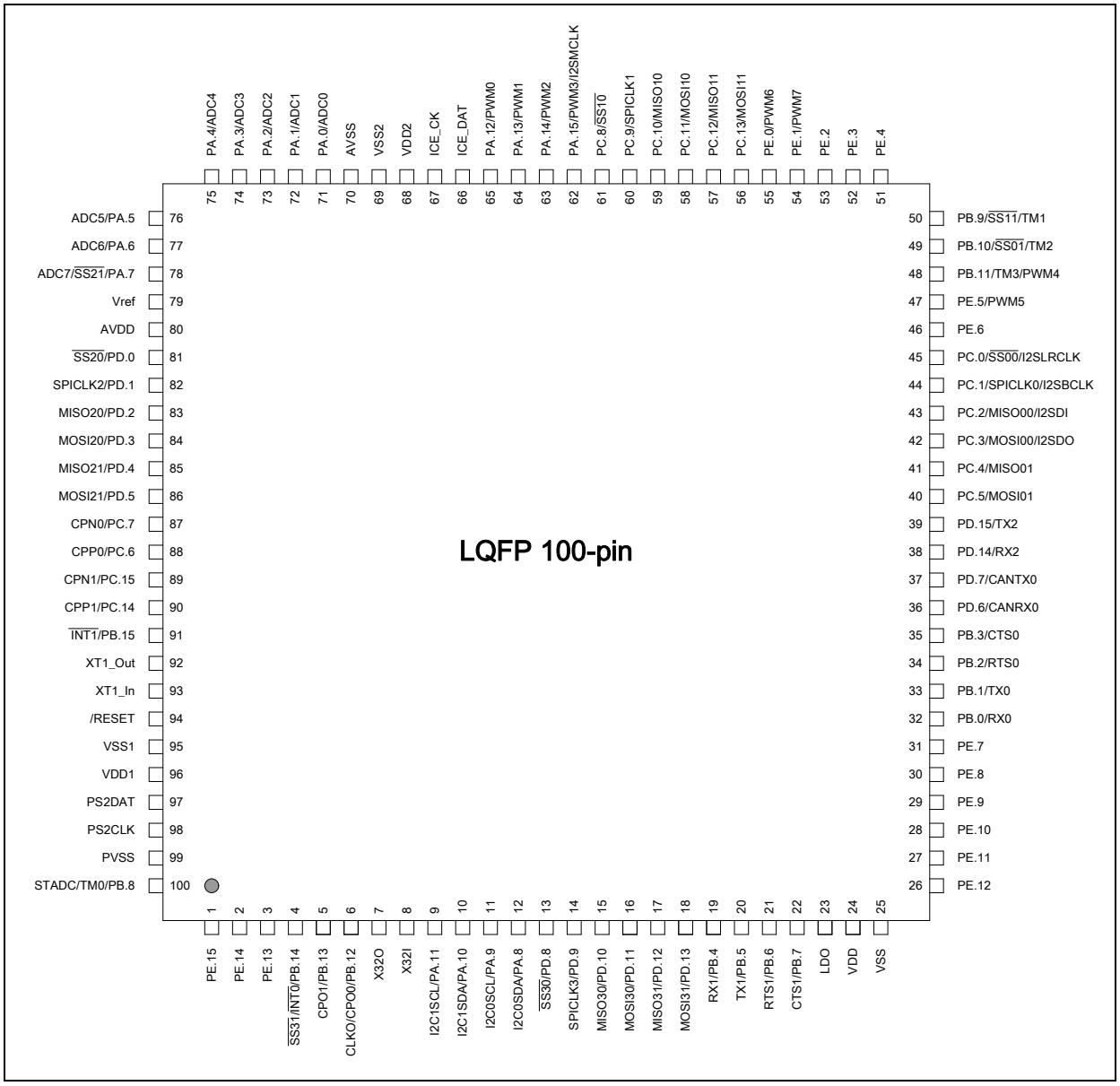
3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NUC130 Products Selection Guide

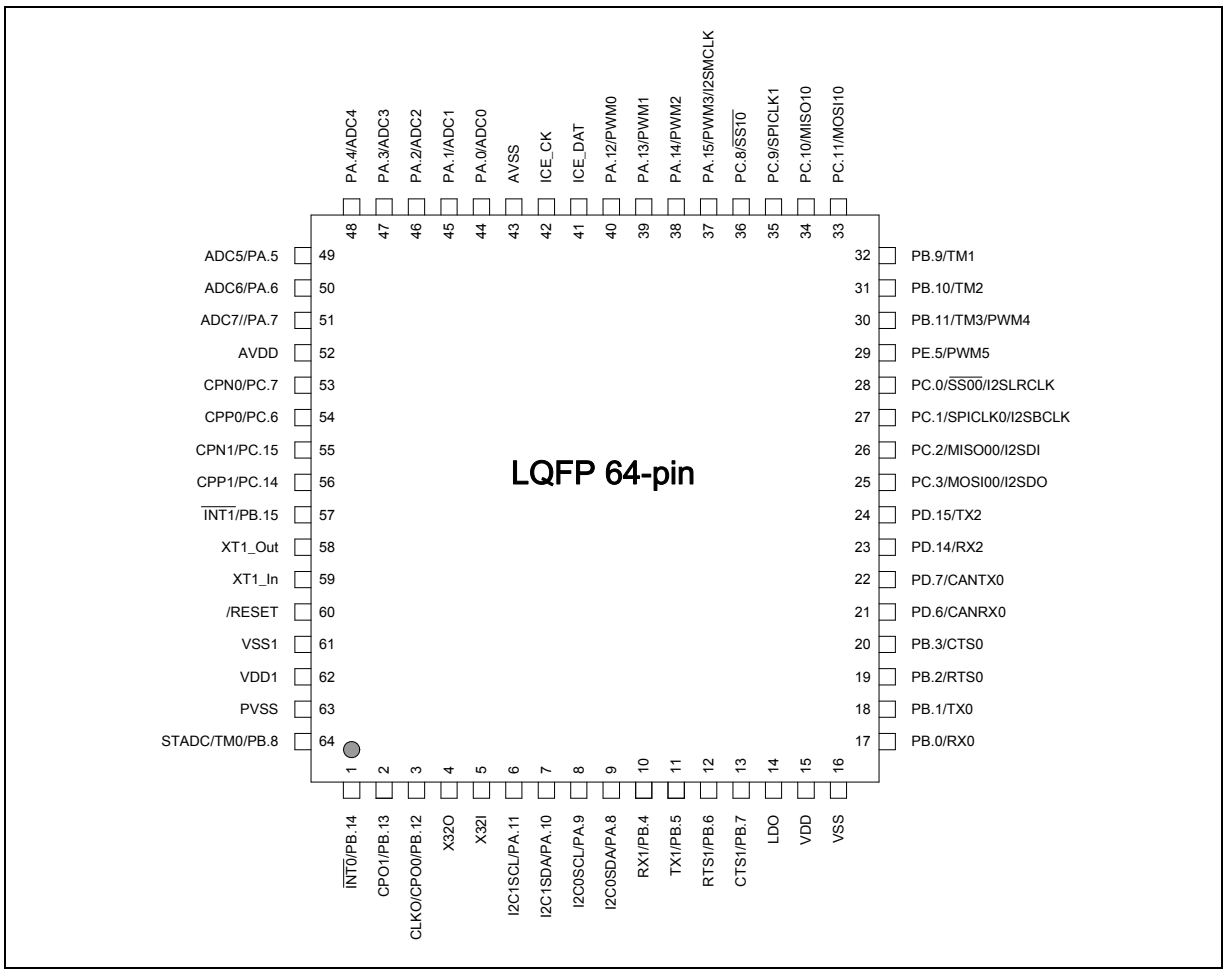
Part number	Flash	SRAM	Connectivity					I^2S	PWM	Comp.	ADC	Timer	RTC	ISP ICP	I/O	Package
			UART	SPI/SSI	I^2C	LIN	CAN									
NUC130LE3AN	128 KB	16 KB	3	1	2	2	1	1	4	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC130LD3AN	64 KB	16 KB	3	1	2	2	1	1	4	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC130LD2AN	64 KB	8 KB	3	1	2	2	1	1	4	1	8x12-bit	4x24-bit	v	v	up to 35	LQFP48
NUC130RE3AN	128 KB	16 KB	3	2	2	2	1	1	6	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC130RD3AN	64 KB	16 KB	3	2	2	2	1	1	6	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC130RD2AN	64 KB	8 KB	3	2	2	2	1	1	6	2	8x12-bit	4x24-bit	v	v	up to 49	LQFP64
NUC130VE3AN	128 KB	16 KB	3	4	2	2	1	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100
NUC130VD3AN	64 KB	16 KB	3	4	2	2	1	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100
NUC130VD2AN	64 KB	8 KB	3	4	2	2	1	1	8	2	8x12-bit	4x24-bit	v	v	up to 80	LQFP100

3.2 Pin Configuration

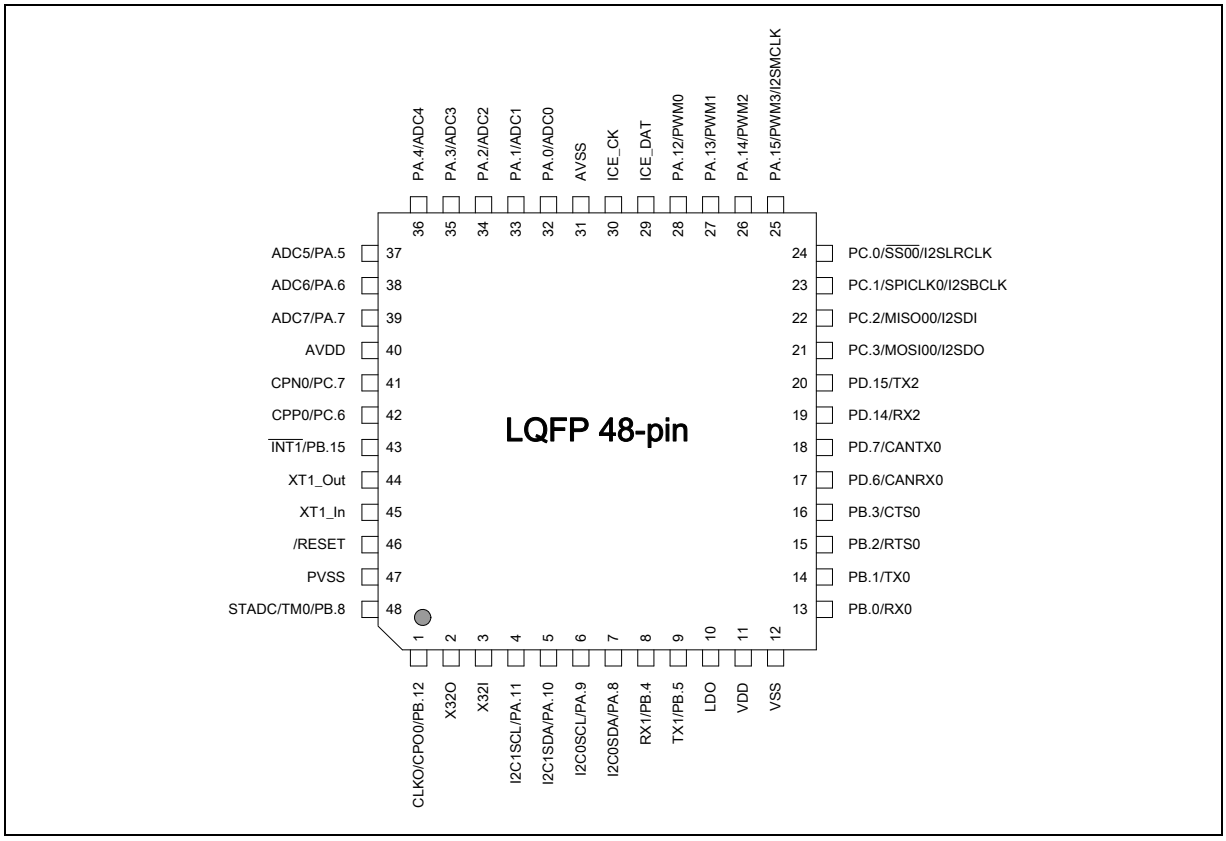
3.2.1 NUC130 LQFP 100 pin



3.2.2 NUC130 LQFP 64 pin



3.2.3 NUC130 LQFP 48 pin



3.3 Pin Description

3.3.1 NUC130 Pin Description

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
1			PE.15	**I/O**		General purpose input/output digital pin
2			PE.14	**I/O**		General purpose input/output digital pin
3			PE.13	**I/O**		General purpose input/output digital pin
4	1		PB.14	**I/O**		General purpose input/output digital pin
			/INT0	**I**		/INT0: External interrupt1 input pin
			/SPISS31	**I/O**		/SPISS31: SPI3 2nd slave select pin
5	2		PB.13	**I/O**		General purpose input/output digital pin
			CPO1	**O**		Comparator1 output pin
6	3	1	PB.12	**I/O**		General purpose input/output digital pin
			CPO0	**O**		Comparator0 output pin
			CLKO	**O**		Frequency Divider output pin
7	4	2	X32O	**I**		32.768 kHz crystal output pin
8	5	3	X32I	**O**		32.768 kHz crystal input pin
9	6	4	PA.11	**I/O**		General purpose input/output digital pin
			I2C1SCL	**I/O**		I2C1SCL: I2C1 clock pin
10	7	5	PA.10	**I/O**		General purpose input/output digital pin
			I2C1SDA	**I/O**		I2C1SDA: I2C1 data input/output pin
11	8	6	PA.9	**I/O**		General purpose input/output digital pin
			I2C0SCL	**I/O**		I2C0SCL: I2C0 clock pin
12	9	7	PA.8	**I/O**		General purpose input/output digital pin
			I2C0SDA	**I/O**		I2C0SDA: I2C0 data input/output pin
13			PD.8	**I/O**		General purpose input/output digital pin
			/SPISS30	**I/O**		/SPISS30: SPI3 slave select pin
14			PD.9	**I/O**		General purpose input/output digital pin
			SPICLK3	**I/O**		SPICLK3: SPI3 serial clock pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
15			PD.10	**I/O**		General purpose input/output digital pin
			MISO30	**I**		MISO30: SPI3 MISO (Master In, Slave Out) pin
16			PD.11	**I/O**		General purpose input/output digital pin
			MOSI30	**O**		MOSI30: SPI3 MOSI (Master Out, Slave In) pin
17			PD.12	**I/O**		General purpose input/output digital pin
			MISO31	**I**		MISO31: SPI3 2nd MISO (Master In, Slave Out) pin
18			PD.13	**I/O**		General purpose input/output digital pin
			MOSI31	**O**		MOSI31: SPI3 2nd MOSI (Master Out, Slave In) pin
19	10	8	PB.4	**I/O**		General purpose input/output digital pin
			RX1	**I**		RX1: Data Receiver input pin for UART1
20	11	9	PB.5	**I/O**		General purpose input/output digital pin
			TX1	**O**		TX1: Data transmitter output pin for UART1
21	12		PB.6	**I/O**		General purpose input/output digital pin
			RTS1			RTS1: Request to Send output pin for UART1
22	13		PB.7	**I/O**		General purpose input/output digital pin
			CTS1			CTS1: Clear to Send input pin for UART1
23	14	10	LDO	**P**		LDO output pin
24	15	11	VDD	**P**		Power supply for I/O ports and LDO source for internal PLL and digital function
25	16	12	VSS	**P**		Ground
26			PE.12	**I/O**		General purpose input/output digital pin
27			PE.11	**I/O**		General purpose input/output digital pin
28			PE.10	**I/O**		General purpose input/output digital pin
29			PE.9	**I/O**		General purpose input/output digital pin
30			PE.8	**I/O**		General purpose input/output digital pin
31			PE.7	**I/O**		General purpose input/output digital pin
32	17	13	PB.0	**I/O**		General purpose input/output digital pin
			RX0	**I**		RX0: Data Receiver input pin for UART0

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
33	18	14	PB.1	I/O		General purpose input/output digital pin
			TX0	O		TX0: Data transmitter output pin for UART0
34	19	15	PB.2	I/O		General purpose input/output digital pin
			RTS0			RTS0: Request to Send output pin for UART0
35	20	16	PB.3	I/O		General purpose input/output digital pin
			CTS0			CTS0: Clear to Send input pin for UART0
36	21	17	PD.6	I/O		General purpose input/output digital pin
			CANRX0	I		CAN Bus0 RX Input
37	22	18	PD.7	I/O		General purpose input/output digital pin
			CANTX0	O		CAN Bus0 TX Output
38	23	19	PD.14	I/O		General purpose input/output digital pin
			CANRX1	I		CAN Bus1 RX Input
39	24	20	PD.15	I/O		General purpose input/output digital pin
			CANTX1	O		CAN Bus1 TX Output
40			PC.5	I/O		General purpose input/output digital pin
			MOSI01	O		MOSI01: SPI0 2nd MOSI (Master Out, Slave In) pin
41			PC.4	I/O		General purpose input/output digital pin
			MISO01	I		MISO01: SPI0 2nd MISO (Master In, Slave Out) pin
42	25	21	PC.3	I/O		General purpose input/output digital pin
			MOSI00	O		MOSI00: SPI0 MOSI (Master Out, Slave In) pin
			I2SDO	O		I2SDO: I2S data output
43	26	22	PC.2	I/O		General purpose input/output digital pin
			MISO00	I		MISO00: SPI0 MISO (Master In, Slave Out) pin
			I2SDI	I		I2SDI: I2S data input
44	27	23	PC.1	I/O		General purpose input/output digital pin
			SPICLK0	I/O		SPICLK0: SPI0 serial clock pin
			I2SBCLK	I/O		I2SBCLK: I2S bit clock pin
45	28	24	PC.0	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			/SPISS00	I/O		/SPISS00: SPI0 slave select pin
			I2SLRCLK	I/O		I2SLRCLK: I2S left right channel clock
46			PE.6	I/O		General purpose input/output digital pin
47	29		PE.5	I/O		General purpose input/output digital pin
			PWM5	O		PWM5: PWM output
48	30		PB.11	I/O		General purpose input/output digital pin
			TM3	O		TM3: Timer3 external counter input
			PWM4	O		PWM4: PWM output
49	31		PB.10	I/O		General purpose input/output digital pin
			TM2	O		TM2: Timer2 external counter input
			/SPISS01	I/O		/SPISS01: SPI0 2nd slave select pin
50	32		PB.9	I/O		General purpose input/output digital pin
			TM1	O		TM1: Timer1 external counter input
			/SPISS11	I/O		/SPISS11: SPI1 2nd slave select pin
51			PE.4	I/O		General purpose input/output digital pin
52			PE.3	I/O		General purpose input/output digital pin
53			PE.2	I/O		General purpose input/output digital pin
54			PE.1	I/O		General purpose input/output digital pin
			PWM7	O		PWM7: PWM output
55			PE.0	I/O		General purpose input/output digital pin
			PWM6	O		PWM6: PWM output
56			PC.13	I/O		General purpose input/output digital pin
			MOSI11	O		MOSI11: SPI1 2nd MOSI (Master Out, Slave In) pin
57			PC.12	I/O		General purpose input/output digital pin
			MISO11	I		MISO11: SPI1 2nd MISO (Master In, Slave Out) pin
58	33		PC.11	I/O		General purpose input/output digital pin
			MOSI10	O		MOSI10: SPI1 MOSI (Master Out, Slave In) pin
59	34		PC.10	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			MISO10	I		MISO10: SPI1 MISO (Master In, Slave Out) pin
60	35		PC.9	I/O		General purpose input/output digital pin
			SPICLK1	I/O		SPICLK1: SPI1 serial clock pin
61	36		PC.8	I/O		General purpose input/output digital pin
			/SPISS10	I/O		/SPISS10: SPI1 slave select pin
62	37	25	PA.15	I/O		General purpose input/output digital pin
			PWM3	O		PWM3: PWM output pin
			I2SMCLK	O		I2SMCLK: I2S master clock output pin
63	38	26	PA.14	I/O		General purpose input/output digital pin
			PWM2	O		PWM2: PWM output
64	39	27	PA.13	I/O		General purpose input/output digital pin
			PWM1	O		PWM1: PWM output
65	40	28	PA.12	I/O		General purpose input/output digital pin
			PWM0	O		PWM0: PWM output
66	41	29	ICE_DAT	I/O		Serial Wired Debugger Data pin
67	42	30	ICE_CLK	I		Serial Wired Debugger Clock pin
68			VDD2	P		Power supply for I/O ports and LDO source for internal PLL and digital circuit
69		31	VSS2	P		Ground
70	43		AVSS	AP		Ground Pin for analog circuit
71	44	32	PA.0	I/O		General purpose input/output digital pin
			ADC0	AI		ADC0: ADC analog input
72	45	33	PA.1	I/O		General purpose input/output digital pin
			ADC1	AI		ADC1: ADC analog input
73	46	34	PA.2	I/O		General purpose input/output digital pin
			ADC2	AI		ADC2: ADC analog input
74	47	35	PA.3	I/O		General purpose input/output digital pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
			ADC3	**AI**		ADC3: ADC analog input
75	48	36	PA.4	**I/O**		General purpose input/output digital pin
			ADC4	**AI**		ADC4: ADC analog input
76	49	37	PA.5	**I/O**		General purpose input/output digital pin
			ADC5	**AI**		ADC5: ADC analog input
77	50	38	PA.6	**I/O**		General purpose input/output digital pin
			ADC6	**AI**		ADC6: ADC analog input
78	51	39	PA.7	**I/O**		General purpose input/output digital pin
			ADC7	**AI**		ADC7: ADC analog input
			/SPISS21	**I/O**		/SPISS21: SPI2 2nd slave select pin
79			Vref	**AP**		Voltage reference input for ADC
80	52	40	AVDD	**AP**		Power supply for internal analog circuit
81			PD.0	**I/O**		General purpose input/output digital pin
			/SPISS20	**I/O**		/SPISS20: SPI2 slave select pin
82			PD.1	**I/O**		General purpose input/output digital pin
			SPICLK2	**I/O**		SPICLK2: SPI2 serial clock pin
83			PD.2	**I/O**		General purpose input/output digital pin
			MISO20	**I**		MISO20: SPI2 MISO (Master In, Slave Out) pin
84			PD.3	**I/O**		General purpose input/output digital pin
			MOSI20	**O**		MOSI20: SPI2 MOSI (Master Out, Slave In) pin
85			PD.4	**I/O**		General purpose input/output digital pin
			MISO21	**I**		MISO21: SPI2 2nd MISO (Master In, Slave Out) pin
86			PD.5	**I/O**		General purpose input/output digital pin
			MOSI21	**O**		MOSI21: SPI2 2nd MOSI (Master Out, Slave In) pin
87	53	41	PC.7	**I/O**		General purpose input/output digital pin
			CPN0	**I**		CPN0: Comparator0 Negative input pin
88	54	42	PC.6	**I/O**		General purpose input/output digital pin
			CPP0	**I**		CPP0: Comparator0 Positive input pin

Pin No.			Pin Name	Pin Type		Description
LQFP 100	LQFP 64	LQFP 48				
89	55		PC.15	**I/O**		General purpose input/output digital pin
			CPN1	**I**		CPN1: Comparator1 Negative input pin
90	56		PC.14	**I/O**		General purpose input/output digital pin
			CPP1	**I**		CPP1: Comparator1 Positive input pin
91	57	43	PB.15	**I/O**		General purpose input/output digital pin
			/INT1	**I**		/INT1: External interrupt0 input pin
92	58	44	XT1_OUT	**O**		Crystal output pin
93	59	45	XT1_IN	**I**		Crystal input pin
94	60	46	/RESET	**I**		External reset input: Low active, set this pin low reset MCU to initial state. With internal pull-up.
95	61		VSS1	**P**		Ground
96	62		VDD1	**P**		Power supply for I/O ports and LDO source for internal PLL and digital circuit
97			PS2DAT	**I/O**		PS2 Data pin
98			PS2CLK	**I/O**		PS2 clock pin
99	63	47	PVSS	**I/O**		PLL Ground
100	64	48	PB.8	**I/O**		General purpose input/output digital pin
			STADC	**I**		STADC: ADC external trigger input.
			TM0	**O**		TM0: Timer0 external counter input

Note:

1. Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

4.1 NUC130 Block Diagram

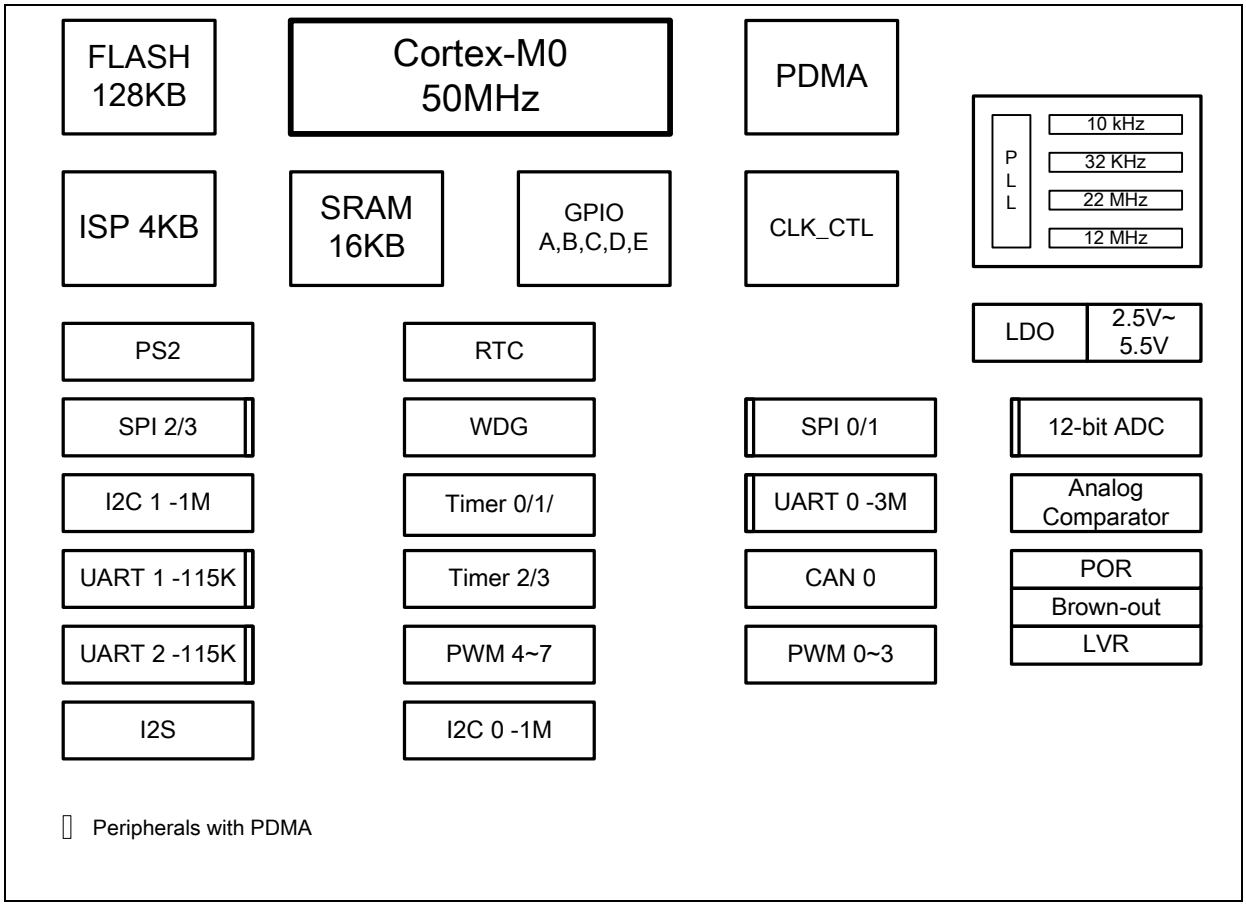


Figure 4-1 NUC130 Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex™-M0 core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor.

Figure 5-1 shows the functional blocks of processor.

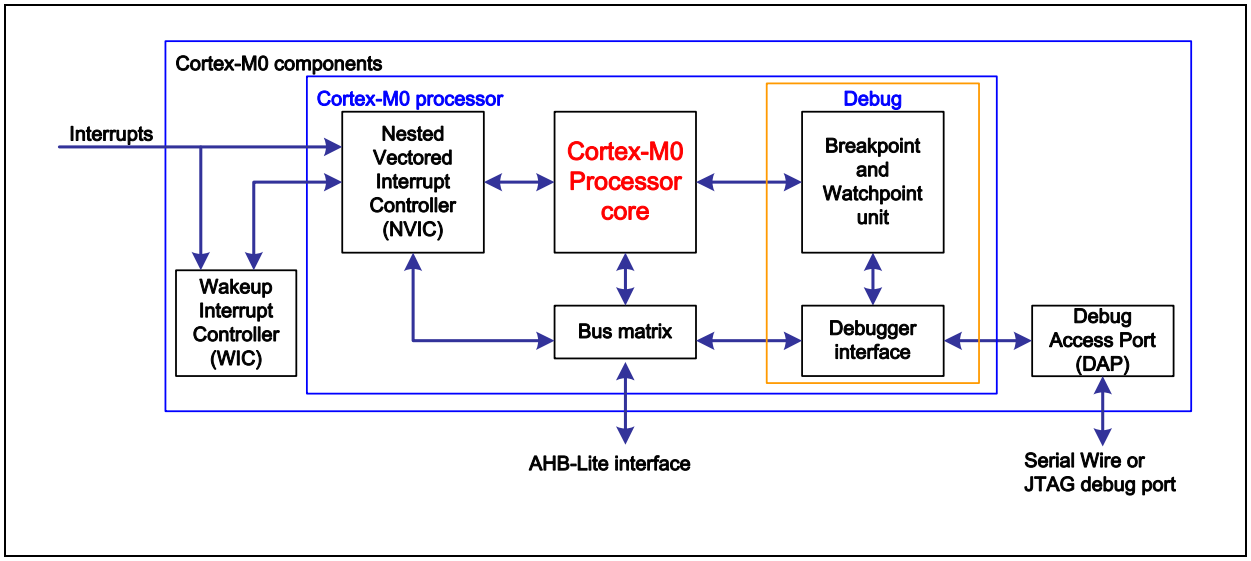


Figure 5-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor that features:
  - The ARMv6-M Thumb® instruction set.
  - Thumb-2 technology.
  - ARMv6-M compliant 24-bit SysTick timer.
  - A 32-bit hardware multiplier.
  - The system interface supports little-endian data accesses.
  - The ability to have deterministic, fixed-latency, interrupt handling.
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling.
  - C Application Binary Interface compliant exception model.
    This is the ARMv6-M, C Application Binary Interface(C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers.
  - Low power sleep-mode entry using Wait For Interrupt(WFI), Wait For Even(WFE) instructions, or the return from interrupt sleep-on-exit feature.
- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority.

- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines
- Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support.

- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

The following functions are included in system manager section

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-Out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTRC register.

- The Power-On Reset
- The low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Brown-Out-Detected Reset
- Coretex-M0 MCU Reset
- PMU Reset

5.2.3 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example 100Hz) and invokes a SysTick routine.
- A high speed alarm timer using Core clock.
- A variable rate alarm or signal timer – the duration range dependent on the reference clock used and the dynamic range of the counter.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When enabled, the timer will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

5.2.4 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.4.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NUC1xx serials. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Table 5-1 Exception Model

Exception Name	Vector Number	Priority
Reset	*1*	-3
NMI	*2*	-2
Hard Fault	*3*	-1
Reserved	*4 ~ 10*	**Reserved**
SVCall	*11*	Configurable
Reserved	*12 ~ 13*	**Reserved**
PendSV	*14*	Configurable
SysTick	*15*	Configurable
Interrupt (IRQ0 ~ IRQ31)	*16 ~ 47*	Configurable

Table 5-2 System Interrupt Map

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	**-**	-	System exceptions
16	0	**BOD_OUT**	Brown-Out	Brownout low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watch Dog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0] / PB[13:0]
21	5	**GPCDE_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**PWMB_INT**	PWM4~7	PWM4, PWM5, PWM6 and PWM7 interrupt
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt

25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt
30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**SPI2_INT**	SPI2	SPI2 interrupt
33	17	**SPI3_INT**	SPI3	SPI3 interrupt
34	18	**I2C0_INT**	I2C0	I2C0 interrupt
35	19	**I2C1_INT**	I2C1	I2C1 interrupt
36	20	**CAN0_INT**	CAN0	CAN0 interrupt
37	21	Reserved	Reserved	Reserved
38	22	Reserved	Reserved	Reserved
39	23	Reserved	Reserved	Reserved
40	24	**PS2_INT**	PS2	PS2 interrupt
41	25	**ACMP_INT**	ACMP	Analog Comparator-0 or Comaprator-1 interrupt
42	26	**PDMA_INT**	PDMA	PDMA interrupt
43	27	**I2S_INT**	I2S	I2S interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake up from power-down state
45	29	**ADC_INT**	ADC0/1	ADC interrupt
46	30	Reserved	Reserved	Reserved
47	31	**RTC_INT**	RTC	Real time clock interrupt

5.3 Clock Controller

The clock controller generates the clock sources for the whole chip, including all AMBA interface modules and all peripheral clocks. The clock controller also implements the power control function with the individually clock on or off control, clock source selection and a 4-bit clock divider next to clock source selection. The chip will into power-down mode after set the Power-Down bit and then the CPU Cortex-M0 execute the WFI or the WFE instruction. On the power down mode, the controller turns off the external crystal and internal oscillator to reduce the power consumption to minimum.

5.3.1 Clock Generator

The clock generator consists of 5 sources which list below:

- One external 32kHz crystal
- One external 12 MHz crystal
- One programmable PLL FOUT(PLL source consists of 12M and 22M)
- One internal 22 MHz oscillator
- One internal 10 kHz oscillator

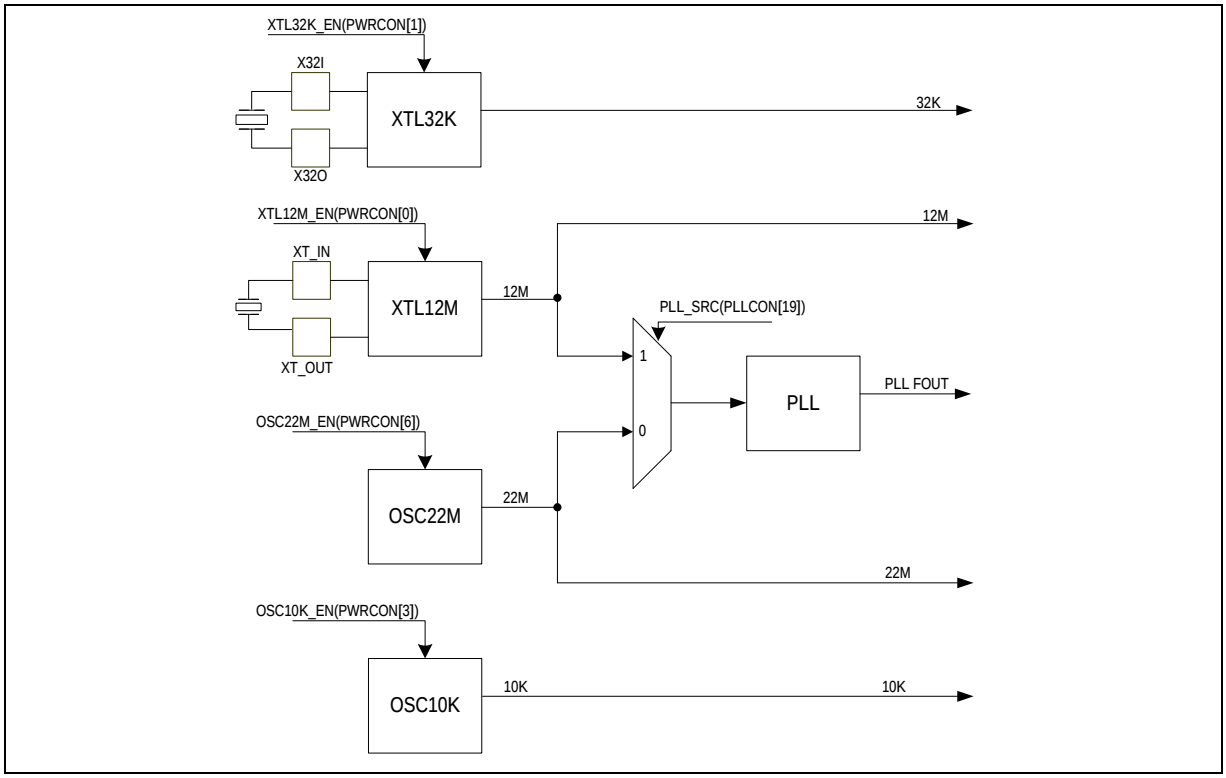


Figure 5-2 Clock generator block diagram

5.3.2 System Clock & SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S(CLKSEL0[2:0]). The block diagram lists below.

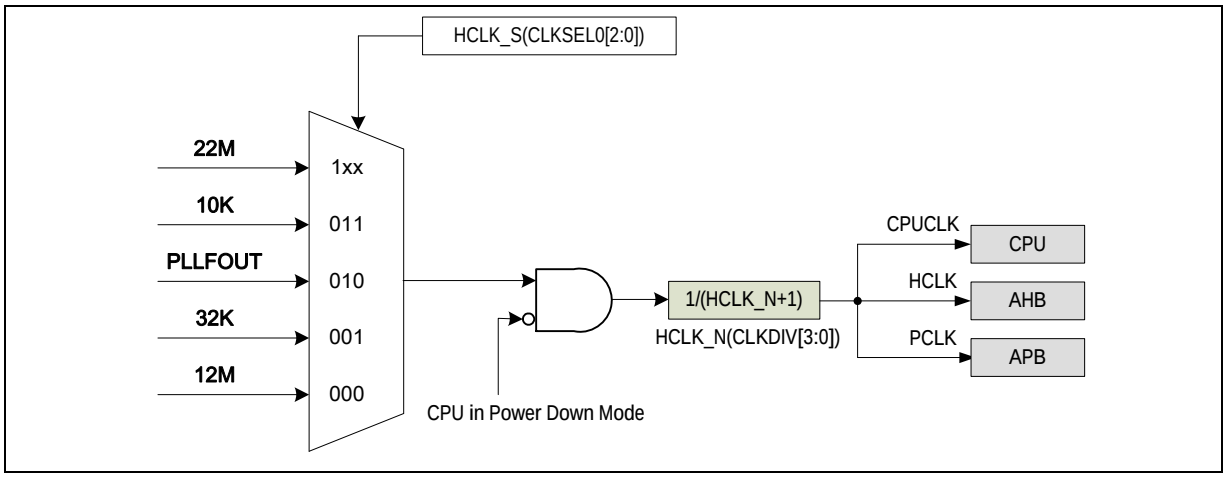


Figure 5-3 System Clock Block Diagram

The SysTick clock(STCLK) has 5 clock sources which were generated from clock generator block. The clock source switch depends on the setting of the register STCLK_S(CLKSEL0[5:3]. The block diagram lists below.

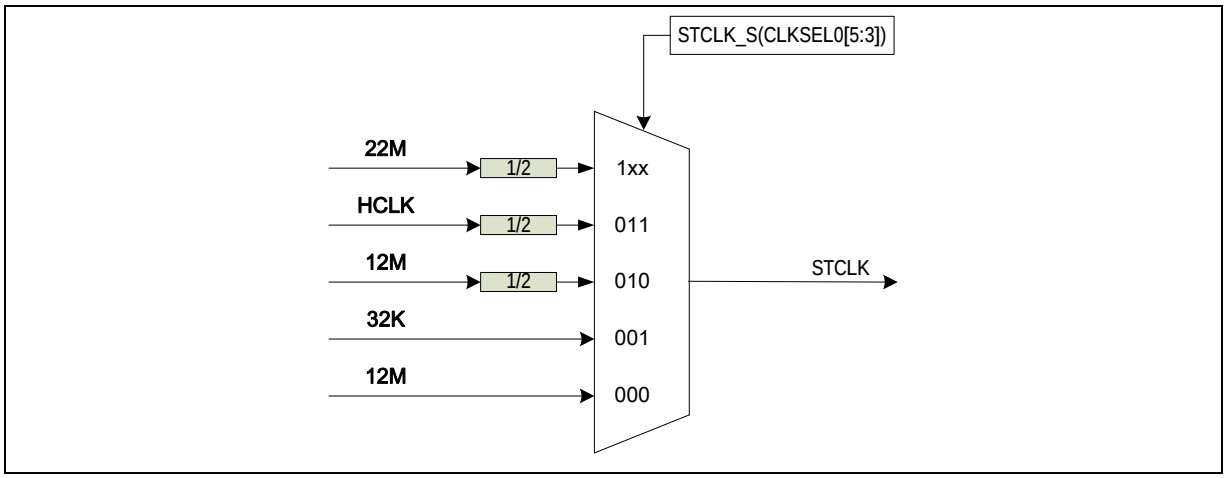


Figure 5-4 SysTick clock Control Block Diagram

5.3.3 Peripherals Clock

The peripherals clock had different clock source switch setting which depends on the different peripheral. Please refer the CLKSEL1 & APBCLK register description.

5.3.4 Power down mode (Deep Sleep Mode) Clock

When enter into power down mode, some clock sources and peripherals clock and system clock will be disable. Some clock sources and peripherals clock are still active in power down mode.

For theses clocks which still keep active list below:

- Clock Generator
  - Internal 10K oscillator clock
  - External 32K crystal clock
- Peripherals Clock (When these IP adopt 32K or 10K Hz as clock source)
  - Watch Dog Clock
  - RTC Clock
  - Timer 0/1/2/3 Clock
  - PWM Clock
  - ADC Clock

5.3.5 Frequency Divider Output

This device is equipped a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to GPIOB.12. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $F_{out} = F_{in}/2^{(N+1)}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When FREQDIV.FDIV_EN[4] is set to high, the rising transition will reset the chained counter and starts it counting. When FREQDIV.FDIV_EN[4] is written with a zero, the chained counter continuously runs till divided clock reaches low state and stay in low state.

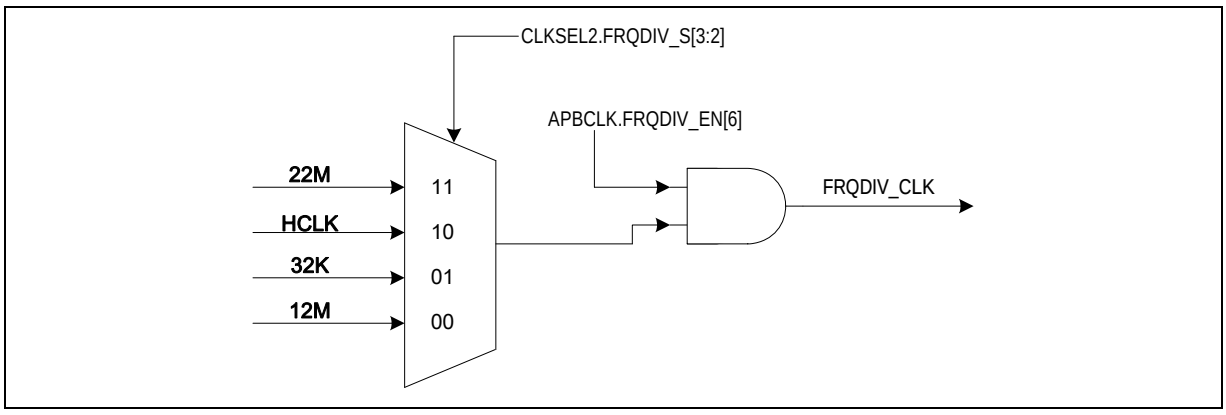


Figure 5-5 Clock Source of Frequency Divider

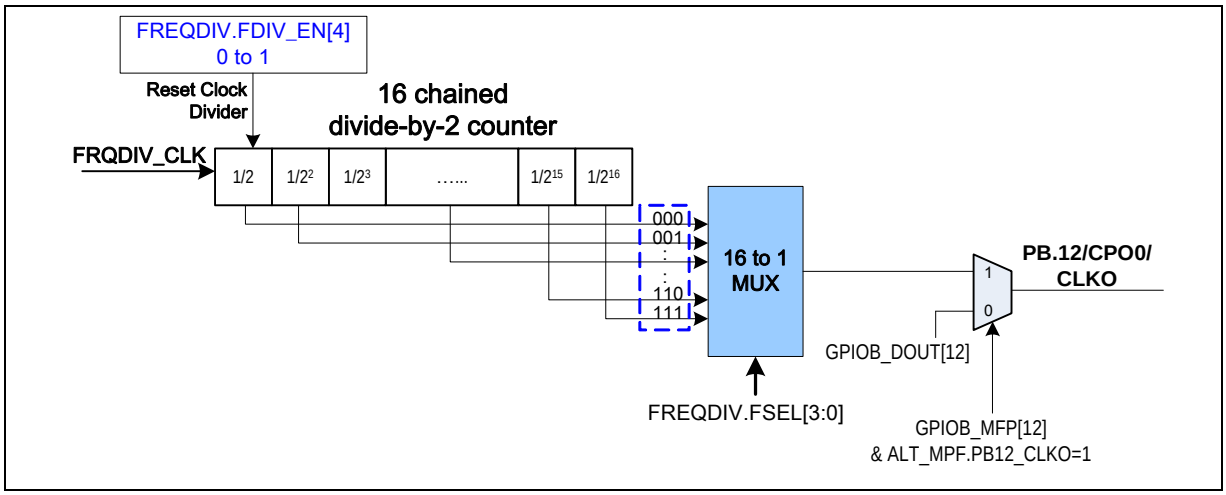


Figure 5-6 Block Diagram of Frequency Divider

5.4 General Purpose I/O

5.4.1 Overview and Features

Up to 80 General Purpose I/O pins can be shared with other function pins; it depends on the chip configuration. These 80 pins are arranged in 5 ports named with GPIOA, GPIOB, GPIOC, GPIOD and GPIOE. Each port equips maximum 16 pins. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register GPIOx_DOUT[15:0] resets to 0x000_FFFF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} is from 5.0V to 2.5V.

5.4.1.1 Input Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 00b the GPIOx port [n] pin is in Input mode and the I/O pin is in tri-state (high impedance) without output drive capability. The GPIOx_PIN value reflects the status of the corresponding port pins.

5.4.1.2 Output Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 01b the GPIOx port [n] pin is in Output mode and the I/O pin supports digital output function with source/sink current capability. The bit value in the corresponding bit [n] of GPIO_DOUT is driven on the pin.

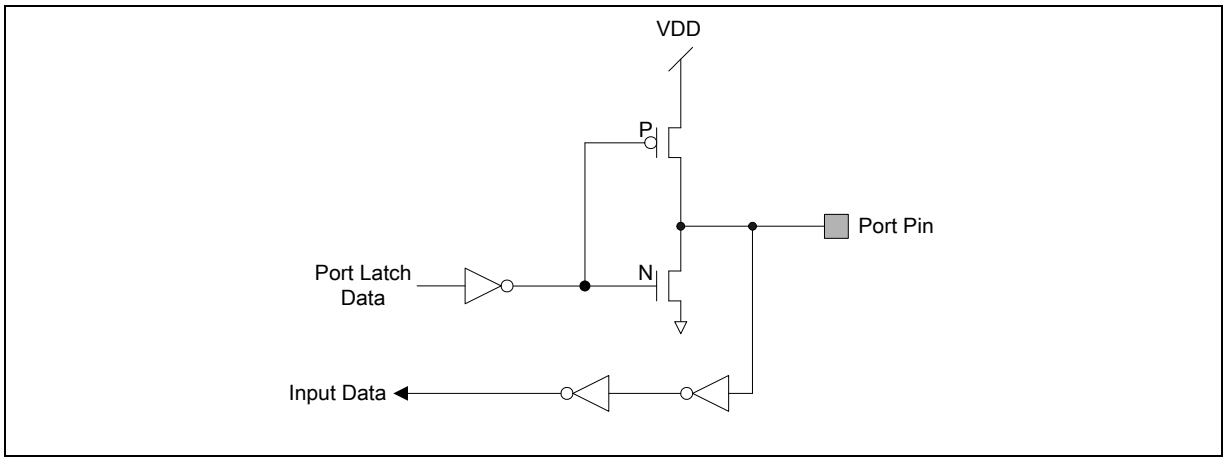


Figure 5-7 Push-Pull Output

5.4.1.3 Open-Drain Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 10b the GPIOx port [n] pin is in Open-Drain mode and the I/O pin supports digital output function but only with sink current capability, an additional pull-up resister is needed for driving high state. If the bit value in the corresponding bit [n] of GPIOx_DOUT is “0”, the pin drive a “low” output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is “1”, the pin output drives high that is controlled by the internal pull-up resistor or the external pull high resistor.

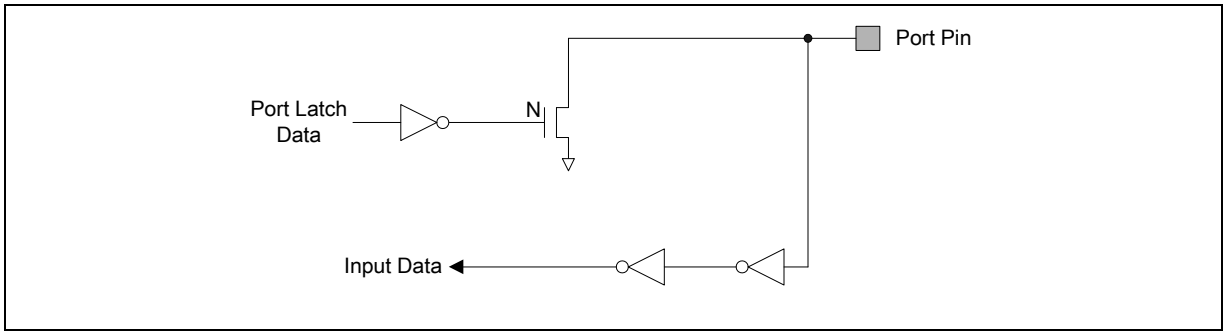


Figure 5-8 Open-Drain Output

5.4.1.4 Quasi-bidirectional Mode Explanation

Set GPIOx_PMD (PMDn[1:0]) to 11b the GPIOx port [n] pin is in Quasi-bidirectional mode and the I/O pin supports digital output and input function at the same time but the source current is only up to hundreds uA. Before the digital input function is performed the corresponding bit in GPIOx_DOUT must be set to 1. The quasi-bidirectional output is common on the 80C51 and most of its derivatives. If the bit value in the corresponding bit [n] of GPIOx_DOUT is “0”, the pin drive a “low” output on the pin. If the bit value in the corresponding bit [n] of GPIOx_DOUT is “1”, the pin will check the pin value. If pin value is high, no action takes. If pin state is low, then pin will drive strong high with 2 clock cycles on the pin and then disable the strong output drive and then the pin status is control by internal pull-up resistor. Note that the source current capability in quasi-bidirectional mode is only about 200uA to 30uA for VDD is form 5.0V to 2.5V

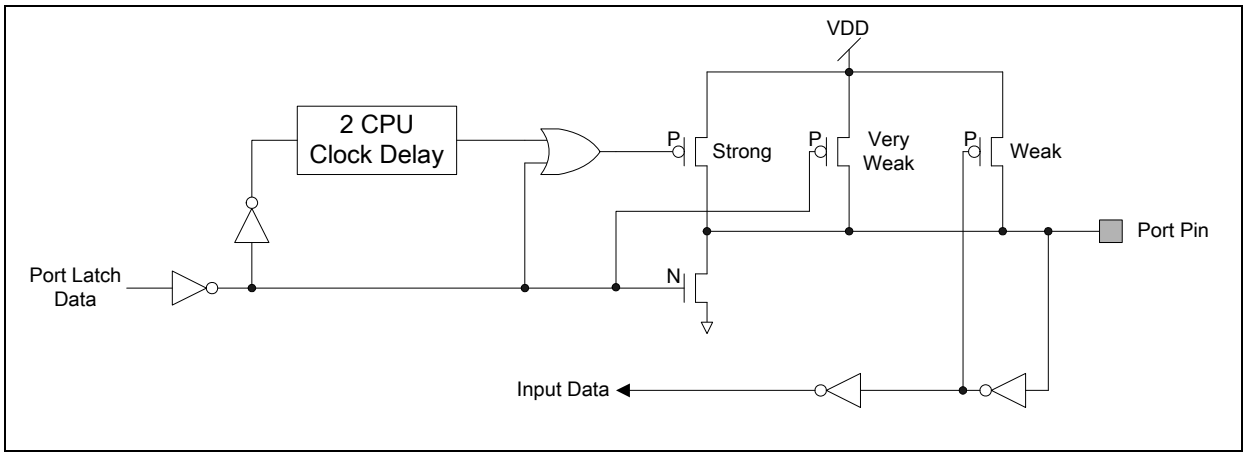


Figure 5-9 Quasi-bidirectional I/O Mode

5.5 I2C Serial Interface Controller (Master/Slave)

5.5.1 Introduction

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up to 100kbit/s in Standard-mode, up to 400kbit/s in the Fast-mode, or up to 1.0 Mbit/s in the Fast-mode Plus.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 5-10 for more detail I2C BUS Timing.

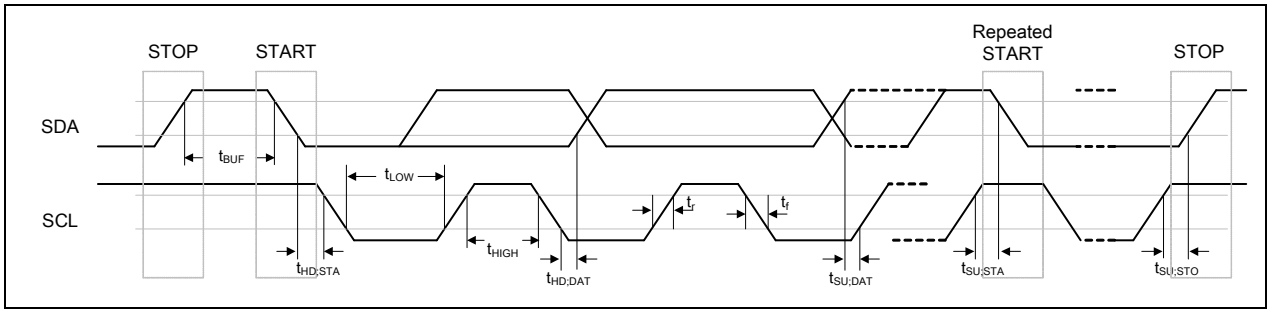


Figure 5-10 I2C Bus Timing

The device's on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The I2C H/W interfaces to the I2C bus via two pins: SDA (Px.y, serial data line) and SCL (Px.y, serial clock line). Pull up resistor is needed for Pin Px.y and Px.y for I2C operation as these are open drain pins. When the I/O pins are used as I2C port, user must set the pins to logic high in advance.

5.5.2 Features

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave up to 1Mbit/s
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate vian one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I2C interrupt if the I2C bus hangs up and timer-out counter overflows.
- External pull-up are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I2C-bus controllers support multiple address recognition (Four slave address with mask option)

5.6 PWM Generator and Capture Timer

5.6.1 Introduction

This chip has 4 sets of PWM Generators which can be configured as 8 independent PWM outputs, PWM0~PWM7, or as 4 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) with 4 programmable dead-zone generators. Each PWM Generator has one 8-bit prescaler, one clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The 4 sets of PWM Generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero. Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or continuous mode to output PWM waveform continuously.

When PCR.DZEN01 is set, PWM0 and PWM1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM0 timer and Dead-zone generator 0. Similarly, the complementary PWM pairs of (PWM2, PWM3), (PWM4, PWM5) and (PWM6, PWM7) are controlled by PWM2, PWM4 and PWM6 timers and Dead-zone generator 2, 4 and 6, respectively.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be load into the 16-bit down counter/ comparator at the time down counter reaching zero. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches zero, the interrupt request is generated. If PWM-timer is set as continuous mode, when the down counter reaches zero, it is reloaded with PWM Counter Register (CNRx) automatically then start decreasing, repeatedly. If the PWM-timer is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches zero.

The value of PWM counter comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

The alternate feature of the PWM-timer is digital input Capture function. If Capture function is enabled the PWM output pin is switched as capture input mode. The Capture0 and PWM0 share one timer which is included in PWM 0; and the Capture1 and PWM1 share PWM1 timer, and etc. Therefore user must setup the PWM-timer before enable Capture feature. After capture feature is enabled, the capture always latched PWM-counter to Capture Rising Latch Register (CRLR) when input channel has a rising transition and latched PWM-counter to Capture Falling Latch Register (CFLR) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CCR0.CRL_IE0[1] (Rising latch Interrupt enable) and CCR0.CFL_IE0[2]] (Falling latch Interrupt enable) to decide the condition of interrupt occur. Capture channel 1 has the same feature by setting CCR0.CRL_IE1[17] and CCR0.CFL_IE1[18]. And capture channel 2 to channel 7 have the same feature by setting the corresponding control bits in CCR1 to CCR3. Whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

5.6.2 Features

5.6.2.1 PWM function features:

- Four PWM Generators, each one supports one 8-bit prescaler, one clock divider, PWM-timer, one dead-zone generator and two PWM outputs.
- Up to 8 PWM channels or 4 PWM paired channels.
- Up to 16 bits resolution.
- PWM Interrupt request synchronous with PWM period.
- Single-shot or Continuous mode PWM.
- Four Dead-Zone generators

5.6.2.2 Capture Function Features:

- Timing control logic shared with PWM Generators.
- 8 Capture input channels.
- Each channel support one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

5.7 Real Time Clock (RTC)

5.7.1 Overview

Real Time Clock (RTC) unit provides user the real time and calendar message. The clock source of RTC is from an external 32.768KHz crystal connected at pins X32I and X32O or from an external 32.768KHz oscillator output fed at pin X32I. The RTC unit provides the time message(second, minute, hour) in Time Loading Register (TLR) as well as calendar message(day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. This unit offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC unit supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR(TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). The RTC Time Tick and Alarm Match can cause CPU wakeup from sleep or power-down mode if Wakeup CPU function is enabled(TWKE(TTR[3])=1).

5.7.2 RTC Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time.
- Alarm register (second, minute, hour, day, month, year).
- 12-hour or 24-hour mode is selectable.
- Leap year compensation automatically.
- Day of week counter.
- Frequency compensate register (FCR).
- All time and calendar message is expressed in BCD code.
- Support periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Support RTC Time Tick and Alarm Match interrupt
- Support wake up CPU from sleep or power-down mode.

5.8 Serial Peripheral Interface (SPI) Controller

5.8.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. NUC1XX series contain up to four sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it also can be set as a slave controlled by an off-chip master device.

5.8.2 Features

- Four sets of SPI controller
- Support master or slave operation
- Support 1 and 2-bit serial data IN/OUT
- Configurable data length of transfer word up to 32 bits
- Variable output serial clock frequency in master mode
- Provide burst mode operation, transmit/receive can be executed up to two times in one transfer
- MSB or LSB first data transfer
- 2 slave/device select lines when it is set as the master mode, and 1 slave/device select line when it is set as slave mode
- Fully static synchronous design with one clock domain
- Byte Suspend Sleep Mode
- Support two programmable serial output clock frequency.

5.9 Timer Controller

5.9.1 General Timer Controller

The timer module includes four channels, TIMER0~TIMER3 (TIMER0 and TIMER1 are at APB1 and TIMER2 and TIMER3 are at APB2), which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generates an interrupt signal upon timeout, or provide the current value of count during operation.

5.9.2 Features

- Independent clock source for each channel (TMR0_CLK, TMR1_CLK, TMR2_CLK, TMR3_CLK).
- Time out period = (Period of timer clock input) * (8-bit Prescale + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / 25 MHz) * (2^8) * (2^24), if TCLK = 25 MHz.
- Internal 24-bit up counter is readable through TDR (Timer Data Register).

5.10 Watchdog Timer

The purpose of Watchdog Timer is to perform a system reset after the software running into a problem. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wakeup CPU from power-down mode. The watchdog timer includes a 19-bit free running counter with programmable time-out intervals.

Setting WTE (WDTCR[7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time follows the time-out event. User must set WTR (WDTCR[0]) (Watchdog timer reset) high to reset the 19-bit WDT counter to avoid CPU from Watchdog timer reset before the delay time expires. WTR bit is auto cleared by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WDTCR[10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset CPU. This reset will last 64 WDT clocks then CPU restarts executing program from reset vector (0x0000 0000). WTRF will not be cleared by Watchdog reset. User may poll WTFR by software to recognize the reset source.

Table 5-3 Watchdog Timeout Interval Selection

WTIS	Interrupt Timeout	Watchdog Reset Timeout	WTR Timeout Interval (WDT_CLK=12 MHz)	WTR Timeout Interval (WDT_CLK=32kHz)
000	2^4 WDT_CLK	(2^4 + 1024) WDT_CLK	69.33 us	31.7 ms
001	2^6 WDT_CLK	(2^6 + 1024) WDT_CLK	72.53 us	33.2 ms
010	2^8 WDT_CLK	(2^8 + 1024) WDT_CLK	85.33 us	39 ms
011	2^{10} WDT_CLK	(2^{10} + 1024) WDT_CLK	170.67 us	64 ms
100	2^{12} WDT_CLK	(2^{12} + 1024) WDT_CLK	426.67 us	160 ms
101	2^{14} WDT_CLK	(2^{14} + 1024) WDT_CLK	1.45 ms	544 ms
110	2^{16} WDT_CLK	(2^{16} + 1024) WDT_CLK	5.55 ms	2080 ms
111	2^{18} WDT_CLK	(2^{18} + 1024) WDT_CLK	21.93 ms	8224 ms

5.11 UART Interface Controller

This MCU provides three channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1~2 perform Normal Speed UARTs, besides, only UART0 and UART1 support flow control function.

5.11.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports LIN master mode function and IrDA SIR Function. Each UART channel supports seven types of interrupts including transmitter FIFO empty interrupt(INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (overrun error or parity error or framing error or break interrupt) (INT_RLS), time out interrupt (INT_Tout), MODEM/Wakeup status interrupt (INT_Modem), Buffer error interrupt (INT_Buf_Err) and LIN receiver break field detected interrupt.

The UART0 are built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART1~2 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, overrun error, framing error and break interrupt) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing crystal clock input by divisors to produce the clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD)**.** Table 5-4 lists the equations in the various conditions.

The UART0 and UART1 controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the Rx FIFO equals the value of RTS_Tri_Lev(UA_FCR[19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a validly asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN(UA_FUN_SEL[1])to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

The alternate function of UART controllers is LIN(Local Interconnect Network) function. The LIN mode is selected by setting the LIN_EN bit in UA_FUN_SEL register. In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

Table 5-4 UART Baud Rate Equation

DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud rate equation
Disable	0	B	A	UART_CLK / [16 * (A+2)]
Enable	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8

Enable	1	B	A	UART_CLK / (A+2), A must >=3

5.11.2 Features of UART controller

- The UART control supports three channels, UART0, UART1 and UART2.
- UART0/UART1/UART2 supports 64/16/16 bytes entry FIFO for received and transmitted data payloads.
- Auto flow control/flow control function (/CTS, /RTS) are supported in UART0 and UART1.
- Individual programmable baud-rate generator for each channel.
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit character.
  - Even, odd, or no-parity bit generation and detection.
  - 1-, 1&1/2, or 2-stop bit generation.
  - Baud rate generation.
  - False start bit detection.
- Support IrDA SIR Function.
- Support LIN master mode.

5.12 Controller Area Network (CAN Bus)

5.12.1 Introduction

The Controller Area Network (CAN) is a serial communications protocol which is multi-master and it efficiently supports distributed real-time control with very high level of security. Its domain of application range from high speed networks to low cost multiplex wiring. In automotive electronics, engine control units, sensors, anti-skid-systems, etc. are connected using CAN with bit-rates up to 1Mbit/s.

In CAN systems, a node does not make use of any information about the system configuration (station addresses). Any Nodes can be added to the CAN network without requiring any change in the software or hardware of any node. The information on the bus is sent in fixed format message of different but limited length. When the bus is free, any connected unit may start to transmit a new message. The content of message is named by IDENTIFIER. The IDENTIFIER does not indicate the destination of the message, but describes the meaning of the data, so that all nodes in the network are able to decide by Message Filtering whether the data is to be acted upon by them or not. Within a CAN network it is guaranteed that a message is simultaneously accepted either by all nodes or by no node.

5.12.2 Features

- CAN 2.0B protocol compatibility
- AMBA APB bus interface compatible
- Multi-master node
- Support 11-bit identifier as well as 29-bit identifier
- Bit rates up to 1Mbits/s
- NRZ bit coding
- Error detection: bit error, stuff error, form error, 15-bit CRC detection, and acknowledge error
- Listen only mode (no acknowledge, no active error flags)
- Acceptance filter extension (4-byte code, 4-byte mask)
- Error interrupt for each CAN-bus error
- Extended receive buffer (8-byte FIFO)
- Wakeup function

5.13 PS2 Device Controller (PS2D)

5.13.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. S/w can select 1 to 16 bytes for a continuous transmission.

5.13.2 Features

- APB interface compatible
- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

5.14 I2S Controller

5.14.1 Overview

The I2S controller consists of IIS protocol to interface with external audio CODEC. Two 8 word deep FIFO for read path and write path respectively and is capable of handling 8 ~ 32 bit word sizes. DMA controller handles the data movement between FIFO and memory.

5.14.2 Features

- APB interface compatible
- I2S can operate as either master or slave
- Capable of handling 8, 16, and 32 bit word sizes.
- Mono and stereo audio data supported.
- I2S and MSB justified data format supported.
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, one for transmit and one for receive.

5.15 Analog-to-Digital Converter (ADC)

5.15.1 Functional Description

NUC1XX series contain one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode. There are two kinds of scan mode: continuous mode and single cycle mode. The A/D converters can be started by software and external STADC/PB.8 pin.

Note that the analog input port pins must be configured as input type before ADC function is enabled.

5.15.2 Features

- Analog input voltage range: 0~Vref (Max to 5.0V).
- 12-bits resolution and 10-bits accuracy is guaranteed.
- Up to 8 single-end analog input channels or 4 differential analog input channels.
- Maximum ADC clock frequency is 16MHz.
- Up to 800kHz SPS conversion rate, conversion time is less than 1.25us.
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by
  - Software write 1 to ADST bit
  - External pin STADC
- Conversion results are held in data registers for each channel with valid and overrun indicators.
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting.
- Channel 7 supports 4 input sources: external analog voltage, internal fixed bandgap voltage, internal temperature sensor output and analog ground.
- Support Self-calibration to minimum conversion error.

5.16 Analog Comparator

5.16.1 Functional Description

NUC1XX series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes.

Note that the analog input port pins must be configured as input type before Analog Comparator function is enabled.

5.16.2 Features

- Analog input voltage range: 0~5.0V
- Software enabled with hysterisis function
- Two analog comparators with optional internal reference voltage input at negative end
- One comparator interrupt requested by either comparator

5.17 PDMA Controller

5.17.1 Overview

The NUC1XX contains a peripheral direct memory access (PDMA) controller that transfers data to and from memory or transfer data to and from APB devices. The PDMA has nine channels of DMA (Peripheral-to-Memory or Memory-to-Peripheral or Memory-to-Memory). For each PDMA channel (PDMA CH0~CH8), there is one word buffer as transfer buffer between the Peripherals APB devices and Memory.

Software can stop the PDMA operation by disable PDMA [PDMACEN]. The CPU can recognize the completion of a PDMA operation by software polling or when it receives an internal PDMA interrupt. The NUC1XX PDMA controller can increment source or destination address, fixed or wrap around them as well.

5.17.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- PDMA support 32-bit source and destination addressing range address increment, fixed and wrap around.

6 FLASH MEMORY CONTROLLER (FMC)

6.1 Overview

NUC1XX series equips with 128/64/32K bytes on chip embedded Flash EEPROM for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NUC1XX series also provide additional 4k bytes DATA Flash for user, to store some application dependent data before chip power off, in 64/32k APROM model. For 128k bytes device, the data flash is shared with original 128k program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user depends on her application request.

6.2 Features

- AHB interface compatible
- Run up to 50 MHz with zero wait state for discontinuous address read access
- 128/64/32KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Configurable or fixed 4KB data flash with 512 bytes page erase unit
- Programmable data flash start address and memory size for 128K program memory
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage (bypass = 0)	V_{LDO}	-10%	2.45	+10%	V	V_{DD} > 2.7V
LDO Output Voltage (bypass = 0)	V_{LDO}	-10%	V_{DD}	+10%	V	V_{DD} < 2.7V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Operating Current Normal Run Mode @ 50Mhz	I_{DD1}		50		mA	V_{DD}= 5.5V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{DD2}		33		mA	V_{DD}=5.5V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
	I_{DD3}		45		mA	V_{DD} = 3V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{DD4}		27		mA	V_{DD} = 3V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Normal Run Mode @ 12Mhz	I_{DD5}		22		mA	V_{DD} = 5.5V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD6}		15		mA	V_{DD} = 5.5V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
	I_{DD7}		20		mA	V_{DD} = 3V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{DD8}		12		mA	V_{DD} = 3V@12Mhz, disable all IP and disable PLL, XTAL=12MHz

Operating Current Normal Run Mode @ 4Mhz	I_{DD9}		5.8		mA	V_{DD} = 5V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD10}		4.2		mA	V_{DD} = V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
	I_{DD11}		5.1		mA	V_{DD} = 3V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{DD12}		3.6		mA	V_{DD} = 3V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
Operating Current Idle Mode @ 50Mhz	I_{IDLE1}		35		mA	V_{DD}= 5.5V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE2}		15		mA	V_{DD}=5.5V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
	I_{IDLE3}		34		mA	V_{DD} = 3V@50Mhz, enable all IP and PLL, XTAL=12MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V@50Mhz, disable all IP and enable PLL, XTAL=12MHz
Operating Current Idle Mode @ 12Mhz	I_{IDLE5}		14		mA	V_{DD} = 5.5V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE6}		5		mA	V_{DD} = 5.5V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
	I_{IDLE7}		12		mA	V_{DD} = 3V@12Mhz, enable all IP and disable PLL, XTAL=12MHz
	I_{IDLE8}		4		mA	V_{DD} = 3V@12Mhz, disable all IP and disable PLL, XTAL=12MHz
Operating Current Idle Mode @ 4Mhz	I_{IDLE9}		3.4		mA	V_{DD} = 5V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE10}		1.8		mA	V_{DD} = V@4Mhz, disable all IP and disable PLL, XTAL=4MHz
	I_{IDLE11}		2.8		mA	V_{DD} = 3V@4Mhz, enable all IP and disable PLL, XTAL=4MHz
	I_{IDLE12}		1.2		mA	V_{DD} = 3V@4Mhz, disable all IP and disable PLL, XTAL=4MHz

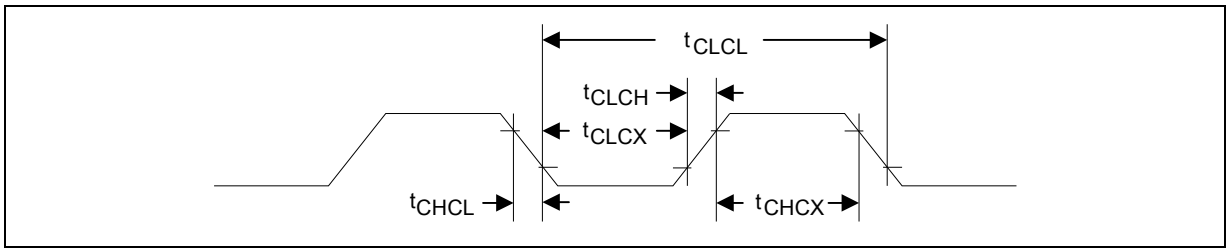
Standby Current Power-down Mode (Deep Sleep Mode)	I_{PWD1}		23		μA	V_{DD} = 5.5V, RTC OFF, No load @ Disable BOV function
	I_{PWD2}		18		μA	V_{DD} = 3.3V, RTC OFF, No load @ Disable BOV function
	I_{PWD3}		28		μA	V_{DD} = 5.5V, RTC run , No load @ Disable BOV function
	I_{PWD4}		22		μA	V_{DD} = 3.3V, RTC run , No load @ Disable BOV function
Input Current PA, PB, PC, PD, PE	I_{IN1}	-60	-	+15	μA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current at /RESET [1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidiretional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN}<2.0V
Input Low Voltage PA, PB, PC, PD, PE (TTL input)	V_{IL1}	-0.3	-	1.0	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE (TTL input)	V_{IH1}	2.2	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} =3.0V
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.8		
		0	-	0.4		
Input High Voltage X32O[*2]	V_{IH4}	3.5	-	V_{DD} +0.2		
		2.4	-	V_{DD} +0.2		
Negative going threshold (Schmitt input), /RST	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input), /RST	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Internal /RST pin pull up resistor	R_{RST}	50		100	KΩ	
Hysteresis voltage	V_{HY}		0.2V_{DD}		V	

Source Current PA, PB, PC, PD, PE (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brownout voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, 5he transition current reaches its maximum value when Vin approximates to 2V.

7.3 AC Electrical Characteristics



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	-	nS	
Clock Low Time	t_{CLCX}	20	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

7.3.1 External XTAL1 Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V

7.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

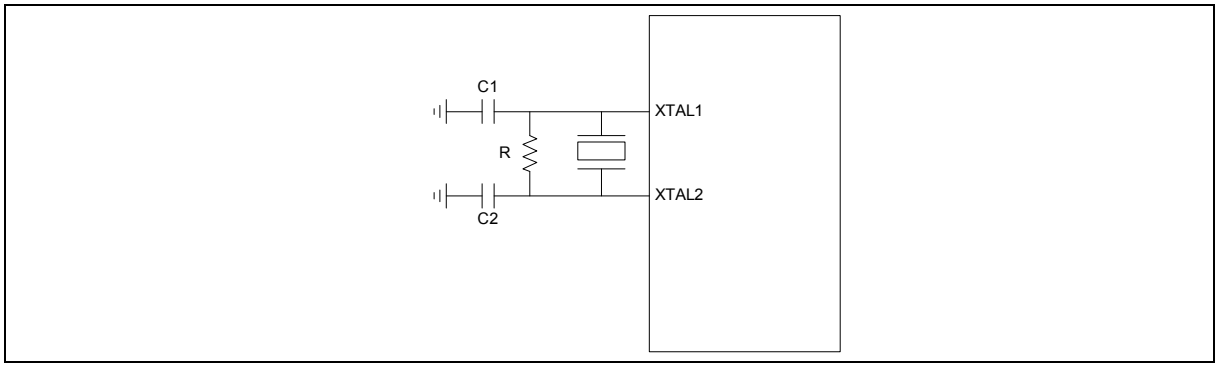


Figure 7-1 Typical Crystal Application Circuit

7.3.2 External 32kHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	-	5.5	V
Operating current	V_{DD} = 5V	-	5	-	uA

7.3.3 Internal 22.1184MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-1	-	+1	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-3	-	+3	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-40°C~+85°C; V_{DD}=2.5V~5.5V	-25	-	+25	%
Operating current	V_{DD} =5V	-	500	-	uA

7.3.4 Internal 10kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes form LDO.

7.4 Analog Characteristics

7.4.1 Specification of 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±3	-	LSB
Integral nonlinearity error	INL	-	±4	-	LSB
Offset error	EO	-	±1	10	LSB
Gain error (Transfer gain)	EG	-	1	1.005	-
Monotonic	-	Guaranteed			-
ADC clock frequency	FADC	-	-	20	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	800	Ksps
Supply voltage	V_{LDO}	-	2.5	-	V
	VADD	3	-	5.5	V
Supply current (Avg.)	IDD	-	0.5	-	mA
	IDDA	-	1.5	-	mA
Reference voltage	VREF	-	VDDA	-	V
Reference current (Avg.)	IREFP	-	1	-	mA
Input voltage range	VIN	0	-	VREF	V
Capacitance	CIN	-	5	-	pF

7.4.2 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V_{DD} input voltage
Output Voltage (bypass=0)	-10%	2.45	+10%	V	LDO output voltage
Output Voltage (bypass=1)	-10%	Input Voltage	+10%	V	Input Voltage < 2.7V
Temperature	-40	25	85	oC	
Quiescent Current (PD=0, bypass=0)	-	100	-	uA	
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Quiescent Current (PD=1, bypass=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

7.4.3 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature=25°	1.7	2.0	2.3	V
	Temperature=-40°	-	2.4	-	V
	Temperature=85°	-	1.6	-	V
Hysteresis	-	0	0	0	V

7.4.4 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

7.4.5 Specification of Power-On Reset (5V)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.6 Specification of Temperature Sensor

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply voltage[1]	2.5	-	5.5	V	
Temperature	-40	-	125	℃	
Current consumption	6.4	-	10.5	uA	
Gain	-1.95	-2	-2.05	mV/℃	
Offset	688	708	730	mV	Temp=0 ℃

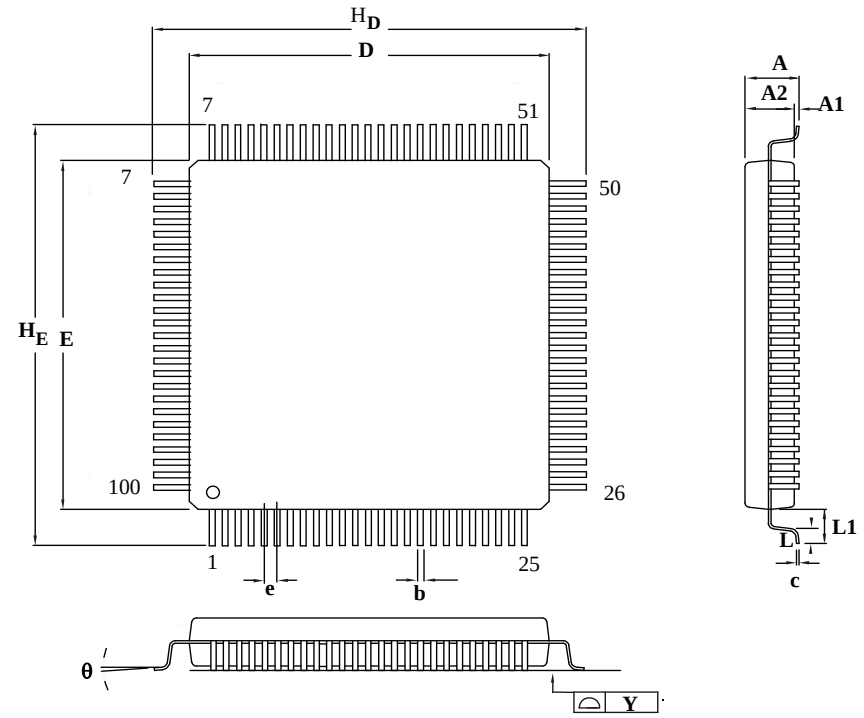
Notes:
1. Internal operation voltage comes form LDO.

7.4.7 Specification of Comparator

PARAMETER	MIN.	TYP.	MAX.	CONDITION
Temperature	-40℃	25 ℃	85℃	-
VDD	2.4	3	5.5	-
VDD current	-	20uA	40uA	20uA@VDD=3V
Input offset voltage	-	5mV	15mV	-
Output swing	0.1	-	VDD-0.1	-
Input common mode range	0.1	-	VDD-1.2	-
DC gain	-	70dB	-	-
Propagation delay	-	200ns	-	@VCM=1.2V & VDIFF=0.1V
Comparison voltage	10mV	20mV	-	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis
Hysteresis	-	±10mV	-	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V
Wake up time	-	-	2us	@CINP=1.3V CINN=1.2V

8 PACKAGE DIMENSIONS

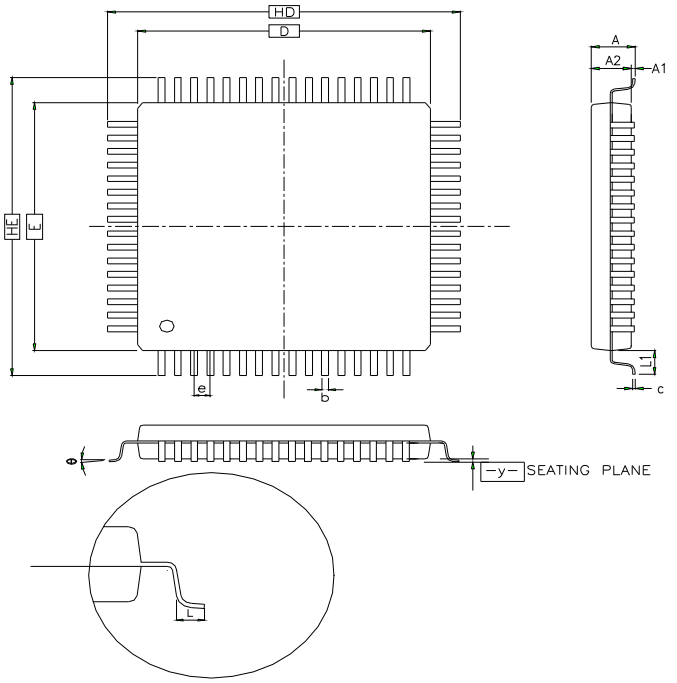
8.1.1 100L LQFP (14x14x1.4 mm footprint 2.0mm)



Controlling Dimension : Millimeters

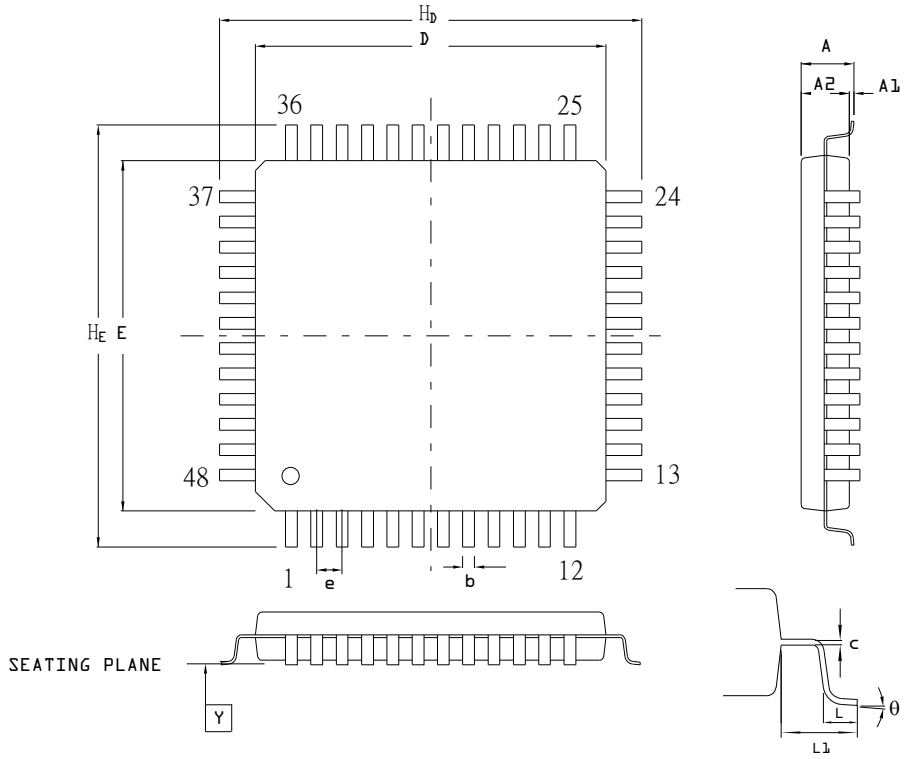
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

8.1.2 64L LQFP (10x10x1.4mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

8.1.3 48L LQFP (7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

9 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.00	March 1, 2010	-	Preliminary version initial issued
V1.01	April 9, 2010	Ch4	1. Modify the block diagram
V1.02	May 31, 2010	7.2	1. Add operation current of DC characteristics

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