

PDTC114E series

NPN resistor-equipped transistors;
R1 = 10 k Ω ; R2 = 10 k Ω

Rev. 11 — 21 November 2011

Product data sheet

1. Product profile

1.1 General description

NPN Resistor-Equipped Transistor (RET) family in small Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package			PNP complement	Package configuration
	NXP	JEITA	JEDEC		
PDTC114EE	SOT416	SC-75	-	PDTA114EE	ultra small
PDTC114EM	SOT883	SC-101	-	PDTA114EM	leadless ultra small
PDTC114ET	SOT23	-	TO-236AB	PDTA114ET	small
PDTC114EU	SOT323	SC-70	-	PDTA114EU	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Digital application in automotive and industrial segments
- Control of IC inputs
- Cost-saving alternative for BC847/857 series in digital applications
- Switching loads

1.4 Quick reference data

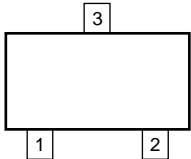
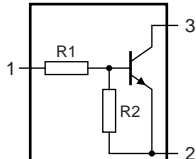
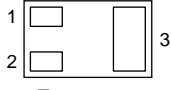
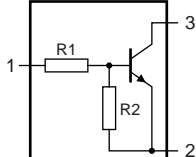
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	100	mA
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		0.8	1.0	1.2	



2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
SOT23; SOT323; SOT416			
1	input (base)	 <p>006aaa144</p>	 <p>sym007</p>
2	GND (emitter)		
3	output (collector)		
SOT883			
1	input (base)	 <p>Transparent top view</p>	 <p>sym007</p>
2	GND (emitter)		
3	output (collector)		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTC114EE	SC-75	plastic surface-mounted package; 3 leads	SOT416
PDTC114EM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTC114ET	-	plastic surface-mounted package; 3 leads	SOT23
PDTC114EU	SC-70	plastic surface-mounted package; 3 leads	SOT323

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PDTC114EE	09
PDTC114EM	DS
PDTC114ET	*16
PDTC114EU	*09

[1] * = placeholder fo manufacturing site code.

5. Limiting values

Table 6. Limiting values

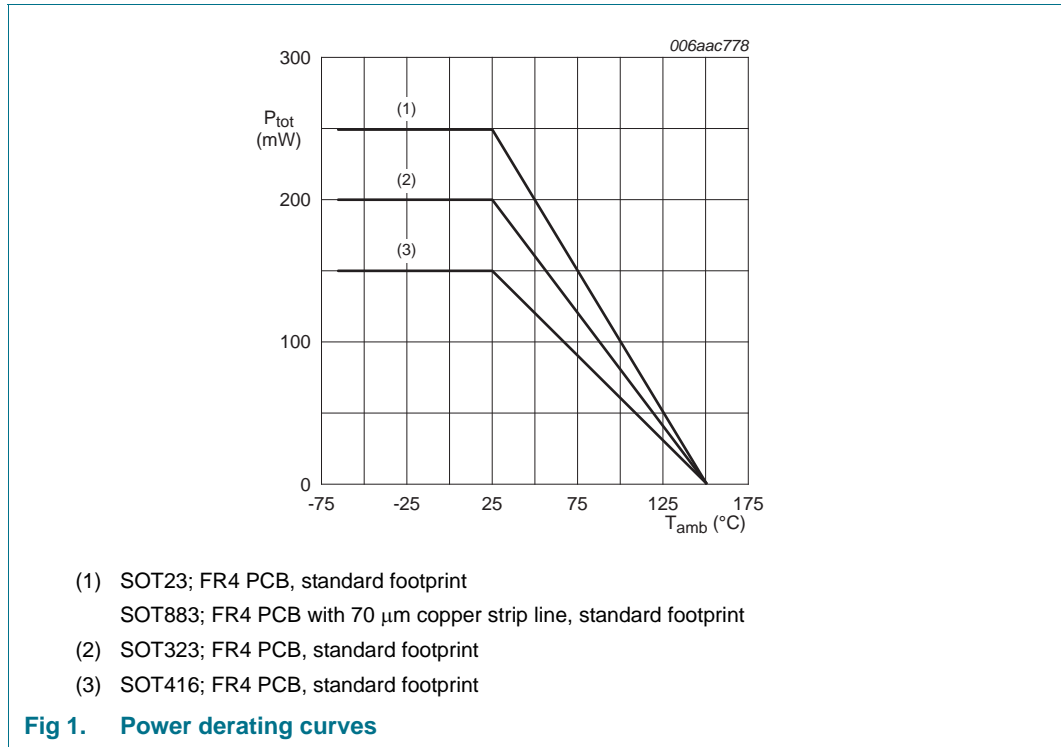
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V _{CBO}	collector-base voltage	open emitter	-	50	V	
V _{CEO}	collector-emitter voltage	open base	-	50	V	
V _{EBO}	emitter-base voltage	open collector	-	10	V	
V _I	input voltage					
	positive		-	+40	V	
	negative		-	-10	V	
I _O	output current		-	100	mA	
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	100	mA	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C				
	PDTC114EE (SOT416)		[1][2]	-	150	mW
	PDTC114EM (SOT883)		[2][3]	-	250	mW
	PDTC114ET (SOT23)		[1]	-	250	mW
	PDTC114EU (SOT323)		[1]	-	200	mW
T _j	junction temperature		-	150	°C	
T _{amb}	ambient temperature		-65	+150	°C	
T _{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.



6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air				
	PDTC114EE (SOT416)	[1][2]	-	-	830	K/W
	PDTC114EM (SOT883)	[2][3]	-	-	500	K/W
	PDTC114ET (SOT23)	[1]	-	-	500	K/W
	PDTC114EU (SOT323)	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

[3] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.



FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114EE (SOT416/SC-75); typical values



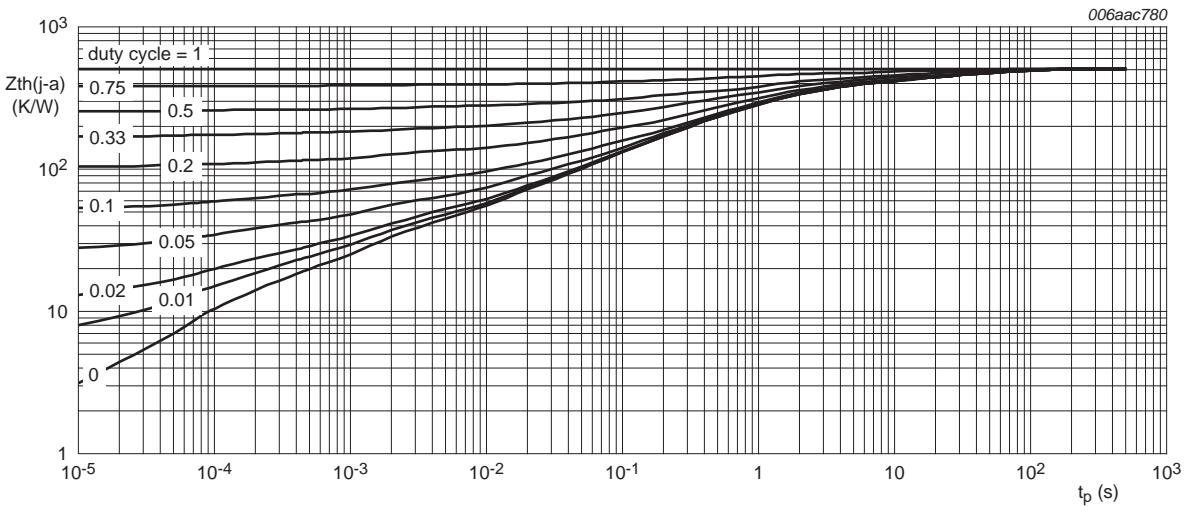
FR4 PCB, standard footprint

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114EM (SOT883/SC-101); typical values



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114ET (SOT23); typical values



FR4 PCB, 70 μm copper strip line, standard footprint

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration for PDTC114EU (SOT323/SC-70); typical values

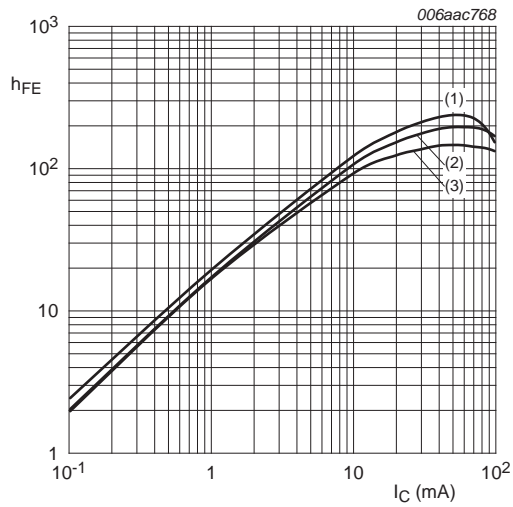
7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

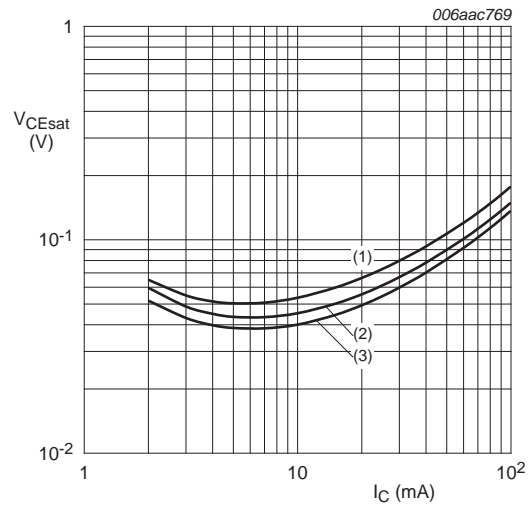
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	μA	
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ °C}$	-	-	5	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	400	μA	
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	30	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ μA}$	-	1.1	0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 10\text{ mA}$	2.5	1.8	-	V	
R1	bias resistor 1 (input)		7	10	13	kΩ	
R2/R1	bias resistor ratio		0.8	1.0	1.2		
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	2.5	pF	
f_T	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}$	[1]	-	230	-	MHz

[1] Characteristics of built-in transistor.



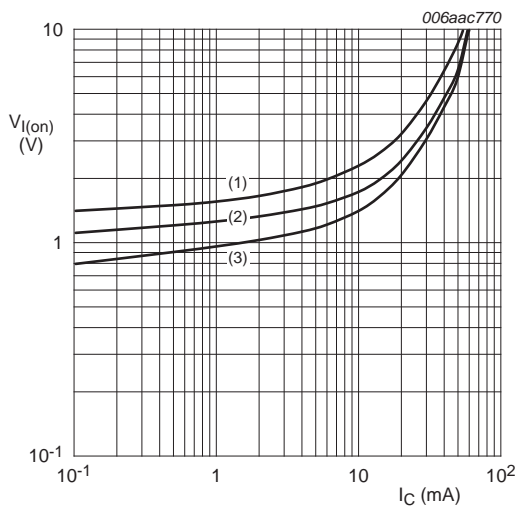
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 6. DC current gain as a function of collector current; typical values



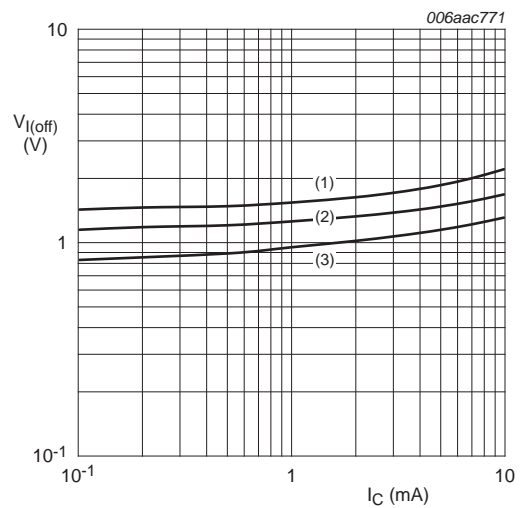
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig 7. Collector-emitter saturation voltage as a function of collector current; typical values



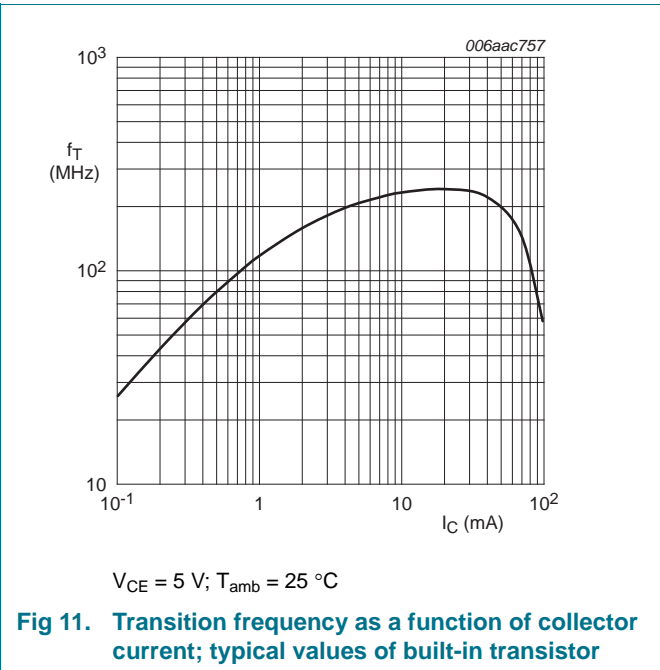
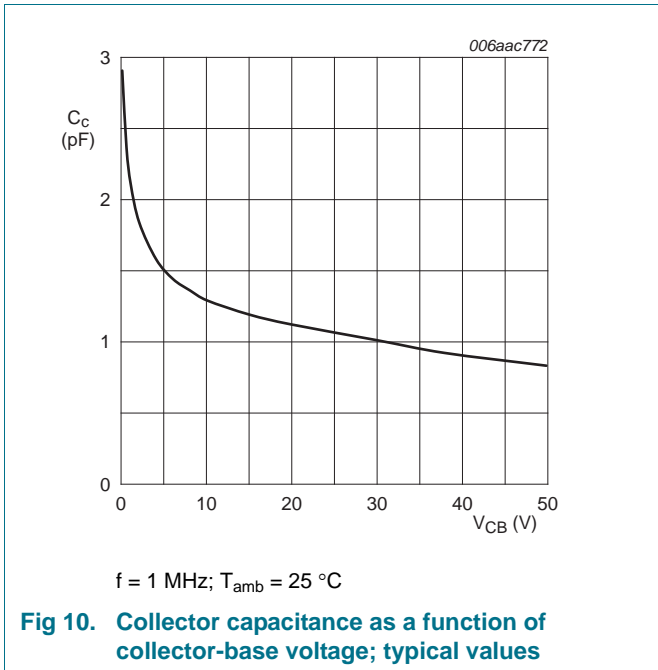
$V_{CE} = 0.3\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 8. On-state input voltage as a function of collector current; typical values



$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 9. Off-state input voltage as a function of collector current; typical values

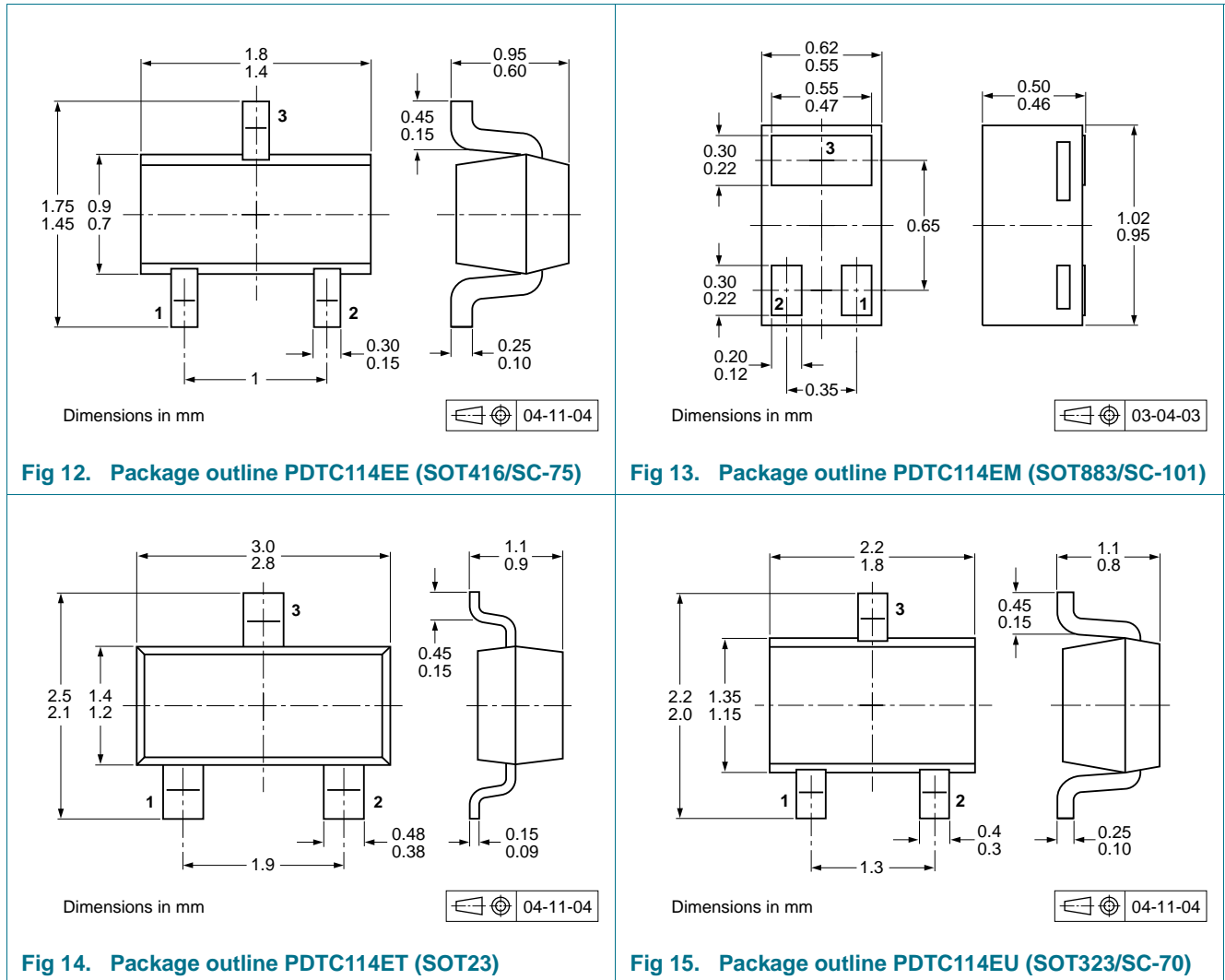


8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PDTC114EE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-135
PDTC114EM	SOT883	2 mm pitch, 8 mm tape and reel	-	-315
PDTC114ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235
PDTC114EU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-135

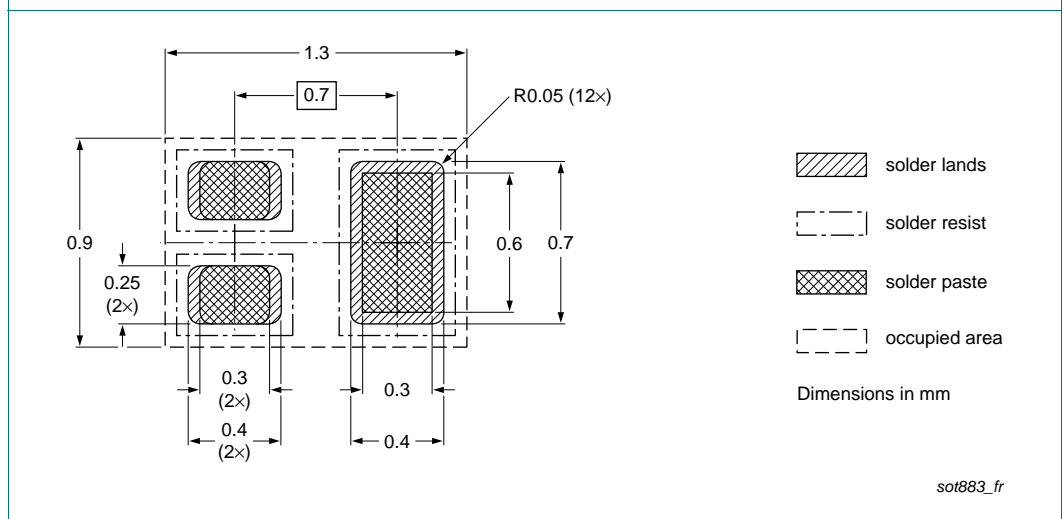
[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 16. Reflow soldering footprint PDTC114EE (SOT416/SC-75)



Reflow soldering is the only recommended soldering method.

Fig 17. Reflow soldering footprint PDTC114EM (SOT883/SC-101)

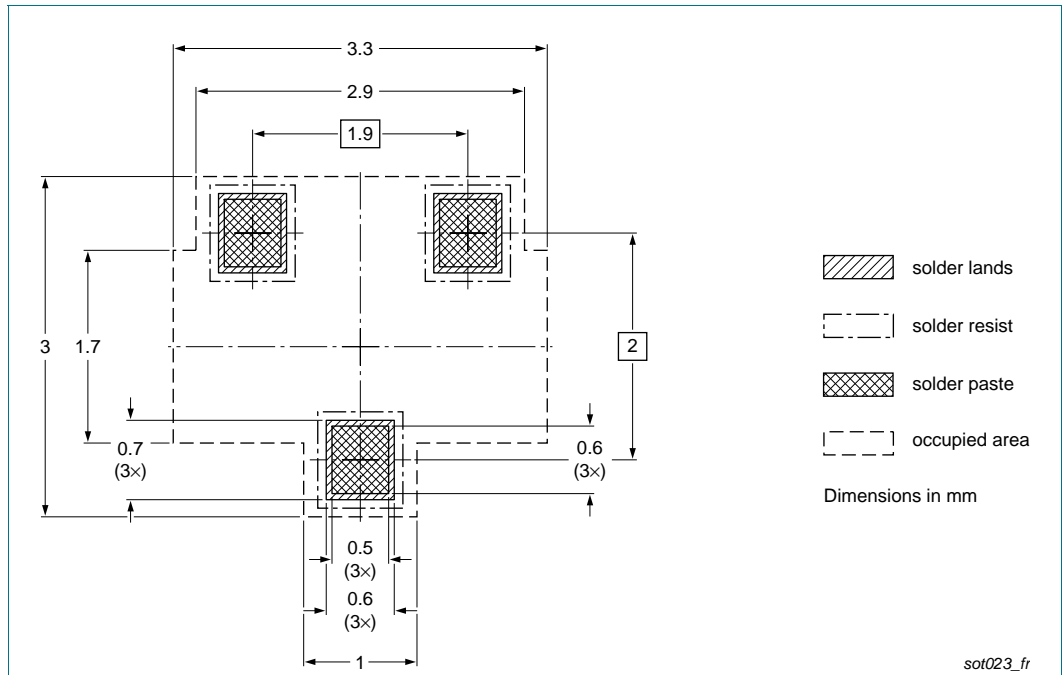


Fig 18. Reflow soldering footprint PDTC114ET (SOT23)

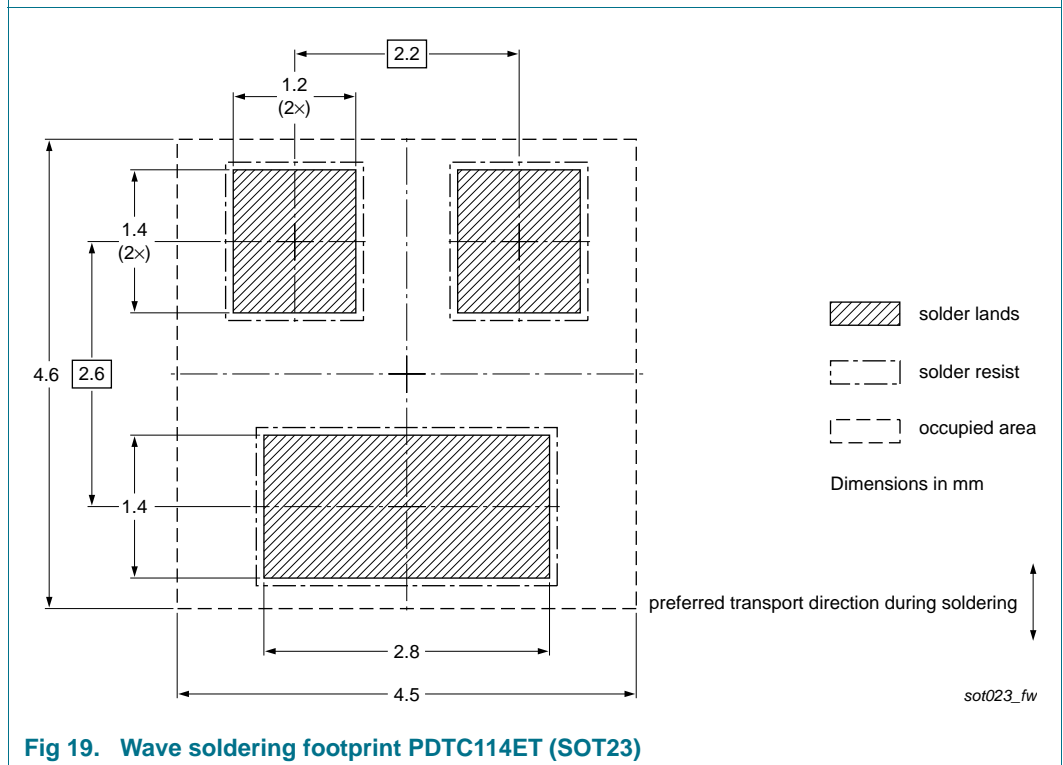


Fig 19. Wave soldering footprint PDTC114ET (SOT23)

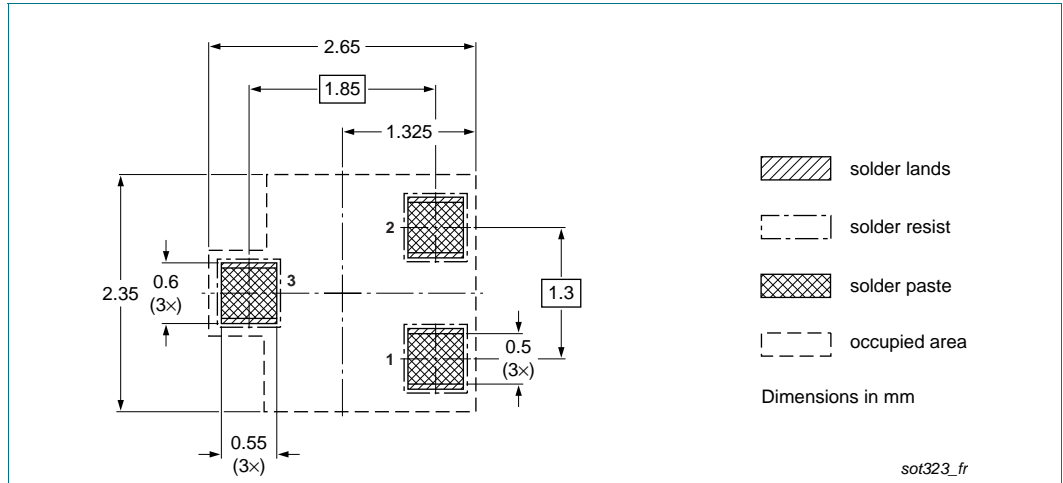


Fig 20. Reflow soldering footprint PDTC114EU (SOT323/SC-70)

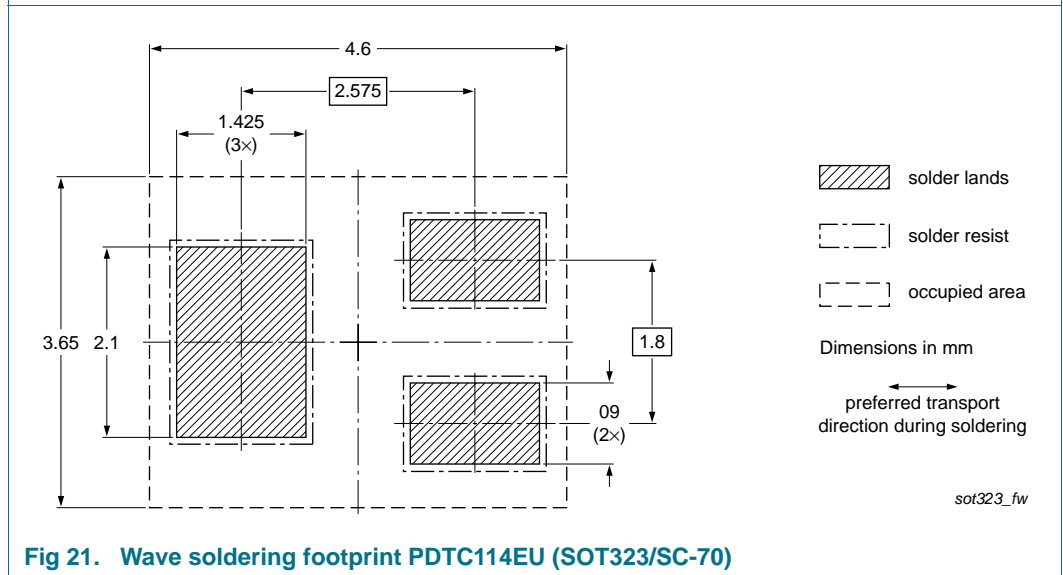


Fig 21. Wave soldering footprint PDTC114EU (SOT323/SC-70)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTC114E_SER v.11	20111121	Product data sheet	-	PDTC114E_SERIES v.10
Modifications:		<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Type numbers PDTC114EEF, PDTC114EK and PDTC114ES: removed Section 1 "Product profile": amended Figure 1 to 11: added Table 8 "Characteristics": $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated and f_T added Figure 12, 13, 14 and 15: superseded by minimized package outline drawings Section 8 "Test information": added Section 10 "Packing information": added Section 11 "Soldering": added Section 13 "Legal information": updated 		
PDTC114E_SERIES v.10	20040805	Product specification	-	PDTC114E_SERIES v.9
PDTC114E_SERIES v.9	20030410	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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