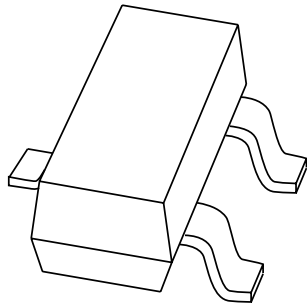


# DATA SHEET



**PBSS4160T**

60 V, 1 A

NPN low  $V_{CEsat}$  (BISS) transistor

Product data sheet  
Supersedes data of 2003 Jun 24

2004 May 12

# 60 V, 1 A NPN low $V_{CEsat}$ (BISS) transistor

**PBSS4160T**

**FEATURES**

- Low collector-emitter saturation voltage  $V_{CEsat}$
- High collector current capability  $I_C$  and  $I_{CM}$
- High efficiency, reduces heat generation
- Reduces printed-circuit board area required
- Cost effective replacement for medium power transistor BCP55 and BCX55.

**APPLICATIONS**

- Major application segments:
  - Automotive 42 V power
  - Telecom infrastructure
  - Industrial.
- Power management:
  - DC-to-DC conversion
  - Supply line switching.
- Peripheral driver
  - Driver in low supply voltage applications (e.g. lamps and LEDs)
  - Inductive load driver (e.g. relays, buzzers and motors).

**DESCRIPTION**

NPN low  $V_{CEsat}$  transistor in a SOT23 plastic package. PNP complement: PBSS5160T.

**MARKING**

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PBSS4160T	*U5

**Note**

1. \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS4160T	–	plastic surface mounted package; 3 leads	SOT23

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	60	V
$I_C$	collector current (DC)	1	A
$I_{CM}$	peak collector current	2	A
$R_{CEsat}$	equivalent on-resistance	250	m $\Omega$

**PINNING**

PIN	DESCRIPTION
1	base
2	emitter
3	collector

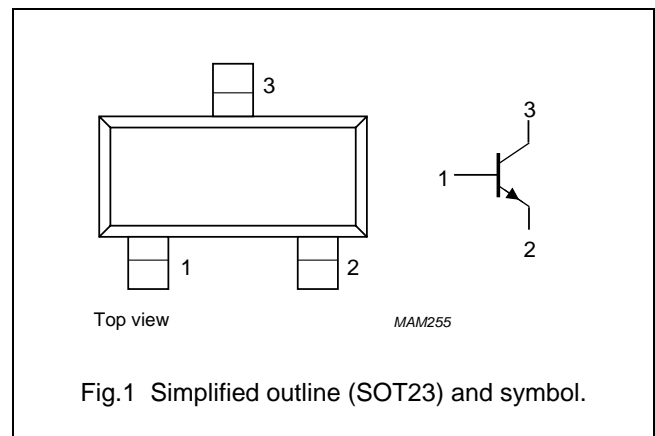


Fig.1 Simplified outline (SOT23) and symbol.

60 V, 1 A  
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PBSS4160T

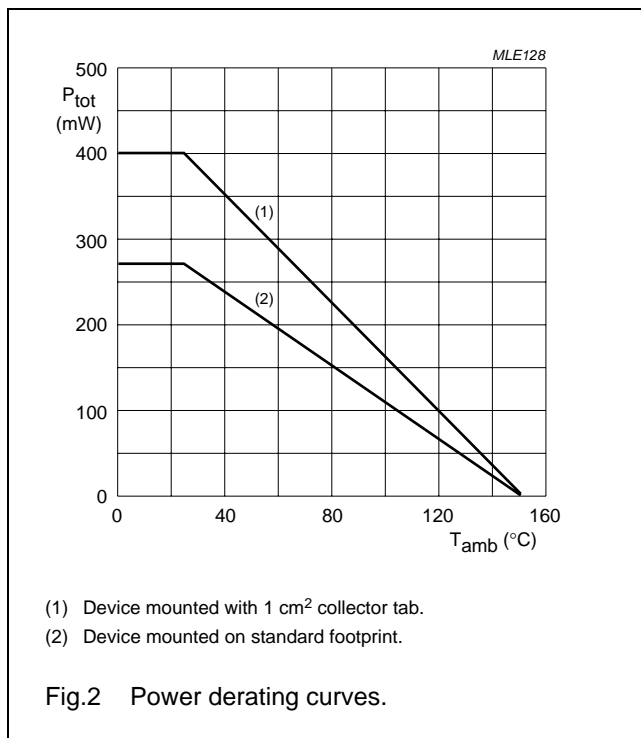
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	80	V
$V_{CEO}$	collector-emitter voltage	open base	–	60	V
$V_{EBO}$	emitter-base voltage	open collector	–	5	V
$I_C$	collector current (DC)	note 1	–	0.9	A
		note 2	–	1	A
$I_{CM}$	peak collector current	$t = 1 \text{ ms}$ or limited by $T_{j(max)}$	–	2	A
$I_B$	base current (DC)		–	300	mA
$I_{BM}$	peak base current	$t_p \leq 300 \mu\text{s}; \delta \leq 0.02$	–	1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$ ; note 1	–	270	mW
		$T_{amb} \leq 25 \text{ }^\circ\text{C}$ ; note 2	–	400	mW
		$T_{amb} \leq 25 \text{ }^\circ\text{C}$ ; notes 1 and 3	–	1.25	W
$T_{stg}$	storage temperature		–65	+150	$^\circ\text{C}$
$T_j$	junction temperature		–	150	$^\circ\text{C}$
$T_{amb}$	operating ambient temperature		–65	+150	$^\circ\text{C}$

**Notes**

1. Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated, standard footprint.
2. Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated, 1 cm<sup>2</sup> collector mounting pad.
3. Operated under pulsed conditions: duty cycle  $\delta \leq 20\%$ , pulse width  $t_p \leq 10 \text{ ms}$ .



60 V, 1 A  
NPN low  $V_{CEsat}$  (BISS) transistor

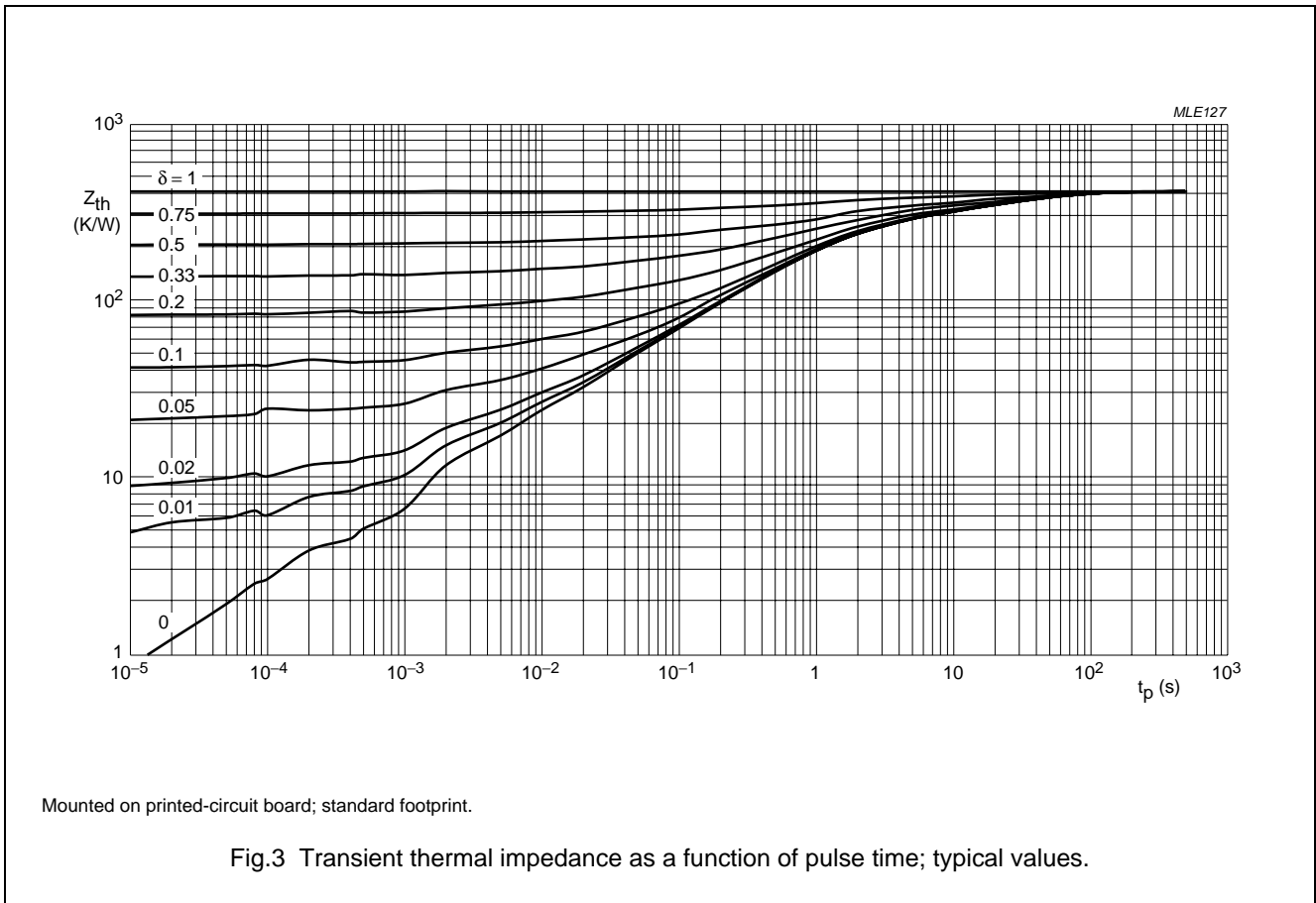
PBSS4160T

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; note 1	465	K/W
		in free air; note 2	312	K/W
		in free air; notes 1 and 3	100	K/W

Notes

1. Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.
2. Device mounted on an FR4 printed-circuit board, single-sided copper, tin-plated and 1 cm<sup>2</sup> collector mounting pad.
3. Operated under pulsed conditions: duty cycle  $\delta \leq 20\%$ , pulse width  $t_p \leq 10$  ms.



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PBSS4160T

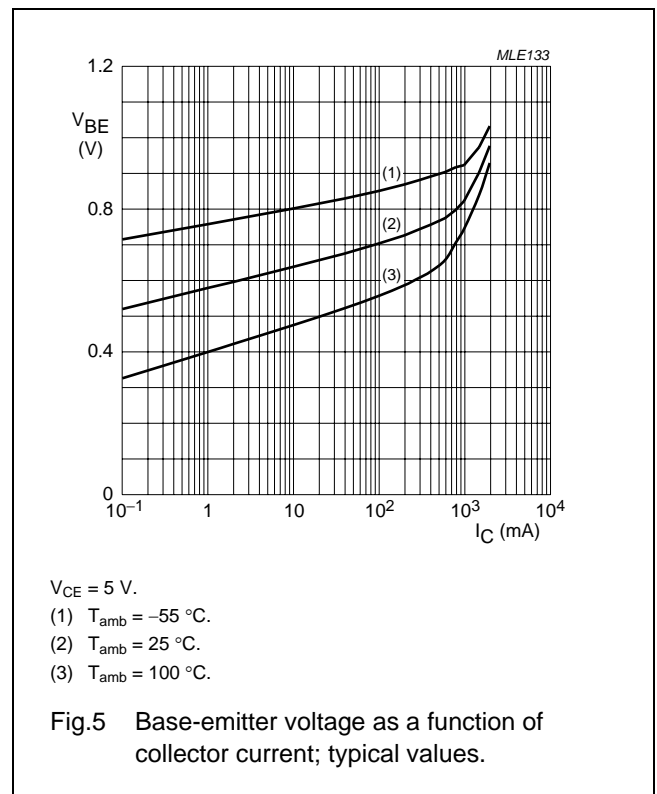
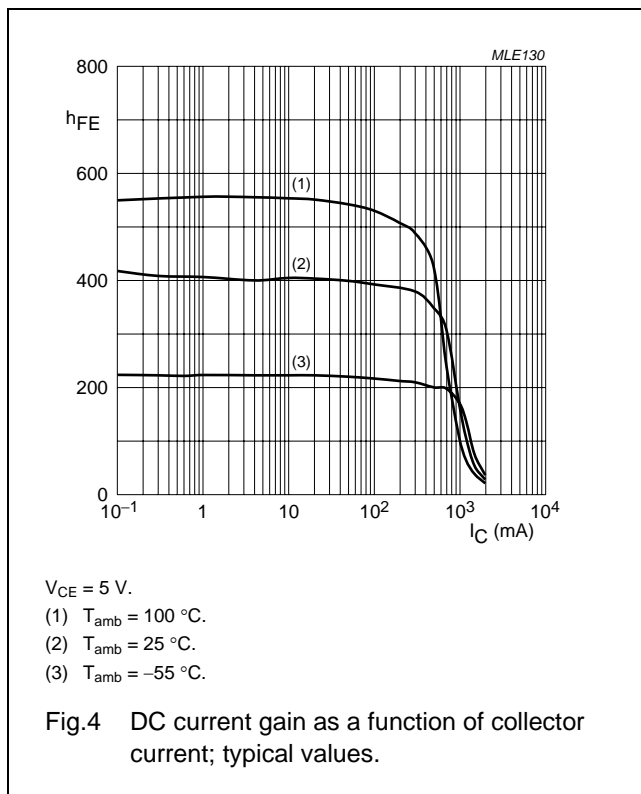
**CHARACTERISTICS**

$T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 60\text{ V}; I_E = 0\text{ A}$	–	–	100	nA
		$V_{CB} = 60\text{ V}; I_E = 0\text{ A}; T_J = 150\text{ }^{\circ}\text{C}$	–	–	50	$\mu\text{A}$
$I_{CES}$	collector-emitter cut-off current	$V_{CE} = 60\text{ V}; V_{BE} = 0\text{ A}$	–	–	100	nA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	–	–	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	250	400	–	
		$V_{CE} = 5\text{ V}; I_C = 500\text{ mA}; \text{note 1}$	200	350	–	
		$V_{CE} = 5\text{ V}; I_C = 1\text{ A}; \text{note 1}$	100	150	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 100\text{ mA}; I_B = 1\text{ mA}$	–	90	110	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	110	140	mV
		$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	200	250	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 1\text{ A}; I_B = 50\text{ mA}$	–	0.95	1.1	V
$R_{CEsat}$	equivalent on-resistance	$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	–	200	250	$\text{m}\Omega$
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ A}$	–	0.82	0.9	V
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	150	220	–	MHz
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$	–	5.5	10	pF

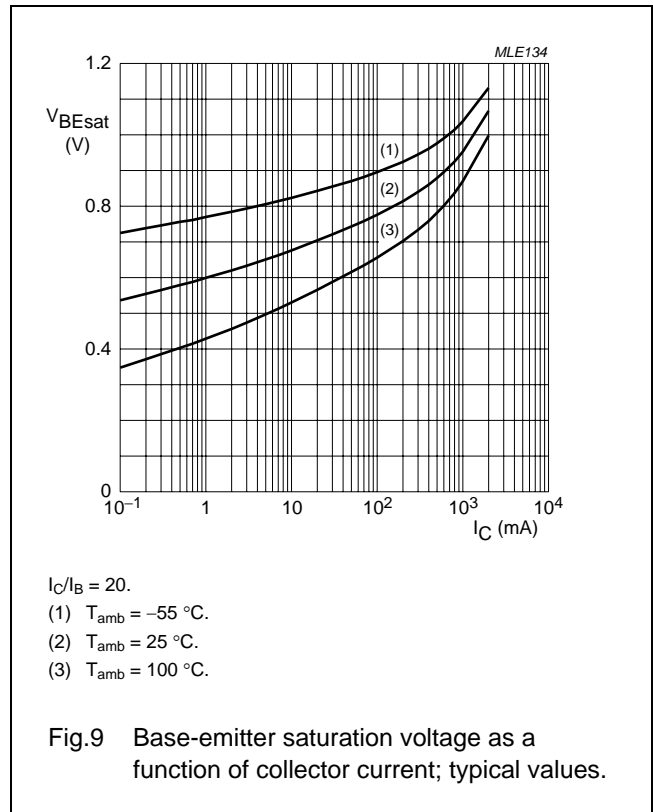
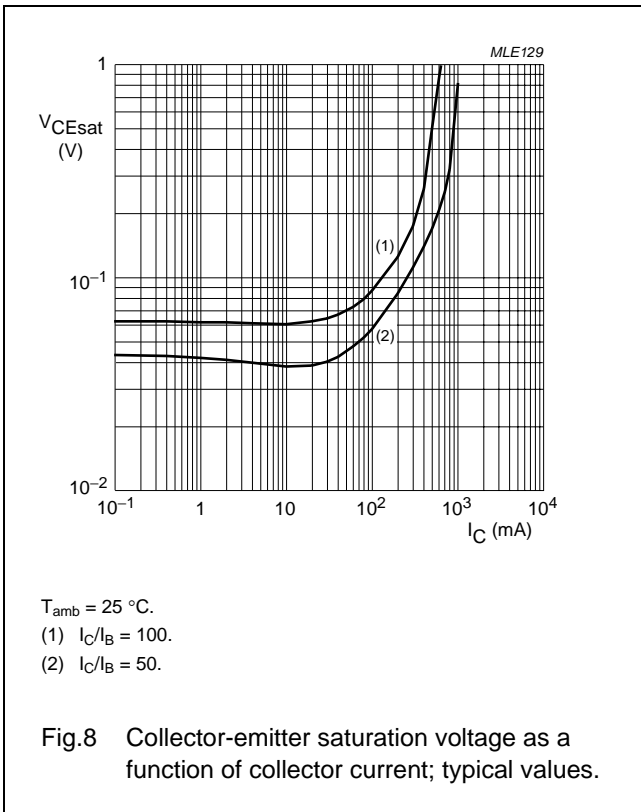
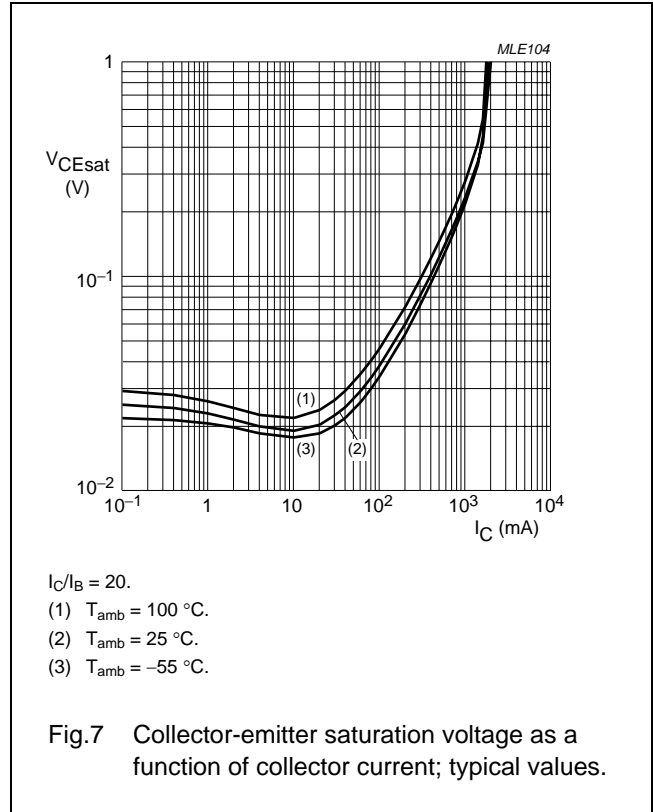
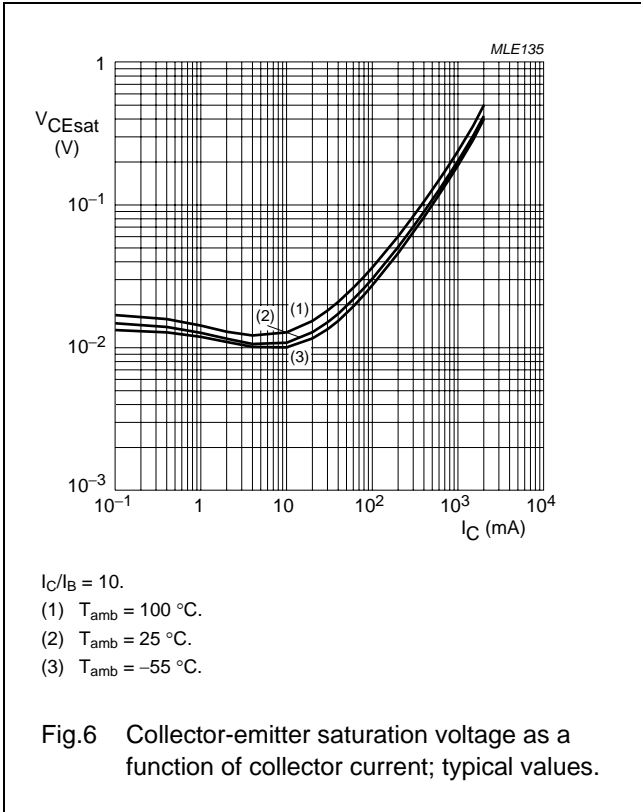
**Note**

1. Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .



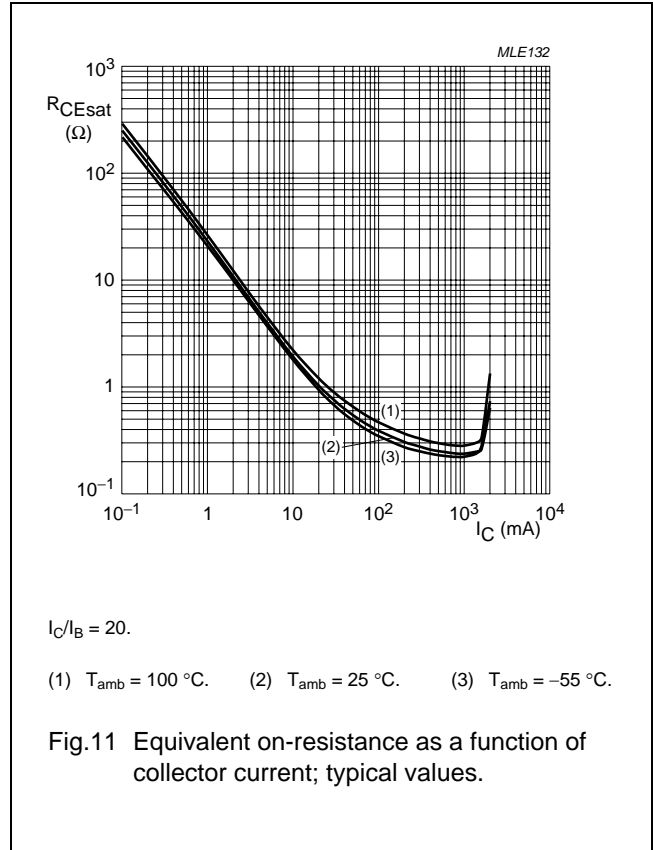
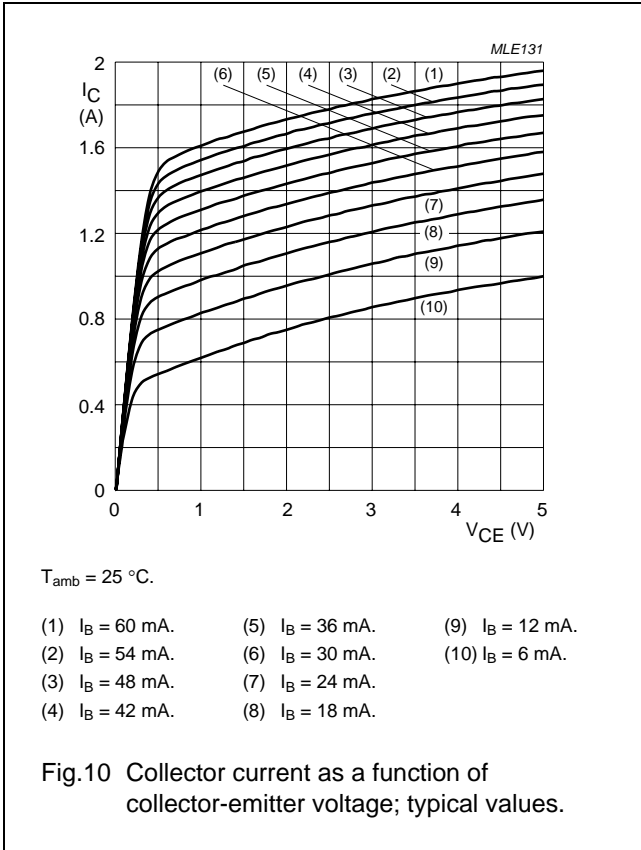
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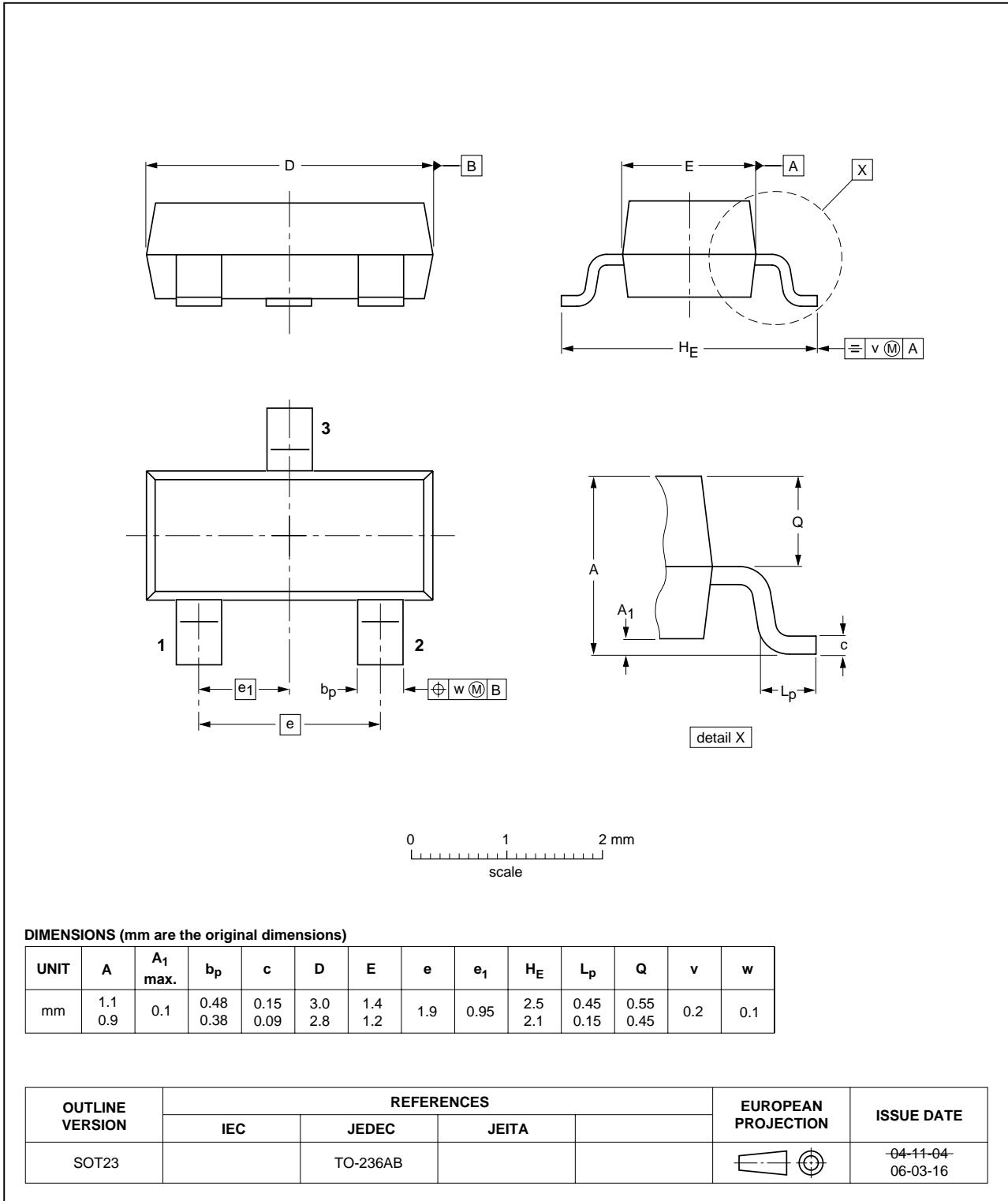
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PBSS4160T

PACKAGE OUTLINE

Plastic surface-mounted package; 3 leads

SOT23





60 V, 1 A  
NPN low  $V_{CEsat}$  (BISS) transistor

PBSS4160T

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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## **Contact information**

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