NTD2955

Power MOSFET
12 Amps, 60 Volts
P−Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low−voltage, high−speed switching applications in power supplies, converters, and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

Features

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Designed for Low−Voltage, High−Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes
- Pb−Free Packages are Available

MAXIMUM RATINGS (Tj = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Gate−to−Source Voltage − Continuous − Non−repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current − Continuous @ T_a = 25°C − Single Pulse ($t_p \le 10$ ms)	I_D I_{DM}	12 36	Adc Apk
Total Power Dissipation @ T_a = 25°C	P_D	55	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.73 71.4 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 in. from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1 in. pad size (Cu. area = 1.127 in^2)
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu. area = 0.412 in^2)

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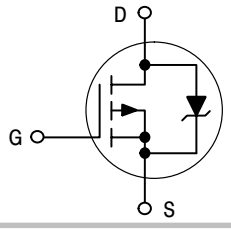
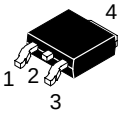
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
60 V	155 mΩ @ 10 V, 6 A	12 A

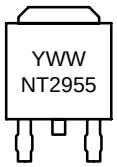
P−Channel





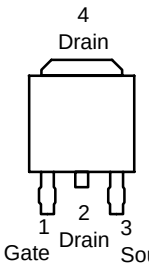
DPAK
CASE 369A
Style 2

MARKING DIAGRAM



Y = Year
WW = Work Week
T = MOSFET

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTD2955−1	DPAK	75 Units/Rail
NTD2955		75 Units/Rail
NTD2955T4		2500 Tape & Reel
NTD2955−1G	DPAK (Pb−Free)	75 Units/Rail
NTD2955G		75 Units/Rail
NTD2955T4G		2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 0.25 μA) (Positive Temperature Coefficient)		$V_{(BR)DSS}$	60 −	− 67	− −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 60 Vdc, T_J = 25°C) (V_{GS} = 0 Vdc, V_{DS} = 60 Vdc, T_J = 150°C)		I_{DSS}	− −	− −	10 100	μAdc
Gate−Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (Negative Temperature Coefficient)		$V_{GS(th)}$	2.0 −	2.8 4.5	4.0 −	Vdc mV/°C
Static Drain−Source On−State Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	−	0.155	0.180	Ω
Drain−to−Source On−Voltage (V_{GS} = 10 Vdc, I_D = 12 Adc) (V_{GS} = 10 Vdc, I_D = 6.0 Adc, T_J = 150°C)		$V_{DS(on)}$		1.86 −	2.6 2.0	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6.0 Adc)		g_{FS}		8.0	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, F = 1.0 MHz)	C_{iss}	−	500	750	pF
Output Capacitance		C_{oss}	−	150	250	
Reverse Transfer Capacitance		C_{rss}	−	50	100	
SWITCHING CHARACTERISTICS (Notes 3 and 4)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 A, V_{GS} = 10 V, R_G = 9.1 Ω)	$t_{d(on)}$	−	10	20	ns
Rise Time		t_r	−	45	85	
Turn−Off Delay Time		$t_{d(off)}$	−	26	40	
Fall Time		t_f	−	48	90	
Gate Charge	(V_{DS} = 48 Vdc, V_{GS} = 10 Vdc, I_D = 12 A,)	Q_T	−	15	30	nC
		Q_{GS}	−	4.0	−	
		Q_{GD}	−	7.0	−	
DRAIN−SOURCE DIODE CHARACTERISTICS (Note 3)						
Diode Forward On−Voltage (I_S = 12 Adc, V_{GS} = 0 V) (I_S = 12 Adc, V_{GS} = 0 V, T_J = 150°C)		V_{SD}	− −	1.6 1.3	2.5 −	Vdc
Reverse Recovery Time (I_S = 12 A, dI_S/dt = 100 A/μs ,V_{GS} = 0 V)		t_{rr}	−	50		ns
		t_a	−	40	−	
		t_b	−	10	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.10	−	μC

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%
4. Switching characteristics are independent of operating junction temperature

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

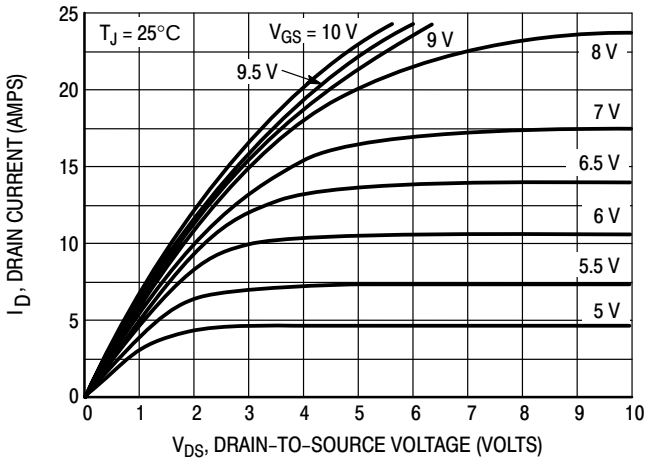


Figure 1. On−Region Characteristics

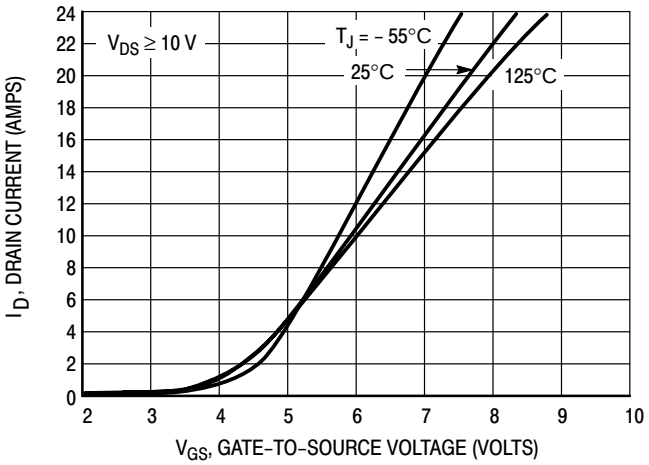


Figure 2. Transfer Characteristics

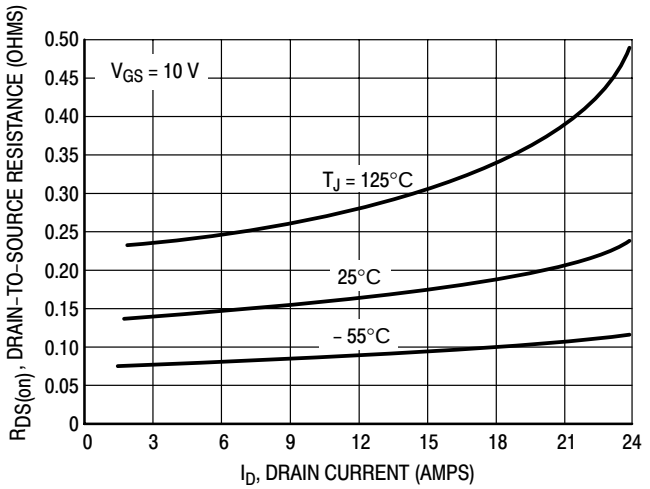


Figure 3. On−Resistance versus Drain Current and Temperature

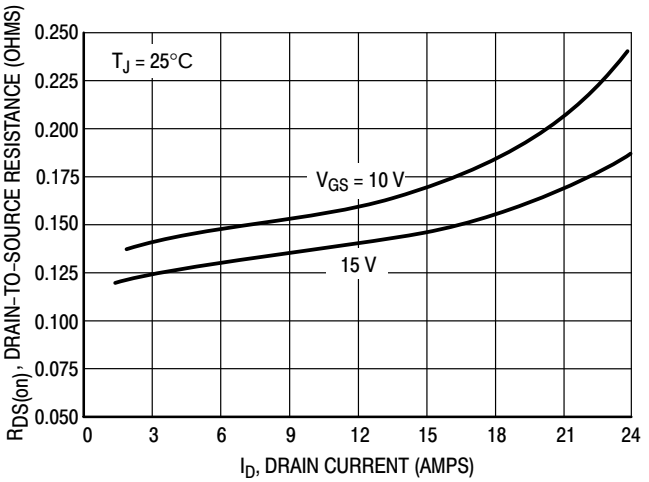


Figure 4. On−Resistance versus Drain Current and Gate Voltage

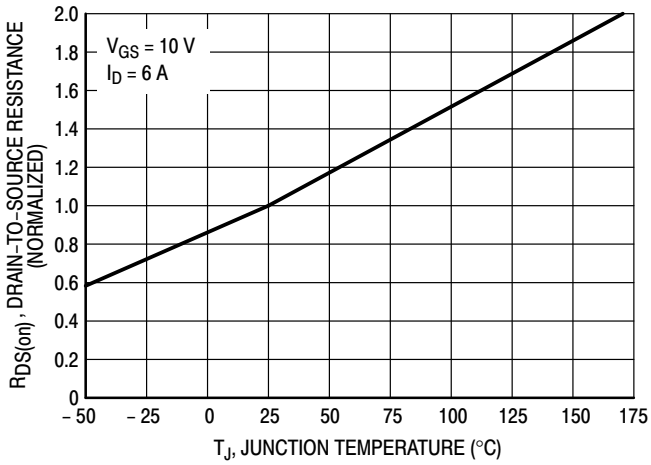


Figure 5. On−Resistance Variation with Temperature

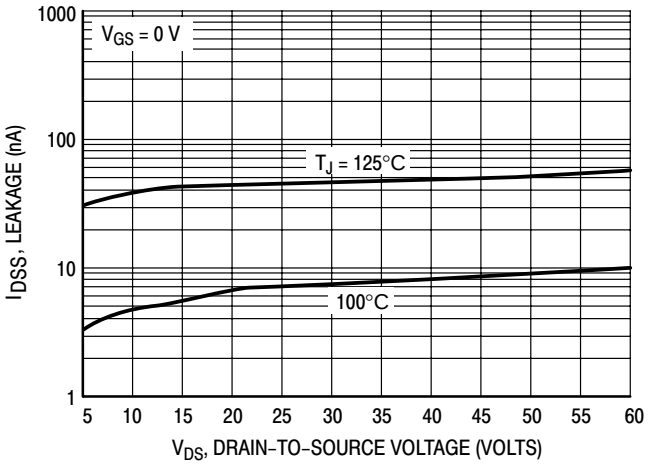


Figure 6. Drain−To−Source Leakage Current versus Voltage

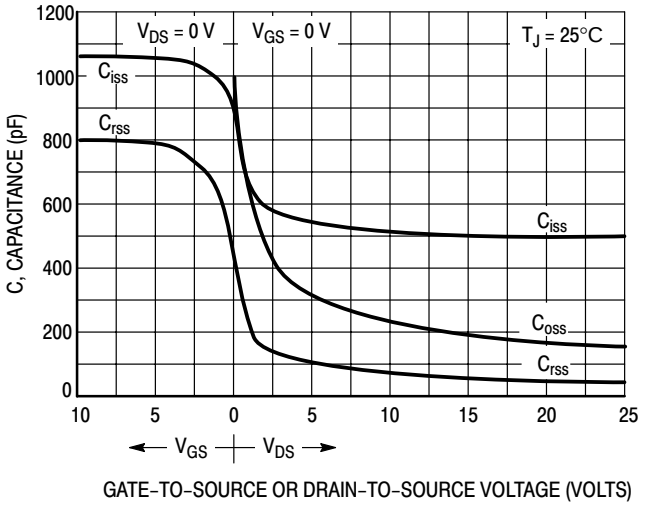


Figure 7. Capacitance Variation

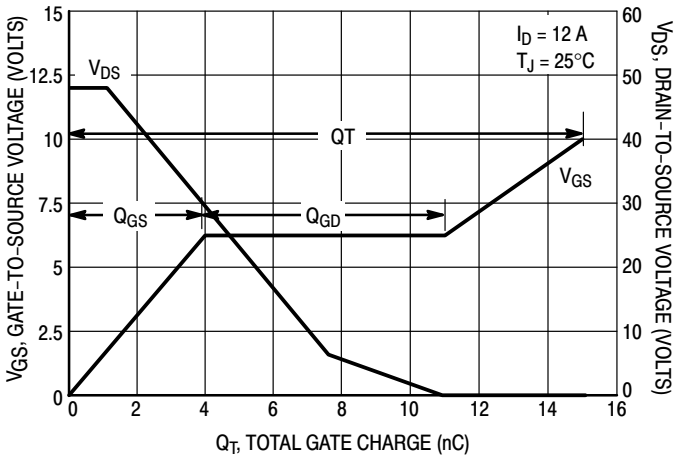


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

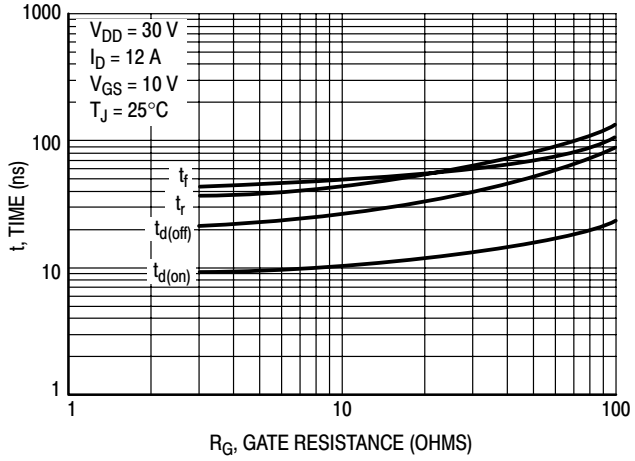


Figure 9. Resistive Switching Time Variation versus Gate Resistance

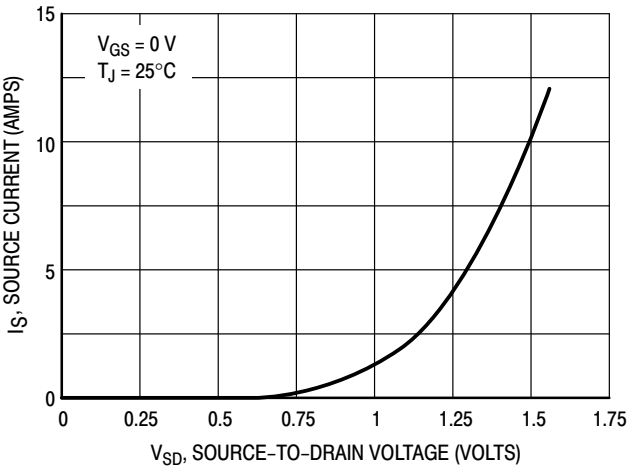


Figure 10. Diode Forward Voltage versus Current

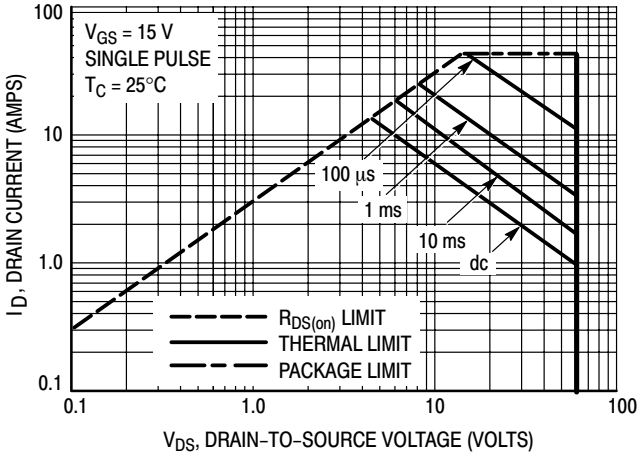


Figure 11. Maximum Rated Forward Biased Safe Operating Area

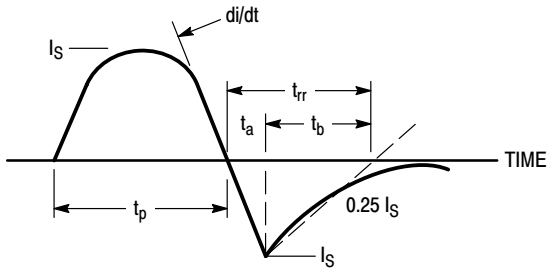


Figure 12. Diode Reverse Recovery Waveform

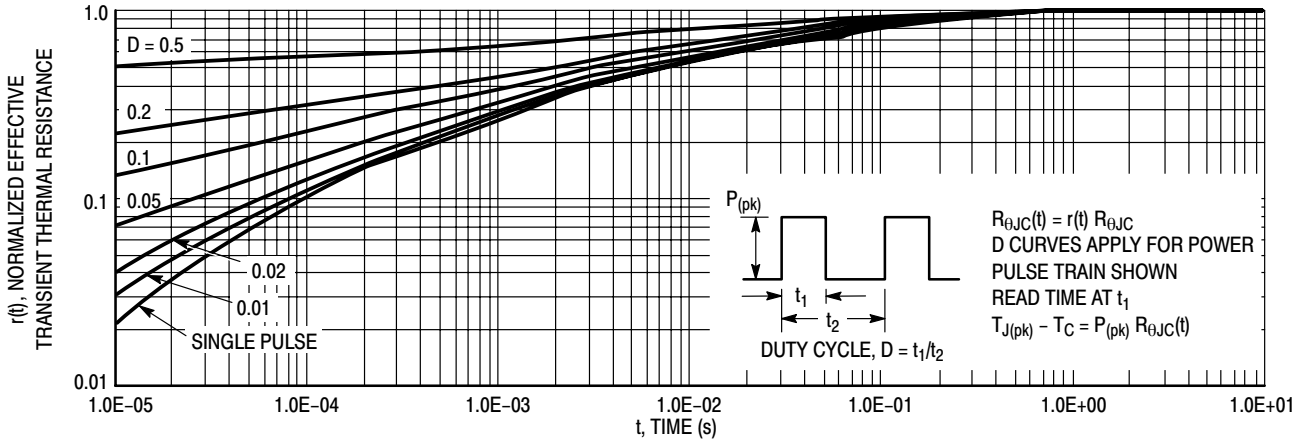
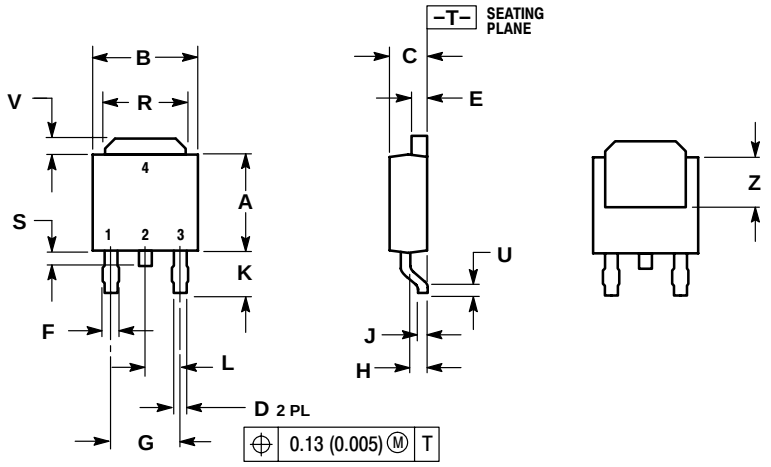


Figure 13. Thermal Response

PACKAGE DIMENSIONS

DPAK
CASE 369A−13
ISSUE AB

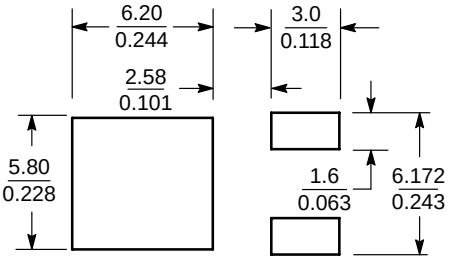


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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