

# MC14049UB

## Hex Buffers

The MC14049UB hex inverter/buffer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS device finds primary use where low power dissipation and/or high noise immunity is desired. This device provides logic-level conversion using only one supply voltage,  $V_{DD}$ . The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic-level conversions. Two TTL/DTL Loads can be driven when the device is used as CMOS-to-TTL/DTL converters ( $V_{DD} = 5.0\text{ V}$ ,  $V_{OL} \leq 0.4\text{ V}$ ,  $I_{OL} \geq 3.2\text{ mA}$ ). Note that pins 13 and 16 are not connected internally on this device; consequently connections to these terminals will not affect circuit operation.

### Features

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- Meets JEDEC UB Specifications
- $V_{IN}$  can exceed  $V_{DD}$
- Improved ESD Protection on All Inputs
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage Range	-0.5 to +18.0	V
$V_{in}$	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
$V_{out}$	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD}$ +0.5	V
$I_{in}$	Input Current (DC or Transient) per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient) per Pin	+45	mA
$P_D$	Power Dissipation, per Package (Note 1)	825 740	mW
$T_A$	Ambient Temperature Range	-55 to +125	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating: All Packages: See Figure 4.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin, only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18\text{ V}$  and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

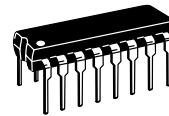
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



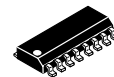
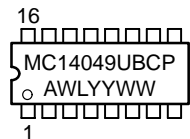
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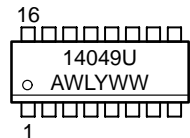
### MARKING DIAGRAMS



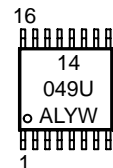
PDIP-16  
P SUFFIX  
CASE 648



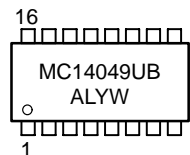
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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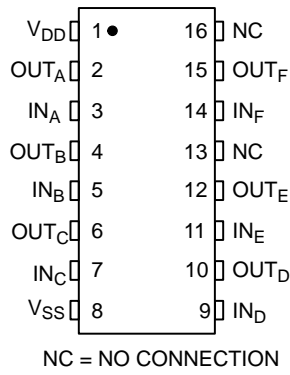


Figure 1. Pin Assignment

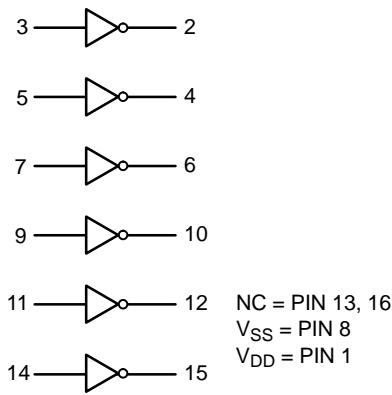


Figure 2. Logic Diagram  
MC14049UB

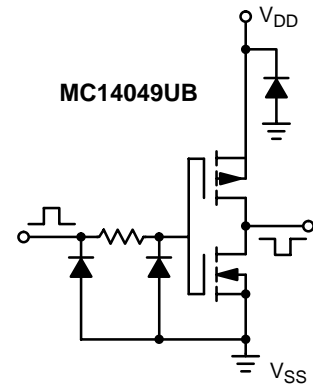


Figure 3. Circuit Schematic  
(1/6 of circuit shown)

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	$V_{OL}$	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
$V_{in} = 0$ or $V_{DD}$	"1" Level	$V_{OH}$	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage ( $V_O = 4.5$ Vdc) ( $V_O = 9.0$ Vdc) ( $V_O = 13.5$ Vdc)	"0" Level	$V_{IL}$	5.0	-	1.0	-	2.25	1.0	-	1.0	Vdc
			10	-	2.0	-	4.50	2.0	-	2.0	
$V_O = 0.5$ Vdc) ( $V_O = 1.0$ Vdc) ( $V_O = 1.5$ Vdc)	"1" Level	$V_{IH}$	5.0	4.0	-	4.0	2.75	-	4.0	-	Vdc
			10	8.0	-	8.0	5.50	-	8.0	-	
			15	12.5	-	12.5	8.25	-	12.5	-	
Output Drive Current ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)	Source	$I_{OH}$	5.0	-1.6	-	-1.25	-2.5	-	-1.0	-	mAdc
	Sink	$I_{OL}$	5.0	3.75	-	3.2	6.0	-	2.6	-	
$V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)			10	10	-	8.0	16	-	6.6	-	
			15	30	-	24	40	-	19	-	
			15	30	-	24	40	-	19	-	
Input Current		$I_{in}$	15	-	±0.1	-	±0.000 01	±0.1	-	±1.0	μAdc
Input Capacitance ( $V_{in} = 0$ )		$C_{in}$	-	-	-	-	10	20	-	-	pF
Quiescent Current (Per Package)		$I_{DD}$	5.0	-	1.0	-	0.002	1.0	-	30	μAdc
			10	-	2.0	-	0.004	2.0	-	60	
			15	-	4.0	-	0.006	4.0	-	120	
Total Supply Current (Note 3 and 4) (Dynamic plus Quiescent, Per Package) ( $C_L = 50$ pF on all outputs, all buffers switching)		$I_T$	5.0	$I_T = (1.8 \mu A/kHz) f + I_{DD}$						μAdc	
			10	$I_T = (3.5 \mu A/kHz) f + I_{DD}$							
			15	$I_T = (5.3 \mu A/kHz) f + I_{DD}$							

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in μA (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.002$ .

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## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (0.8 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 35 \text{ ns}$ $t_{TLH} = (0.27 \text{ ns/pF}) C_L + 26.5 \text{ ns}$	$t_{TLH}$	5.0 10 15	- - -	100 50 40	160 100 60	ns
Output Fall Time $t_{THL} = (0.3 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.12 \text{ ns/pF}) C_L + 14 \text{ ns}$ $t_{THL} = (0.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{THL}$	5.0 10 15	- - -	40 20 15	60 40 30	ns
Propagation Delay Time $t_{PLH} = (0.38 \text{ ns/pF}) C_L + 61 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{PLH} = (0.11 \text{ ns/pF}) C_L + 24.5 \text{ ns}$	$t_{PLH}$	5.0 10 15	- - -	80 40 30	120 65 50	ns
Propagation Delay Time $t_{PHL} = (0.38 \text{ ns/pF}) C_L + 11 \text{ ns}$ $t_{PHL} = (0.12 \text{ ns/pF}) C_L + 9 \text{ ns}$ $t_{PHL} = (0.11 \text{ ns/pF}) C_L + 4.5 \text{ ns}$	$t_{PHL}$	5.0 10 15	- - -	30 15 10	60 30 20	ns

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

## ORDERING INFORMATION

Device	Package	Shipping†
MC14049UBCP	PDIP-16	2,000 Units / Box
MC14049UBCPG	PDIP-16 (Pb-Free)	2,000 Units / Box
MC14049UBD	SOIC-16	2,400 Units / Box
MC14049UBDG	SOIC-16 (Pb-Free)	2,400 Units / Box
MC14049UBDR2	SOIC-16	2,500 / Tape & Reel
MC14049UBDR2G	SOIC-16 (Pb-Free)	2,500 / Tape & Reel
MC14049UBDT	TSSOP-16	96 Units / Rail
MC14049UBDTEL	TSSOP-16*	96 Units / Rail
MC14049UBDTR2	TSSOP-16*	2,500 / Tape & Reel
MC14049UBF	SOEIAJ-16	See Note 7
MC14049UBFEL	SOEIAJ-16	See Note 7

7. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

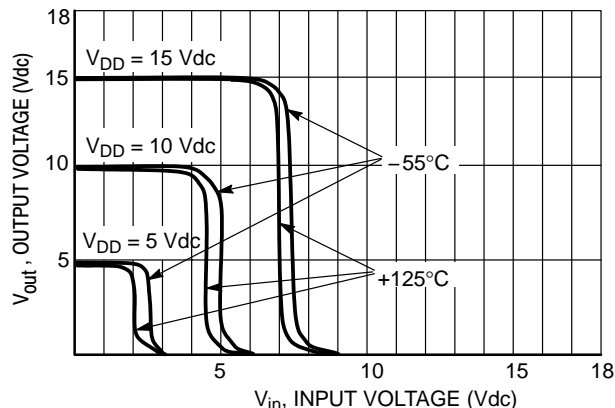


Figure 4. Typical Voltage Transfer Characteristics versus Temperature

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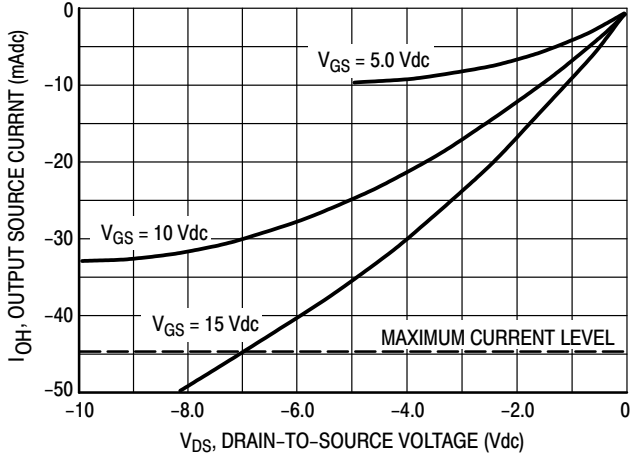
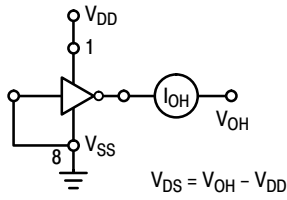


Figure 5. Typical Output Source Characteristics

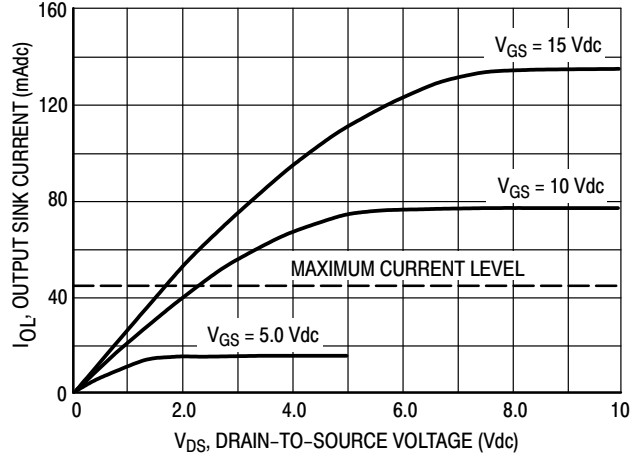
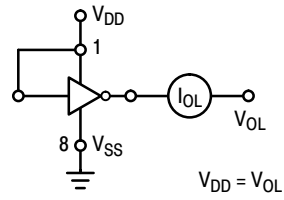


Figure 6. Typical Output Sink Characteristics

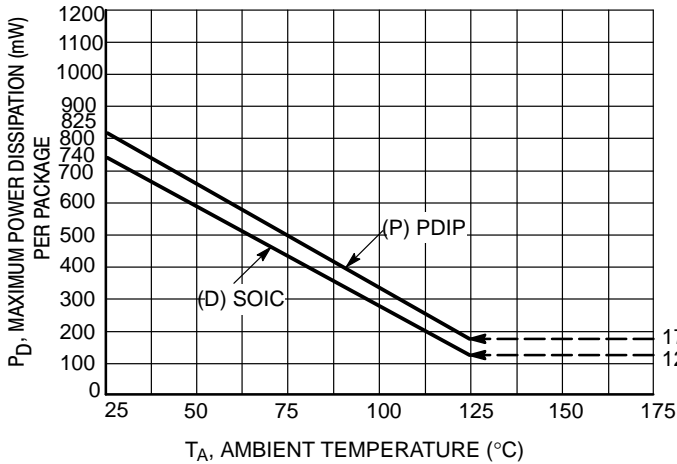


Figure 7. Ambient Temperature Power Derating

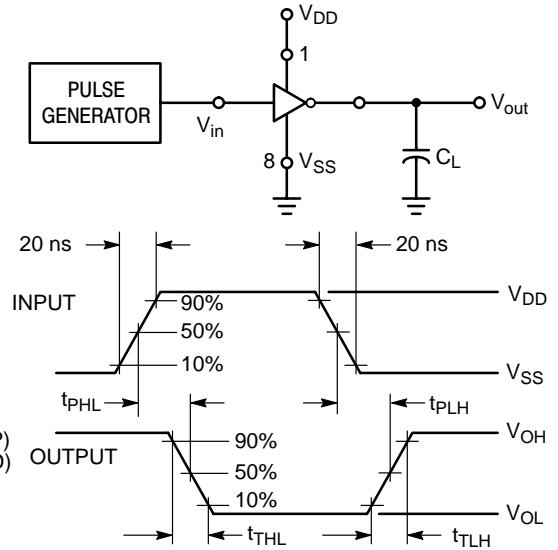
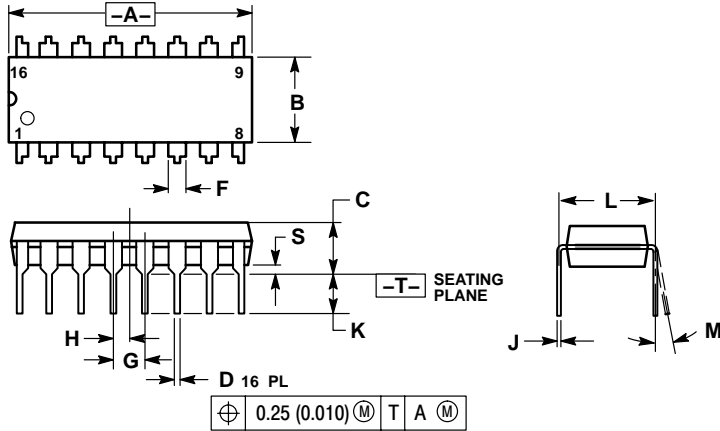


Figure 8. Switching Time Test Circuit and Waveforms

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## PACKAGE DIMENSIONS

**PDIP-16**  
**P SUFFIX**  
 PLASTIC DIP PACKAGE  
 CASE 648-08  
 ISSUE T

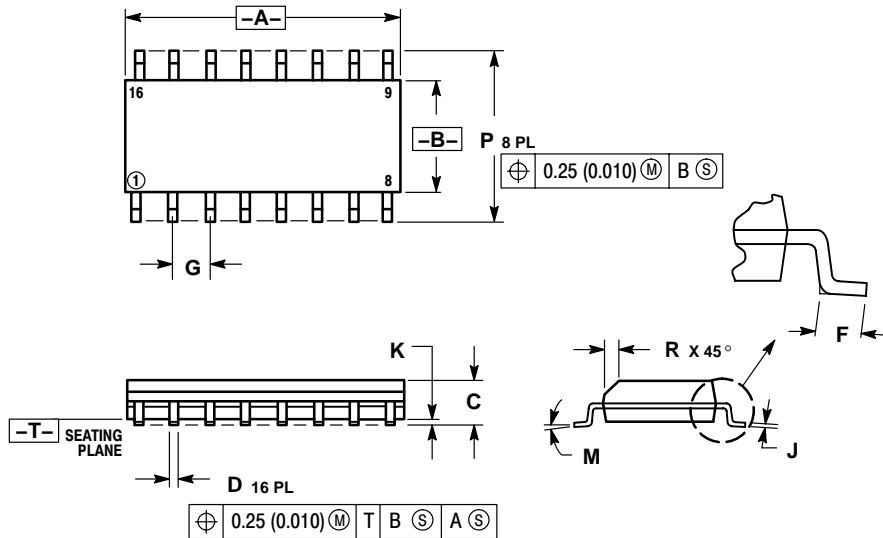


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**SOIC-16**  
**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751B-05  
 ISSUE J



**NOTES:**

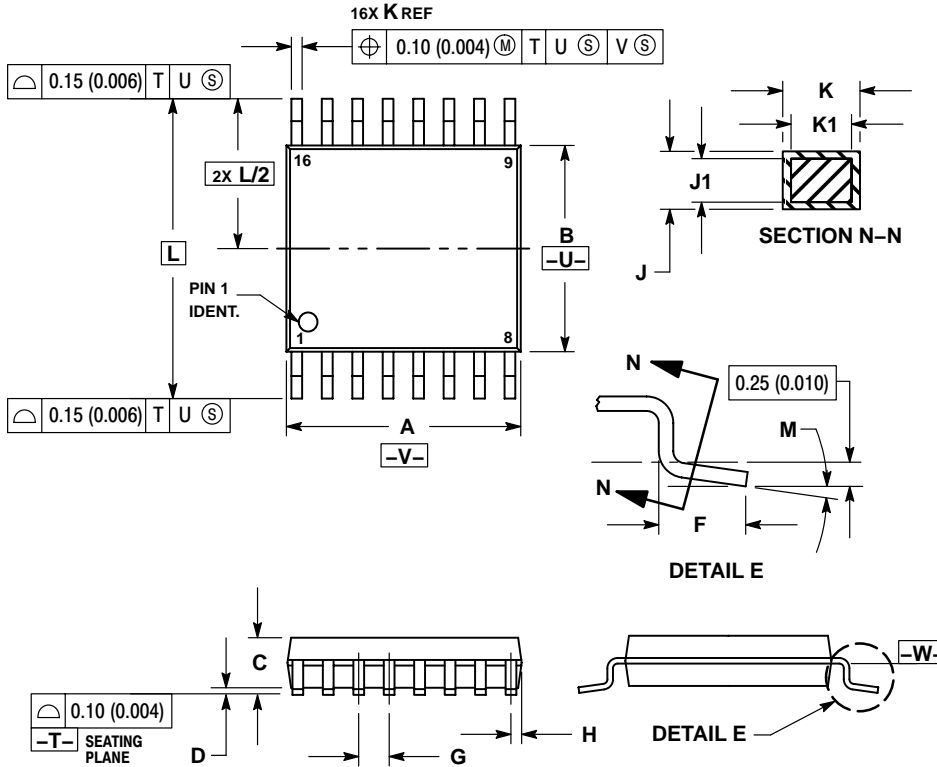
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948F-01  
ISSUE O



### NOTES:

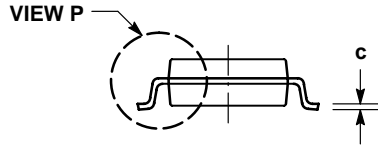
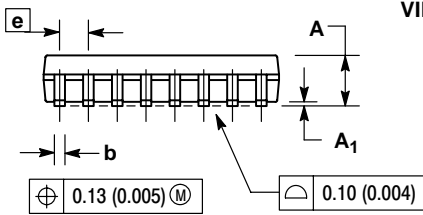
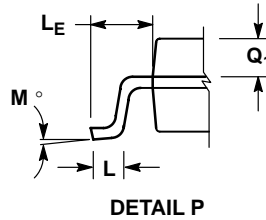
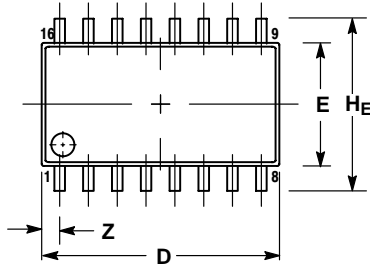
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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## PACKAGE DIMENSIONS

SOEIAJ-16  
 F SUFFIX  
 PLASTIC EIAJ SOIC PACKAGE  
 CASE 966-01  
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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