Preferred Devices

Silicon Power Transistors

The MJW21195 and MJW21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

Features

- Total Harmonic Distortion Characterized
- High DC Current Gain $-h_{FE} = 20$ Min @ $I_C = 8$ Adc
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second
- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	250	Vdc
Collector-Base Voltage	V _{CBO}	400	Vdc
Emitter-Base Voltage	V _{EBO}	5.0	Vdc
Collector-Emitter Voltage - 1.5 V	V _{CEX}	400	Vdc
Collector Current – Continuous – Peak (Note 1)	Ι _C	16 30	Adc
Base Current – Continuous	Ι _Β	5.0	Adc
Total Power Dissipation @ $T_C = 25^{\circ}C$ Derate Above $25^{\circ}C$	P _D	200 1.43	W W/∘C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	°C/W
Thermal Resistance, Junction-to-Ambient	R_{\thetaJA}	40	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

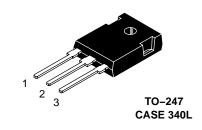
1. Pulse Test: Pulse Width = 5 μ s, Duty Cycle \leq 10%.



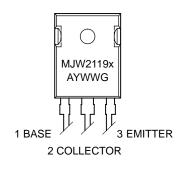
ON Semiconductor®

http://onsemi.com

16 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS, 200 WATTS



MARKING DIAGRAM



= 5 or 6

х

А

= Assembly Location

Y = Year

- WW = Work Week
- G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJW21195	TO-247	30 Units/Rail
MJW21195G	TO–247 (Pb–Free)	30 Units/Rail
MJW21196	TO-247	30 Units/Rail
MJW21196G	TO–247 (Pb–Free)	30 Units/Rail

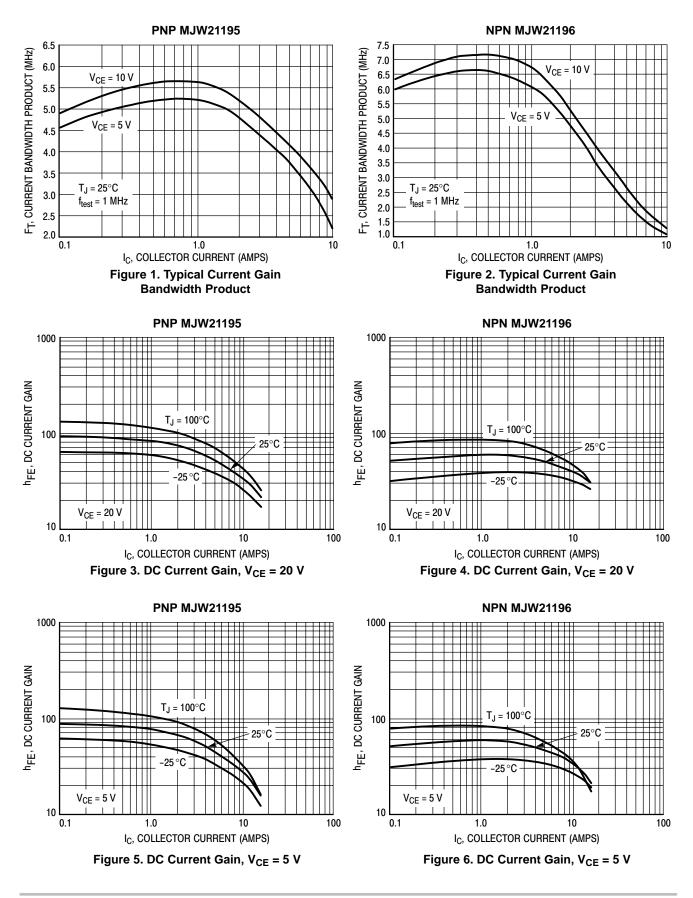
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Preferred devices are recommended choices for future use and best overall value.

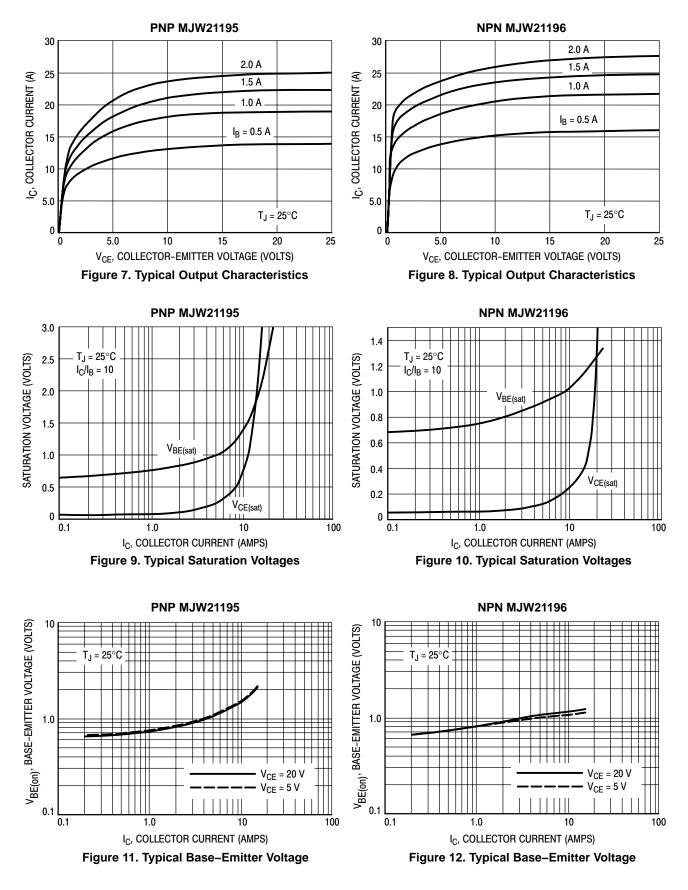
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Characteristic		Symbol	Min	Typical	Мах	Unit
OFF CHARACTERISTICS			•	· · ·		
Collector–Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}, I_B = 0$)		V _{CEO(sus)}	250	-	_	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)		I _{CEO}	-	-	100	μAdc
Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}, I_C = 0$)		I _{EBO}	-	-	50	μAdc
Collector Cutoff Current (V _{CE} = 250 Vdc, V _{BE(off)} = 1.5 Vdc)		I _{CEX}	-	-	50	μAdc
SECOND BREAKDOWN						
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50 \text{ Vdc}, t = 1 \text{ s} (\text{non-repetitive})$ ($V_{CE} = 80 \text{ Vdc}, t = 1 \text{ s} (\text{non-repetitive})$	I _{S/b}	4.0 2.25		-	Adc	
ON CHARACTERISTICS						
DC Current Gain $(I_C = 8 \text{ Adc}, V_{CE} = 5 \text{ Vdc})$ $(I_C = 16 \text{ Adc}, I_B = 5 \text{ Adc})$		h _{FE}	20 8		80 -	
Base–Emitter On Voltage ($I_C = 8 \text{ Adc}, V_{CE} = 5 \text{ Vdc}$)		V _{BE(on)}	-	-	2.0	Vdc
Collector–Emitter Saturation Voltage ($I_C = 8 \text{ Adc}, I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}, I_B = 3.2 \text{ Adc}$)	V _{CE(sat)}			1.0 3	Vdc	
DYNAMIC CHARACTERISTICS						
Total Harmonic Distortion at the Output V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS}	h _{FE} unmatched	T _{HD}	_	0.8	_	%
(Matched pair h_{FE} = 50 @ 5 A/5 V)	h _{FE} matched		_	0.08	-	
Current Gain Bandwidth Product ($I_C = 1 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f_{test} = 1 \text{ MHz}$)		f _T	4	-	_	MHz
Output Capacitance (V _{CB} = 10 Vdc, $I_E = 0$, $f_{test} = 1$ MHz)		C _{ob}	_	-	500	pF

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150^{\circ}C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

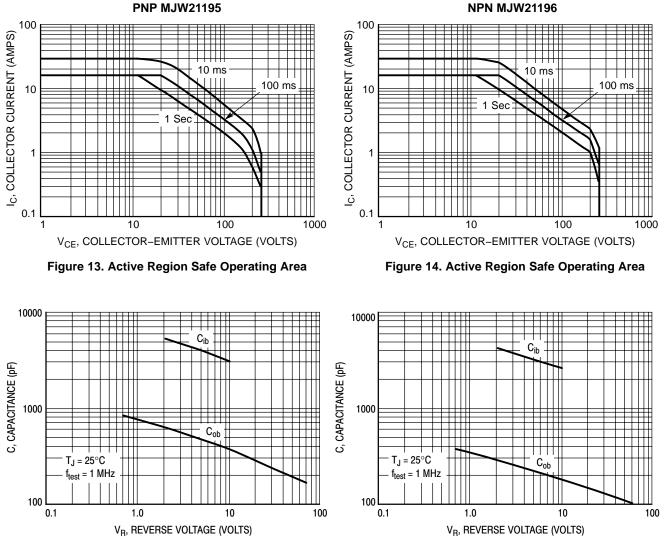


Figure 15. MJW21195 Typical Capacitance

Figure 16. MJW21196 Typical Capacitance

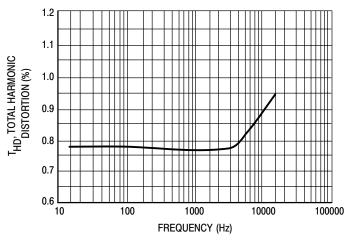


Figure 17. Typical Total Harmonic Distortion

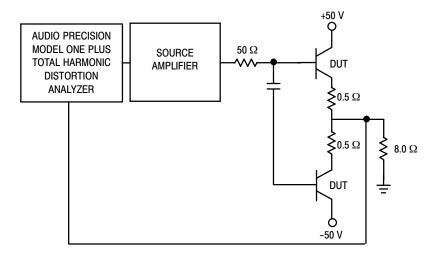
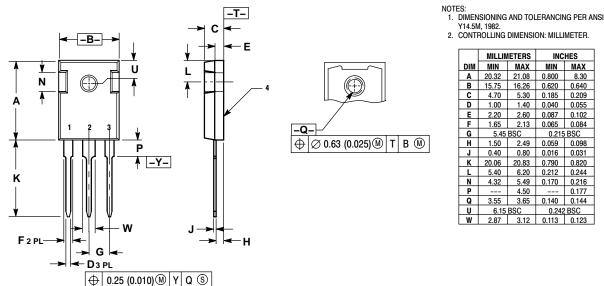


Figure 18. Total Harmonic Distortion Test Circuit

PACKAGE DIMENSIONS

TO-247 PSI CASE 340L-02 ISSUE D



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	20.32	21.08	0.800	8.30
В	15.75	16.26	0.620	0.640
С	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
Е	2.20	2.60	0.087	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
Η	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	20.06	20.83	0.790	0.820
L	5.40	6.20	0.212	0.244
Ν	4.32	5.49	0.170	0.216
Ρ		4.50		0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

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