NCP1397A, NCP1397B

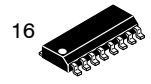
High Performance Resonant Mode Controller with Integrated High-Voltage Drivers

ON Semiconductor®

http://onsemi.com

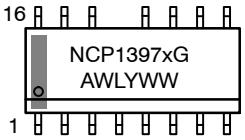
The NCP1397 is a high performance controller that can be utilized in half bridge resonant topologies such as series resonant, parallel resonant and LLC resonant converters. It integrates 600 V gate drivers, simplifying layout and reducing external component count. With its unique architecture, including a 500 kHz Voltage Controlled Oscillator whose control mode permits flexibility when an ORing function is required, the NCP1397 delivers everything needed to build a reliable and rugged resonant mode power supply.

The NCP1397 provides a suite of protection features with configurable settings to optimize any application. These include: auto−recovery or fault latch−off, brown−out, open optocoupler, soft−start and short−circuit protection. Deadtime is also adjustable to overcome shoot through current.



SO−16, LESS PIN 13
D SUFFIX
CASE 751AM

MARKING DIAGRAMS

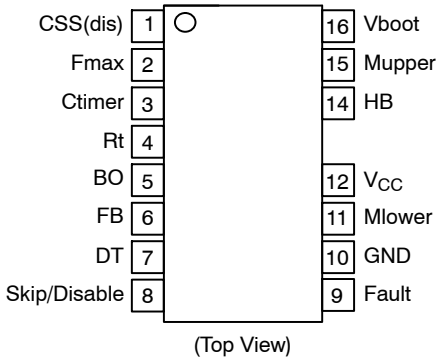


x	= A or B
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

Features

- High−Frequency Operation from 50 kHz up to 500 kHz
- 600 V High−Voltage Floating Driver
- Adjustable Minimum Switching Frequency with ±3% Accuracy
- Adjustable Deadtime from 100 ns to 2 μs.
- Startup Sequence Via an Externally Adjustable Soft−Start
- Brown−Out Protection for a Simpler PFC Association
- Latched Input for Severe Fault Conditions, e.g. Over Temperature or OVP
- Timer−Based Input with Auto−Recovery Operation for Delayed Event Reaction
- Latched Overcurrent Protection
- Disable Input for Immediate Event Reaction or Simple ON/OFF Control
- V_{CC} Operation up to 20 V
- Low Startup Current of 300 μA
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Common Collector Optocoupler Connection for Easier ORing
- Optional Common Emitter Optocoupler Connection
- Internal Temperature Shutdown
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 26 of this data sheet.

Typical Applications

- Flat Panel Display Power Converters
- High Power ac−dc Adapters for Notebooks
- Computing Power Supplies
- Industrial and Medical Power Sources
- Offline Battery Chargers

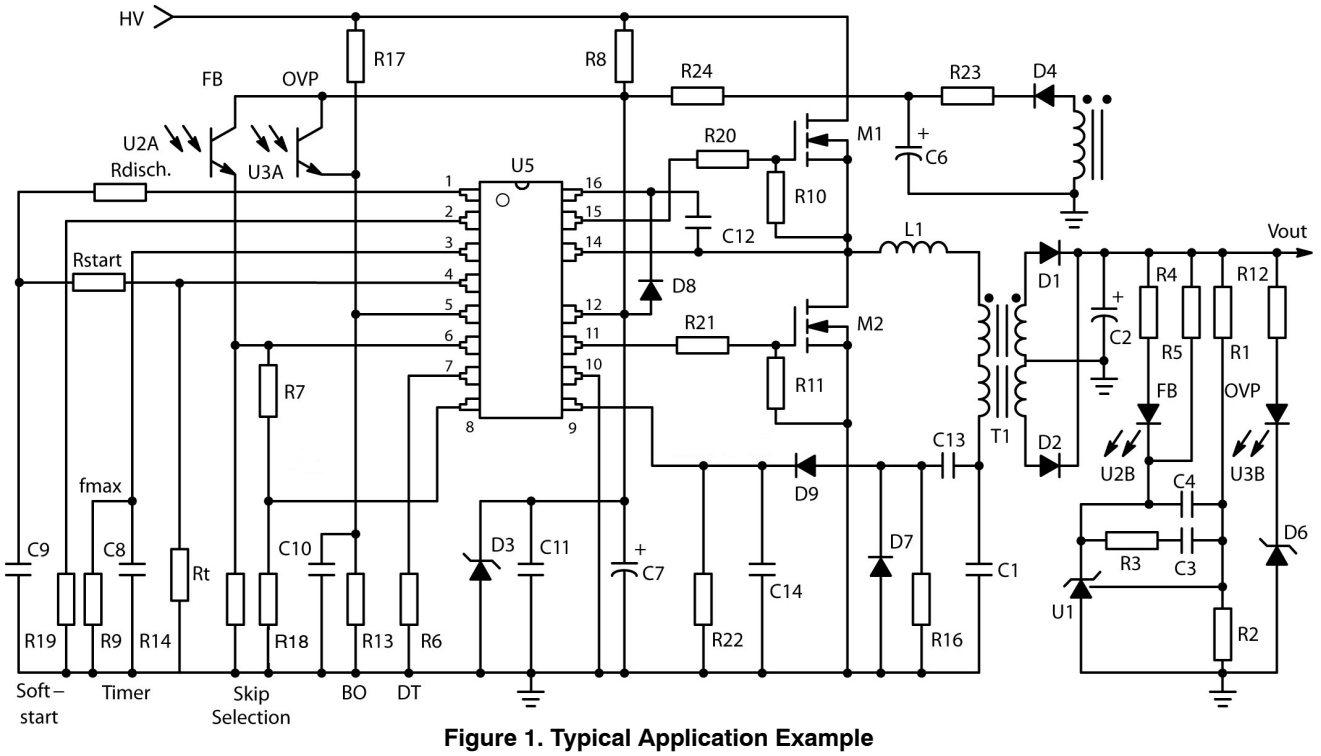


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	CSS(dis)	Soft−Start Discharge	Soft−start capacitor discharge pin. Connect to the soft−start capacitor to reset it before startup or during overload conditions.
2	Fmax	Maximum frequency clamp	A resistor sets the maximum frequency excursion
3	Ctimer	Timer duration	Sets the timer duration in presence of a fault
4	Rt	Minimum frequency clamp	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for V_{FB} = 1 V.
5	BO	Brown−Out	Detects low input voltage conditions. When brought above V_{latch} (4 V typically), it fully latches off the controller.
6	FB	Feedback	Injecting current into this pin increases the oscillation frequency up to Fmax.
7	DT	Deadtime	A simple resistor adjusts the dead−time width
8	Skip/Disable	Skip or Disable input	Upon release, a clean startup sequence occurs if V_{FB} < 0.3 V. During the skip mode, when FB doesn't drop below 0.3 V, the IC restarts without soft−start sequence.
9	Fault	Fault detection input	When asserted, the external timer starts to countdown and shuts down the controller at the end of its time duration. Simultaneously the Soft−Start discharge switch is activated so the converter operating frequency goes up to protect application power stage. This input features also second fault comparator with higher threshold (1.5 V typically) that: A) Speeds up the timer capacitor charging current 8 times − NCP1397A B) latches off the IC permanently − NCP1397B In both versions the second fault comparator helps to protect application in case of short circuit on the output or transformer secondary winding.
10	GND	Analog ground	−
11	Mlower	Low side output	Drives the lower side MOSFET
12	V_{CC}	Supplies the controller	The controller accepts up to 20 V
13	NC	Not connected	Increases the creepage distance
14	HB	Half−bridge connection	Connects to the half−bridge output
15	Mupper	High side output	Drives the higher side MOSFET
16	Vboot	Bootstrap pin	The floating V_{CC} supply for the upper stage

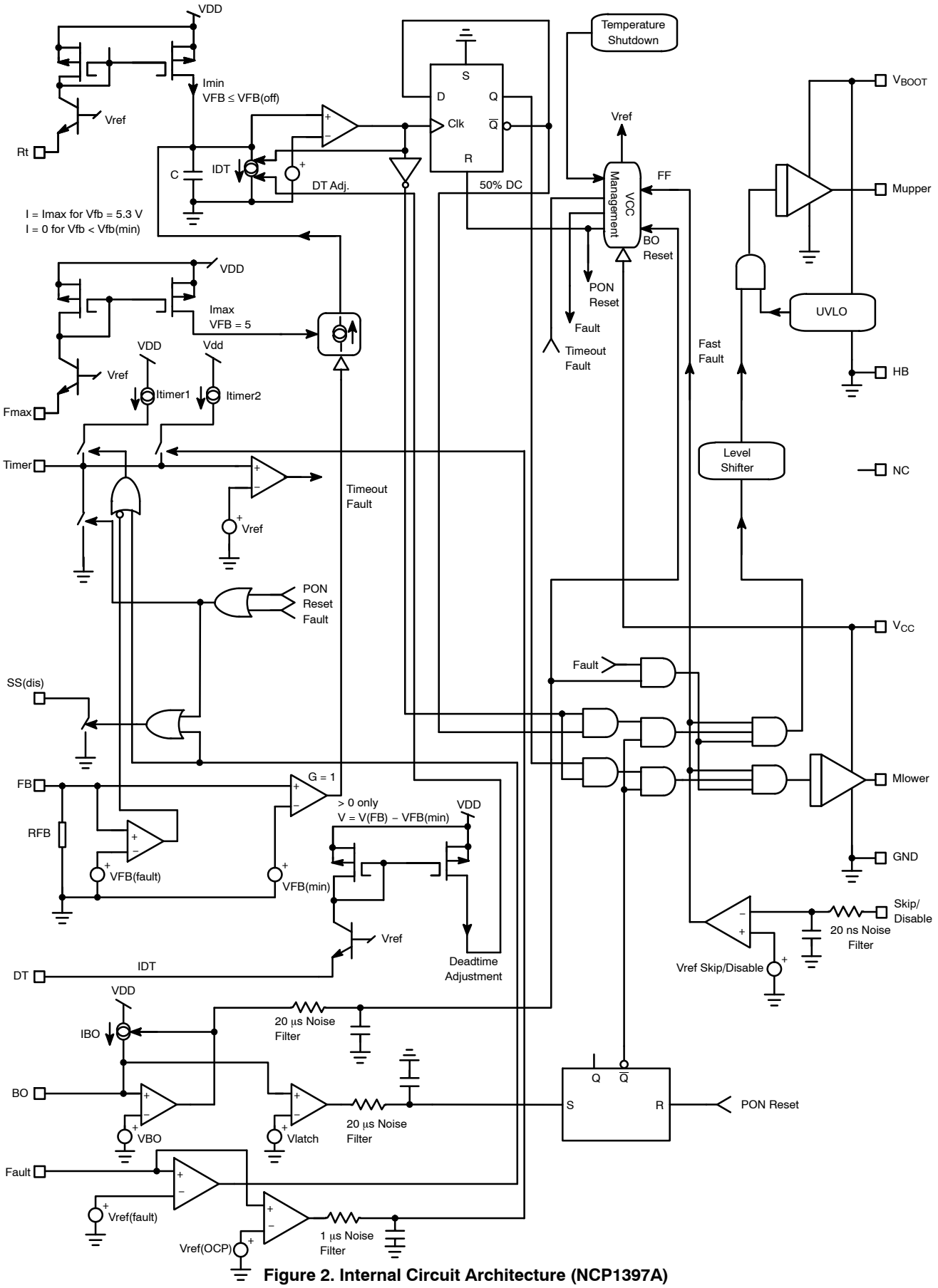


Figure 2. Internal Circuit Architecture (NCP1397A)

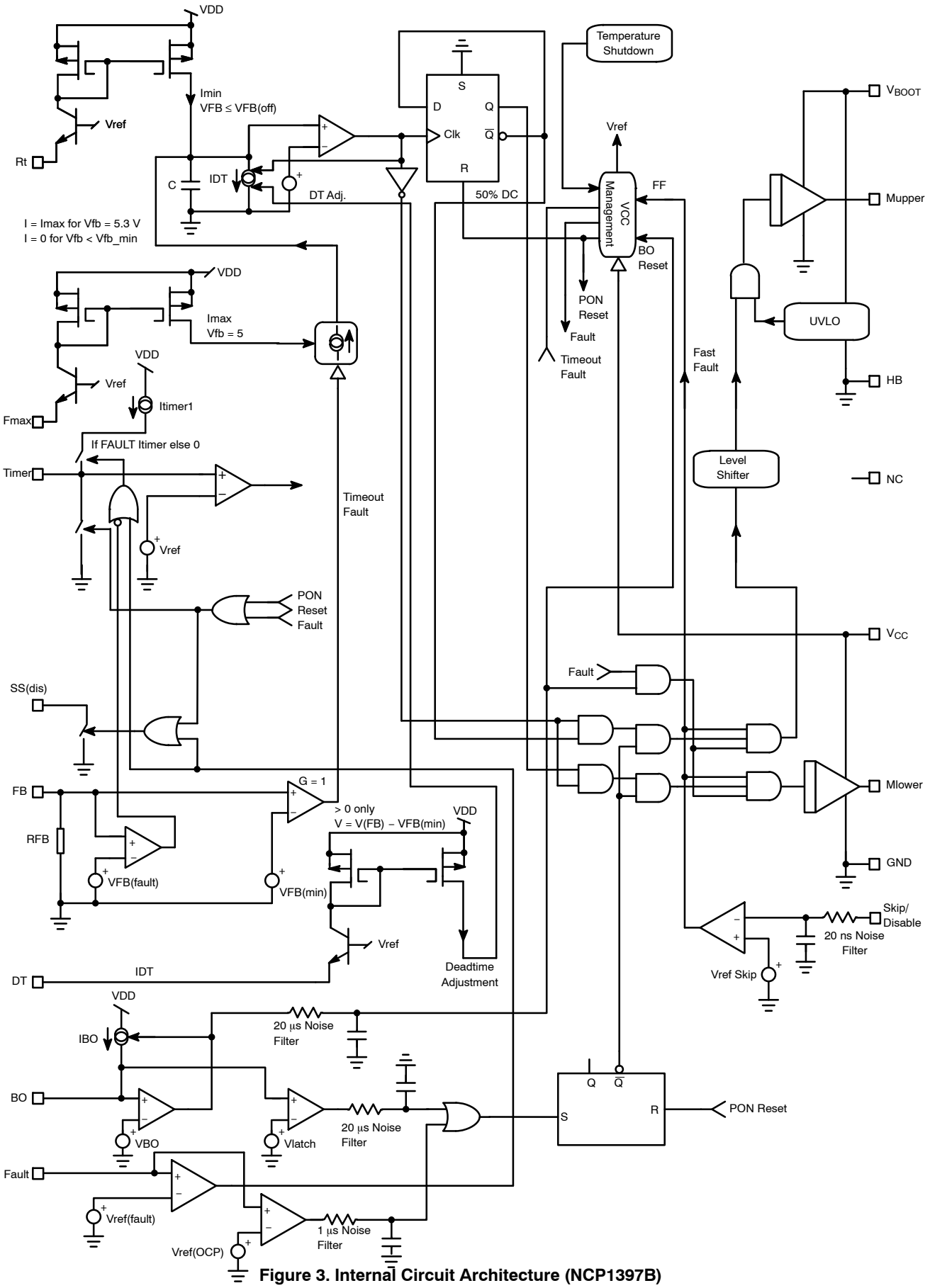


Figure 3. Internal Circuit Architecture (NCP1397B)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage bridge pin, pin 14	V_{BRIDGE}	−1 to 600	V
Floating supply voltage, ground referenced	V_{BOOT} − V_{BRIDGE}	0 to 20	V
High side output voltage	$V_{DRV(HI)}$	V_{BRIDGE}−0.3 to V_{BOOT}+0.3	V
Low side output voltage	$V_{DRV(LO)}$	−0.3 to V_{CC}+0.3	V
Allowable output slew rate	dV_{BRIDGE}/dt	50	V/ns
Power Supply voltage, pin 12	V_{CC}	20	V
Maximum voltage, all pins (except pin 11 and 10)	–	−0.3 to 10	V
Thermal Resistance Junction−to−Air, PDIP version	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction−to−Air, SOIC version	$R_{\theta JA}$	130	°C/W
Storage Temperature Range	–	−60 to +150	°C
ESD Capability, Human Body Model (HBM) (All pins except HV pins)	–	2	kV
ESD Capability, Machine Model (MM)	–	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model 200 V per JEDEC Standard JESD22−A115−A
2. This device meets latchup tests defined by JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
$V_{CC(on)}$	Turn−on threshold level, V_{CC} going up	12	9.7	10.5	11.3	V
$V_{CC(min)}$	Minimum operating voltage after turn−on	12	8.7	9.5	10.3	V
$V_{boot(on)}$	Startup voltage on the floating section	16−14	8	9	10	V
$V_{boot(min)}$	Cutoff voltage on the floating section	16−14	7.4	8.4	9.4	V
$I_{startup}$	Startup current, $V_{CC} < V_{CC(on)}$	12	–	–	300	μA
$V_{CC(reset)}$	V_{CC} level at which the internal logic gets reset	12	–	6.6	–	V
I_{CC1}	Internal IC consumption, no output load on pin 15/14 – 11/10, F_{SW} = 300 kHz	12	–	4	–	mA
I_{CC2}	Internal IC consumption, 1 nF output load on pin 15/14 – 11/10, F_{SW} = 300 kHz	12	–	11	–	mA
I_{CC3}	Consumption in fault or disable mode (All drivers disabled, Rt = 34 kΩ, R_{DT} = 10 kΩ)	12	–	1.5	–	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
$F_{SW(min)}$	Minimum switching frequency, Rt = 34 kΩ on pin 4, V_{pin6} = 0.8 V, DT = 300 ns	4	58.2	60	61.8	kHz
$F_{SW(max)}$	Maximum switching frequency, $R_{f(max)}$ = 1.9 kΩ on pin 2, V_{pin6} > 5.3 V, Rt = 34 kΩ, DT = 300 ns	2	440	500	560	kHz
FB_{SW}	Feedback pin swing above which Δf = 0	6	–	5.3	–	V
DC	Operating duty−cycle symmetry	11−15	48	50	52	%
T_{del1}	Delay before driver restart from fault or disable mode	–	–	700	–	ns
T_{del2}	Delay before driver restart after $V_{CC(on)}$ event (Note 4)	–	–	11	–	μs
$V_{ref(Rt)}$	Reference voltage for Rt pin	4	2.18	2.3	2.42	V
FEEDBACK SECTION						
R_{FB}	Internal pulldown resistor	6	–	20	–	kΩ
$V_{FB(min)}$	Voltage on pin 6 below which the FB level has no VCO action	6	–	1.1	–	V
$V_{FB(off)}$	Voltage on pin 6 below which the controller considers the FB fault	6	240	280	320	mV
$V_{FBoff(hyste)}$	Feedback fault comparator hysteresis	6	–	45	–	mV
DRIVE OUTPUT						
T_r	Output voltage risetime @ C_L = 1 nF, 10−90% of output signal	15−14/11−10	–	40	–	ns
T_f	Output voltage falltime @ C_L = 1 nF, 10−90% of output signal	15−14/11−10	–	20	–	ns
R_{OH}	Source resistance	15−14/11−10	–	13	–	Ω
R_{OL}	Sink resistance	15−14/11−10	–	5.5	–	Ω
T_{dead}	Deadtime with R_{DT} = 10 kΩ from pin 7 to GND	7	250	290	340	ns
$T_{dead(max)}$	Maximum deadtime with R_{DT} = 82 kΩ from pin 7 to GND	7	–	2	–	μs
$T_{dead(min)}$	Minimum deadtime, R_{DT} = 3 kΩ from pin 7 to GND	7	–	100	–	ns
$I_{HV(LEAK)}$	Leakage current on high voltage pins to GND	14, 15,16	–	–	5	μA
TIMERS						
I_{timer1}	Timer capacitor charge current during feedback fault or when $V_{ref(fault)} < V_{pin9} < V_{ref(OCP)}$	3	150	175	190	μA

3. The IC does not activate soft−start (unless the feedback pin voltage is below 0.3 V) when the skip/disable input is released, this is for skip cycle implementation.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
TIMERS						
I_{timer2}	Timer capacitor charge current when $V_{pin9} > V_{ref(OCP)}$ ($I_{charge1}$ + $I_{charge2}$) − A version only	3	1.1	1.3	1.5	mA
T_{timer}	Timer duration with a 1 μF capacitor and a 1 MΩ resistor, I_{timer1} current applied	3	–	24	–	ms
T_{timerR}	Timer recurrence in permanent fault, same values as above	3	–	1.4	–	s
$V_{timer(on)}$	Voltage at which pin 3 stops output pulses	3	3.8	4	4.2	V
$V_{timer(off)}$	Voltage at which pin 3 restarts output pulses	3	0.95	1	1.05	V
$R_{SS(dis)}$	Soft−start discharge switch channel resistance	1	–	100	–	Ω
PROTECTION						
$V_{ref(Skip)}$	Reference voltage for Skip/Disable input (Note 4)	8	630	660	690	mV
$Hyste_{(Skip)}$	Hysteresis for Skip/Disable (Note 4)	8	–	45	–	mV
$V_{ref(Fault)}$	Reference voltage for Fault comparator	9	0.99	1.04	1.09	V
$Hyste_{(Fault)}$	Hysteresis for fault comparator input	9	–	60	–	mV
$V_{ref(OCP)}$	Reference voltage for OCP comparator	9	1.47	1.55	1.63	V
$Hyste_{(OCP)}$	Hysteresis for OCP comparator input	9	–	90	–	mV
$T_{p(Disable)}$	Propagation delay from disable input to the drive shutdown	8	–	60	100	ns
$IBO_{(bias)}$	Brown−Out input bias current	5	–	0.02	–	μA
VBO	Brown−Out level	5	0.99	1.04	1.09	V
IBO	Hysteresis current, V_{pin5} > VBO	5	25	28	31	μA
VI_{atch}	Latching voltage	5	3.7	4	4.3	V
T_{SD}	Temperature shutdown	–	140	–	–	°C
$T_{SD(hyste)}$	Hysteresis	–	–	30	–	°C

3. The IC does not activate soft−start (unless the feedback pin voltage is below 0.3 V) when the skip/disable input is released, this is for skip cycle implementation.
4. Guaranteed by design.

TYPICAL CHARACTERISTICS

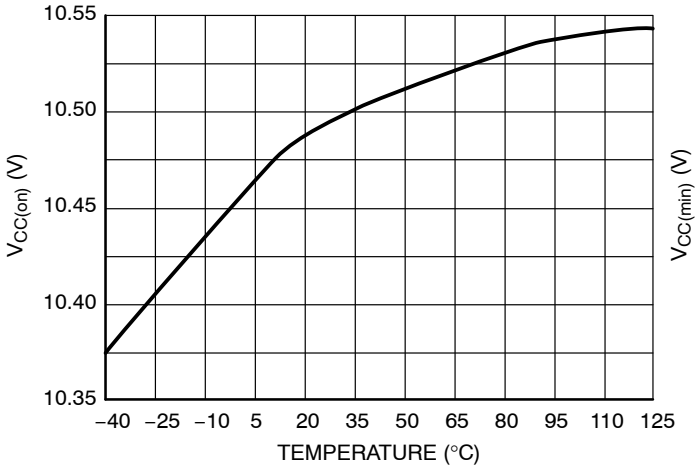


Figure 4. $V_{CC(on)}$ Threshold

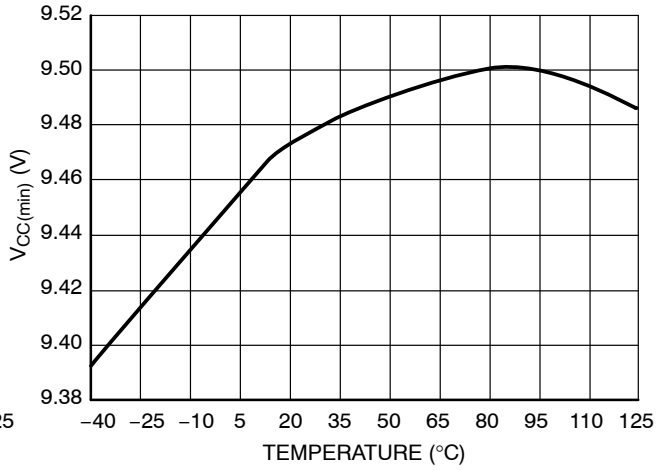


Figure 5. $V_{CC(min)}$ Threshold

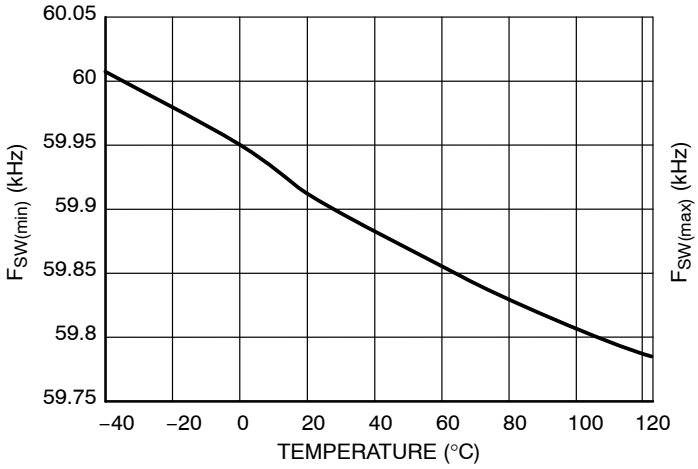


Figure 6. $F_{SW(min)}$ Frequency Clamp

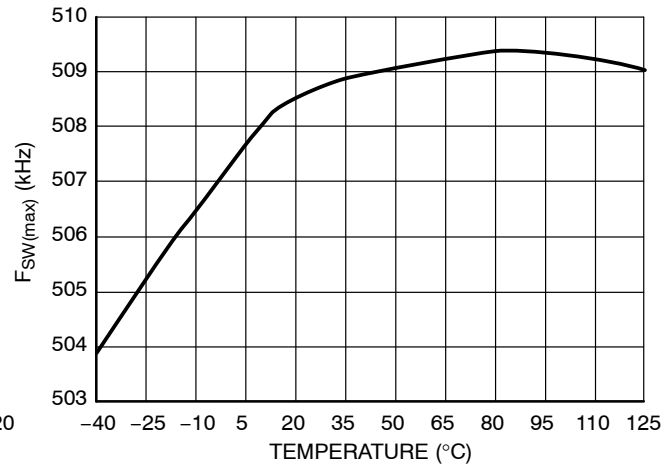


Figure 7. $F_{SW(max)}$ Frequency Clamp

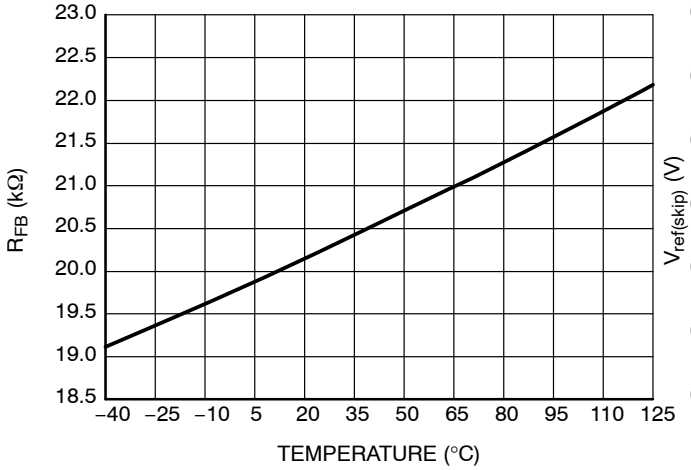


Figure 8. Pulldown Resistor (R_{FB})

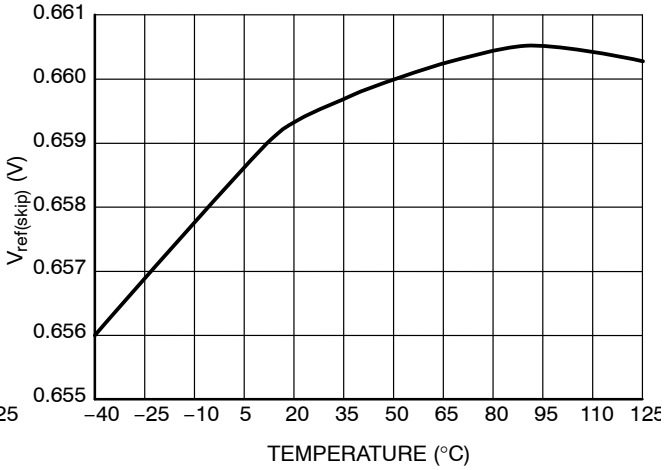


Figure 9. Skip/Disable Threshold ($V_{ref(skip)}$)

TYPICAL CHARACTERISTICS

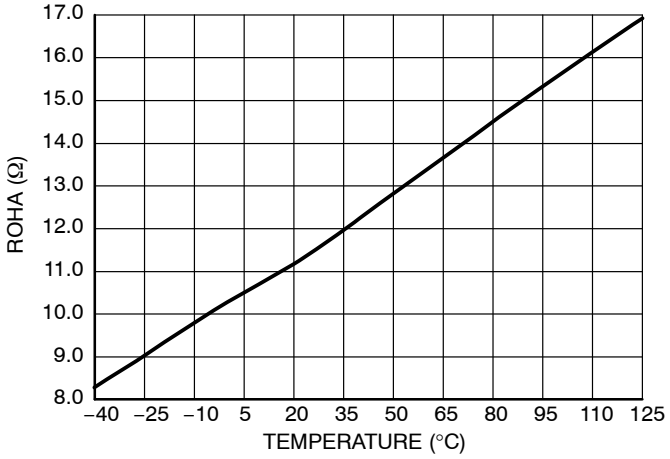


Figure 10. Source Resistance (ROH)

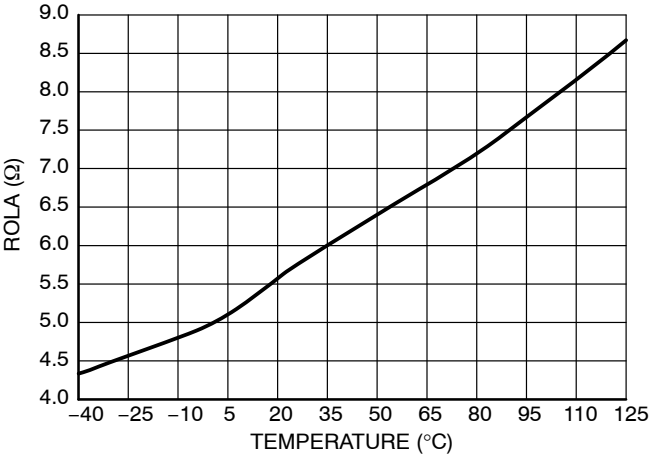


Figure 11. Sink Resistance (ROL)

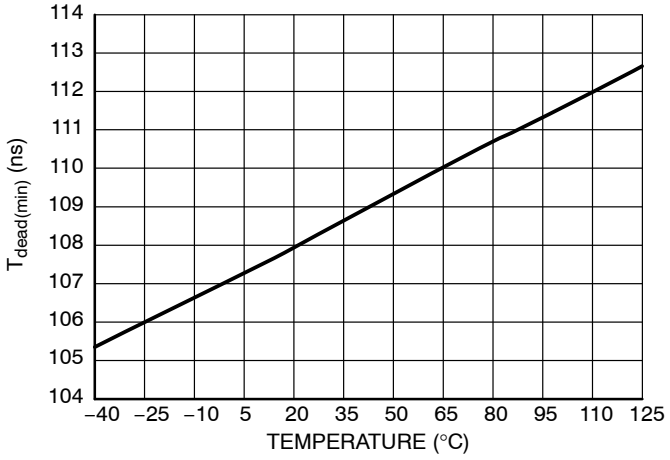


Figure 12. $T_{dead(min)}$

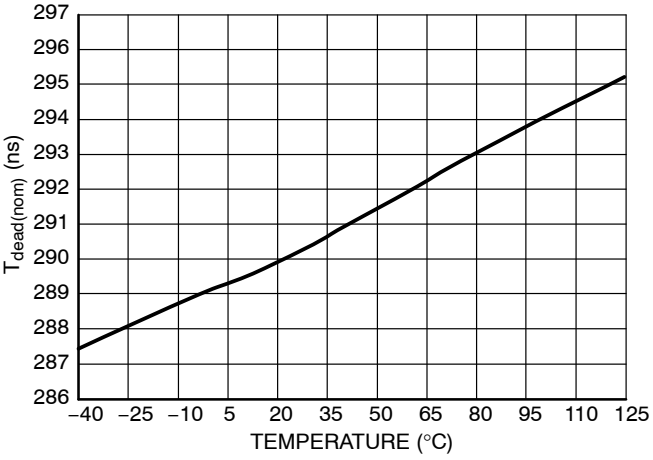


Figure 13. $T_{dead(nom)}$

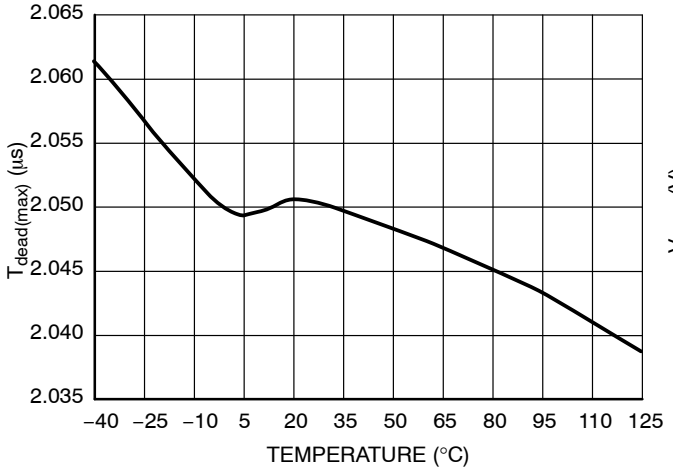


Figure 14. $T_{dead(max)}$

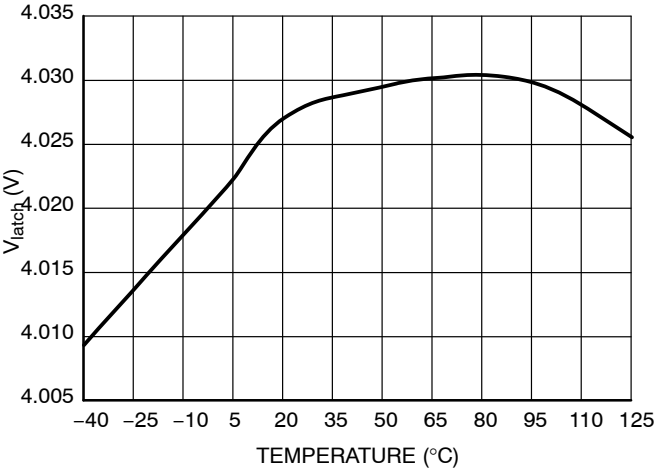


Figure 15. Latch Level (V_{latch})

TYPICAL CHARACTERISTICS

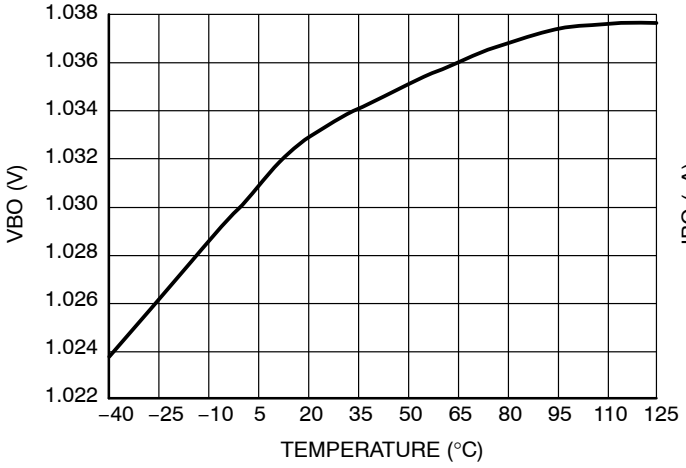


Figure 16. Brown−Out Reference (VBO)

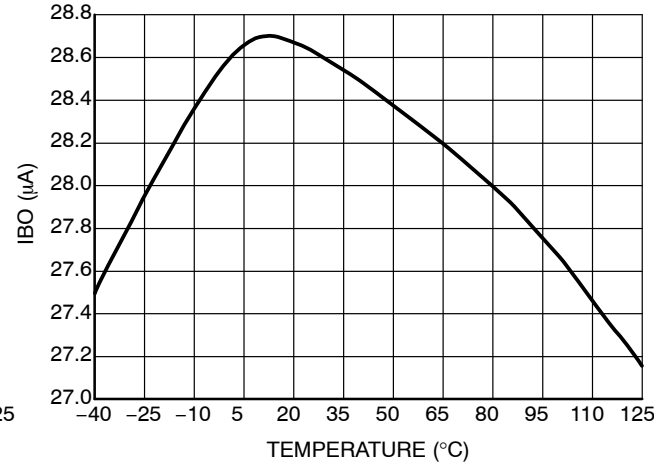


Figure 17. Brown−Out Hysteresis Current (IBO)

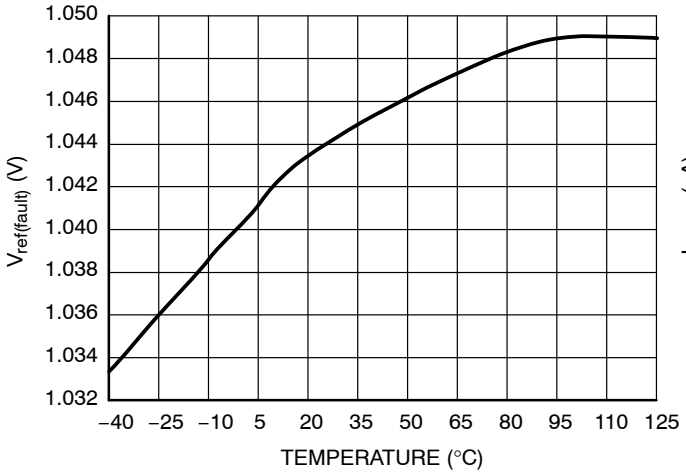


Figure 18. Fault Input Reference ($V_{ref(fault)}$)

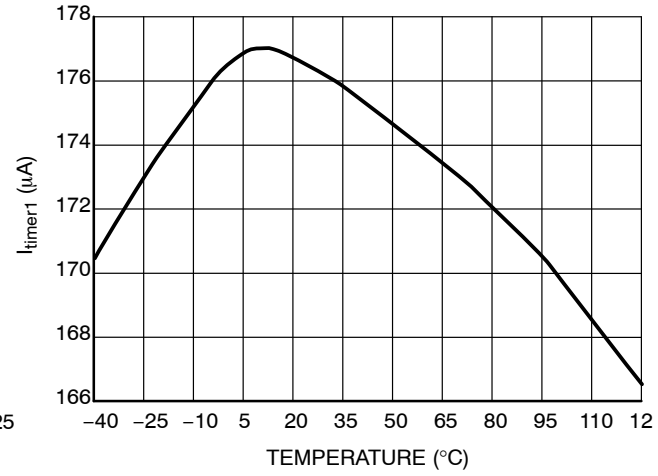


Figure 19. C_{timer} 1st Current (I_{timer1})

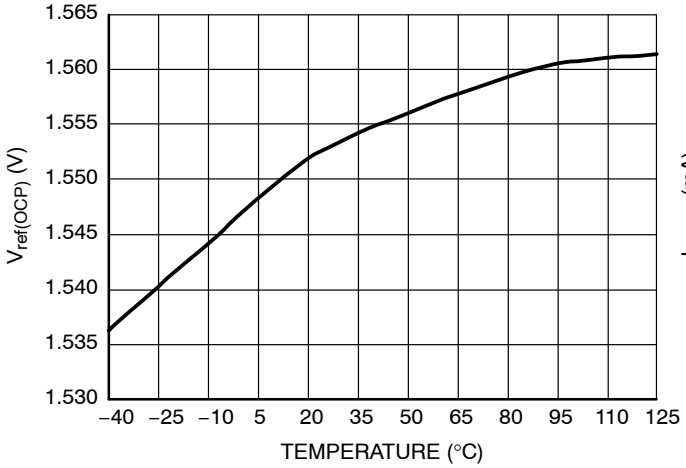


Figure 20. OCP reference ($V_{ref(OCP)}$)

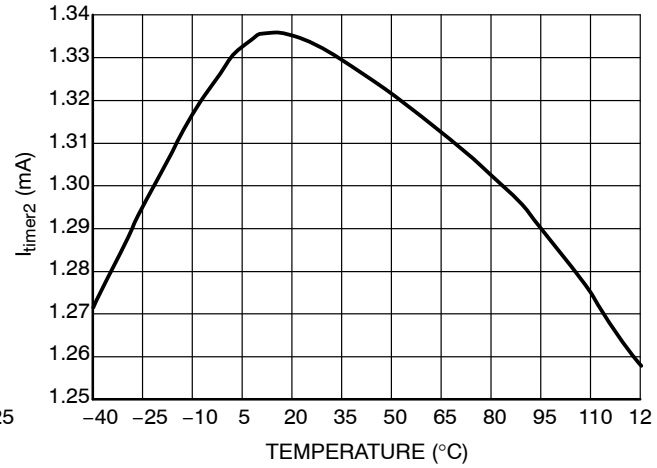


Figure 21. C_{timer} 2nd Current (I_{timer2})

TYPICAL CHARACTERISTICS

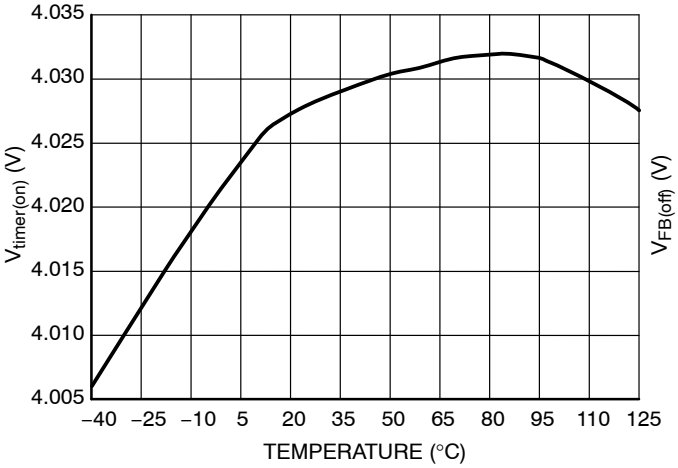


Figure 22. Fault Timer Ending Voltage ($V_{timer(on)}$)

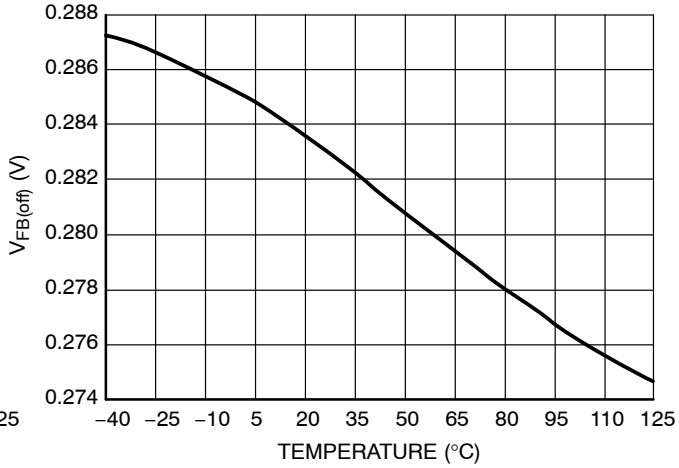


Figure 23. FB Fault Detection Threshold ($V_{FB(fault)}$)

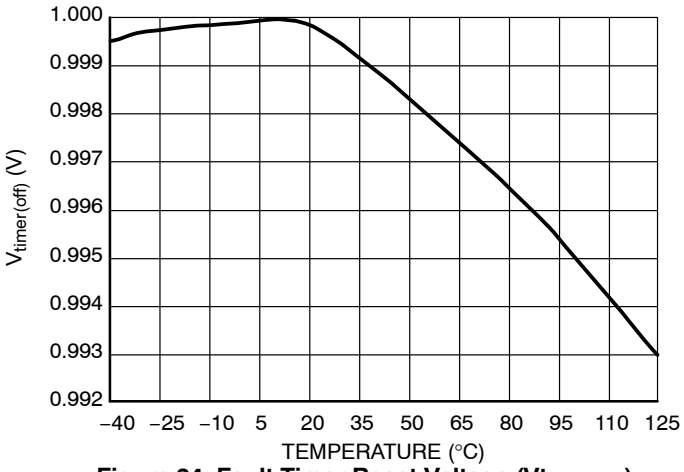


Figure 24. Fault Timer Reset Voltage ($Vt_{imer(off)}$)

APPLICATION INFORMATION

The NCP1397A/B includes all necessary features to help building a rugged and safe switch−mode power supply featuring an extremely low standby power. The below bullets detail the benefits brought by implementing the NCP1397A/B controller:

- **Wide frequency range**: A high−speed Voltage Control Oscillator allows an output frequency excursion from 50 kHz up to 500 kHz on M_{lower} and M_{upper} outputs.
- **Adjustable dead−time**: Due to a single resistor wired to ground, the user has the ability to include some dead−time, helping to fight cross−conduction between the upper and the lower transistor.
- **Adjustable soft−start**: Every time the controller starts to operate (power on), the switching frequency is pushed to the programmed starting value by external components (R_{Fmin}//R_{Fstart}) and slowly moves down toward the minimum frequency, until the feedback loop closes. The soft−start discharge input (SS(dis)) discharges the Soft−Start capacitor before any IC restart excluding the restart after Disable is released AND FB voltage is higher than 0.3 V. The Soft−Start discharge switch also activates in case the Fault input detects the overload conditions.
- **Adjustable minimum and maximum frequency excursion**: In resonant applications, it is important to stay away from the resonating peak to keep operating the converter in the right region. Thanks to a single external resistor, the designer can program its lowest frequency point, obtained in lack of feedback voltage (during the startup sequence or in short−circuit conditions). Internally trimmed capacitors offer a $\pm 3\%$ precision on the selection of the minimum switching frequency. The adjustable upper stop being less precise to $\pm 12\%$.
- **Low startup current**: When directly powered from the high−voltage DC rail, the device only requires 300 μA to startup.
- **Brown−Out detection**: To avoid operation from a low input voltage, it is interesting to prevent the controller from switching if the high−voltage rail is not within the right boundaries. Also, when teamed with a PFC front−end circuitry, the brown−out detection can ensure a clean startup sequence with soft−start, ensuring that the PFC is stabilized before energizing the resonant tank. The BO input features a 28 μA hysteresis current for the lowest consumption.
- **Adjustable fault timer duration**: When a fault is detected on the Fault input or when the FB path is broken, timer pin starts to charge an external capacitor. If the fault is removed, the timer opens the charging path and nothing happens. When the timer reaches its selected duration (via a capacitor on Pin 3), all pulses are stopped. The controller now waits for the discharge via an external resistor on Pin 3 to issue a new clean startup sequence via soft−start.
- **Cumulative fault events**: In the NCP1397A/B, the timer capacitor is not reset when the fault disappears. It actually integrates the information and cumulates the occurrences. A resistor placed in parallel with the capacitor will offer a simple way to adjust the discharge rate and thus the auto−recovery retry rate.
- **Overcurrent detection using Fault input**: The fault input is specifically designed to protect LLC application in case of short circuit or overload. In case the voltage on this input grows above first threshold the I_{timer} current source is activated and Fault timer capacitor starts charging. Simultaneously the Soft−Start discharge switch is activated to increase operating frequency of the converter. The IC stops operation in case the Fault timer elapses. The Fault input includes also second fault comparator that:
  - Speeds up the fault timer capacitor charging by increasing the I_{timer1} current to I_{timer2} – **NCP1397A**
  - Latches off the device – **NCP1397B**

The second fault comparator thus helps to protect the power stage in case of hard short circuit (like shorted transformer winding etc.)

- **Skip cycle possibility**: The absence of the soft−start on the Skip/Disable input (in case the $V_{FB} > 0.3$ V) offers an easy way to implement skip cycle when power saving features are necessary. A simple resistive divider from the feedback pin to the Skip/Disable input, and skip can be implemented.
- **Broken feedback loop detection**: Upon startup or any time during operation, if the FB signal is missing, the timer starts to charge timer capacitor. If the loop is really broken, the FB level does not grow−up before the timer ends charging. The controller then stops all pulses and waits until the timer pin voltage collapses to 1 V typically before a new attempt to restart, via the soft−start. If the optocoupler is permanently broken, a hiccup takes place.
- **Common collector or common emitter optocoupler connection options**: This IC allows the designer to select from two possible optocoupler configurations.

Voltage−Controlled Oscillator

The VCO section features a high−speed circuitry allowing operation from 100 kHz up to 1 MHz. However, as a division by two internally creates the two Q and /Q outputs, the final effective signal on output M_{lower} and M_{upper} switches between 50 kHz and 500 kHz. The VCO is configured in such a way that if the feedback pin voltage goes up, the switching frequency also goes up. Figure 25 shows the architecture of the VCO oscillator.

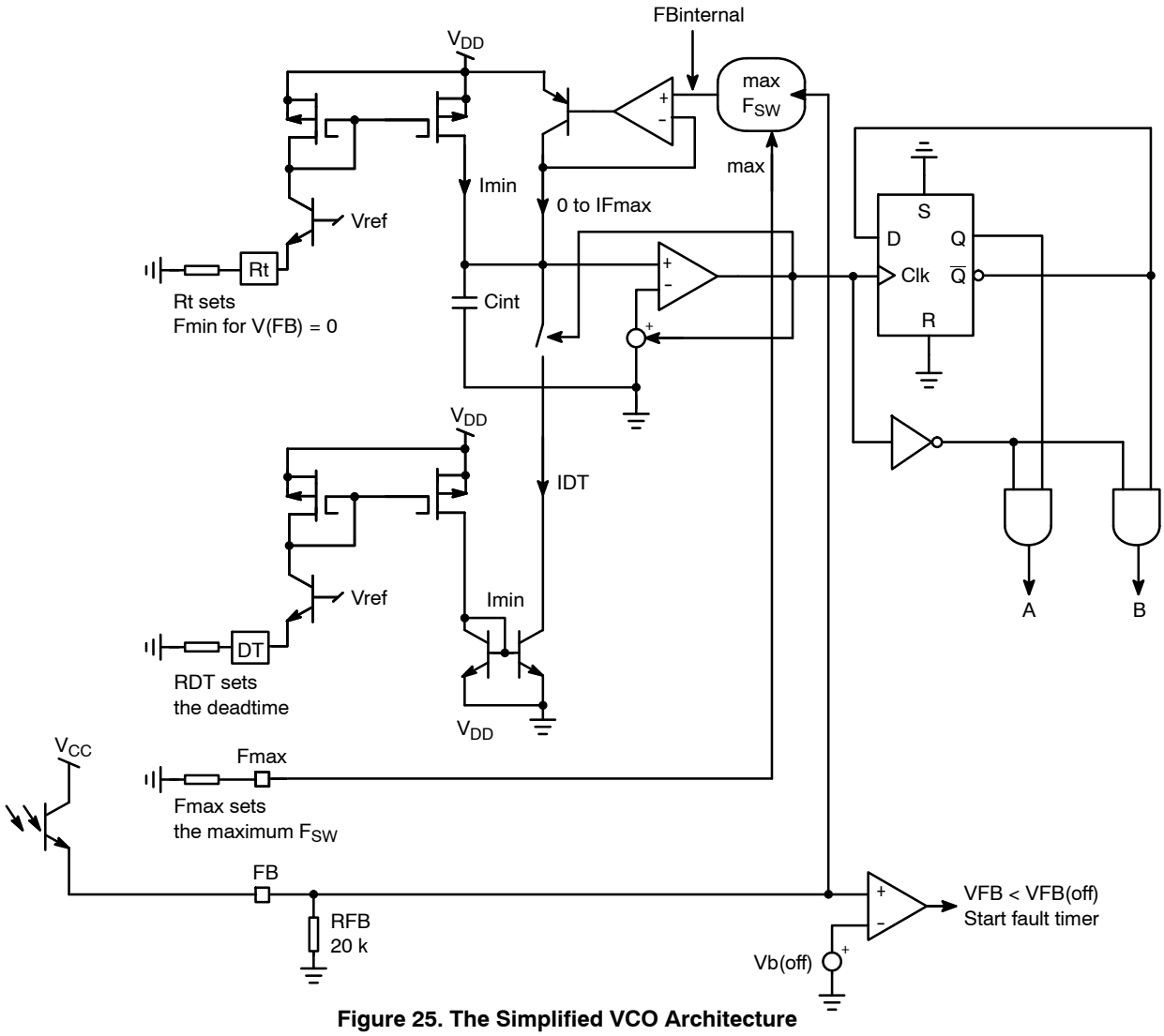


Figure 25. The Simplified VCO Architecture

The designer needs to program the maximum switching frequency and the minimum switching frequency. In LLC configurations, for circuits working above the resonant frequency, a high precision is required on the minimum frequency, hence the ±3% specification. This minimum switching frequency is actually reached when no feedback closes the loop. It can happen during the startup sequence, a strong output transient loading or in a short−circuit condition. By installing a resistor from Pin 4 to GND, the minimum frequency is set. Using the same philosophy, wiring a resistor from Pin 2 to GND will set the maximum frequency excursion. To improve the circuit protection features, we have purposely created a dead zone, where the feedback loop has no action. This is typically below 1.1 V. Figure 26 details the arrangement where the internal voltage (that drives the VCO) varies between 0 and 2.3 V. However, to create this swing, the feedback pin (to which the optocoupler emitter connects), will need to swing typically between 1.1 V and 5.3 V.

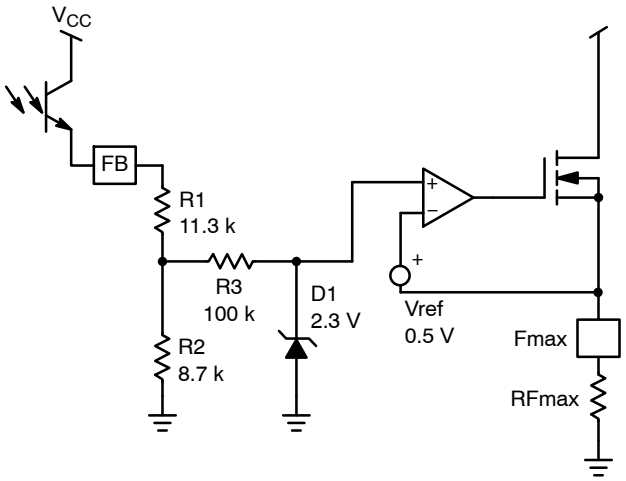


Figure 26. The OPAMP Arrangement Limits the VCO Modulation Signal between 0.5 and 2.3 V

This techniques allows us to detect a fault on the converter in case the FB pin cannot rise above 0.3 V (to actually close the loop) in less than a duration imposed by the programmable timer. Please refer to the fault section for detailed operation of this mode.

As shown on Figure 26, the internal dynamics of the VCO control voltage will be constrained between 0.5 V and 2.3 V, whereas the feedback loop will drive Pin 6 (FB) between 1.1 V and 5.3 V. If we take the default FB pin excursion numbers, 1.1 V = 50 kHz, 5.3 V = 500 kHz, then the VCO maximum slope will be:

$$\frac{500k - 50k}{4.2} = 107\ kHz/V$$

Figures 27 and 28 portray the frequency evolution depending on the feedback pin voltage level in a different frequency clamp combination.

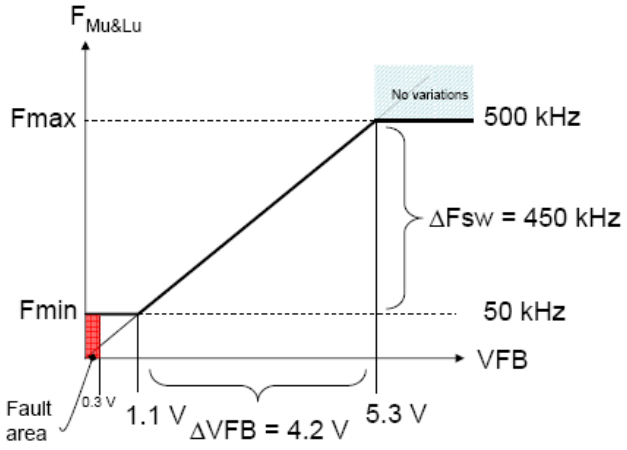


Figure 27. Maximal Default Excursion, Rt = 34 kΩ on Pin 4 and $R_{F(max)}$ = 1.9 kΩ on Pin 2

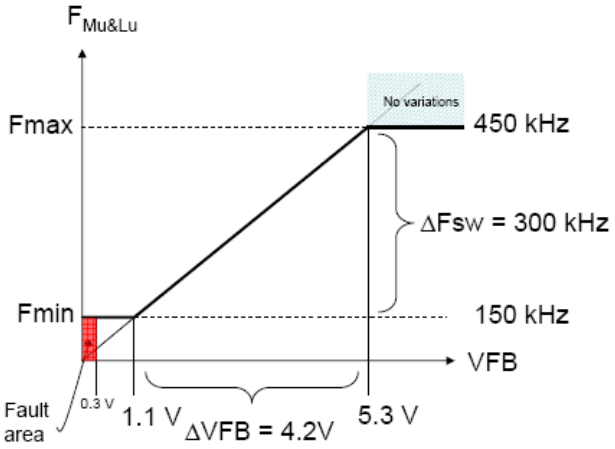


Figure 28. Here a different minimum frequency was programmed as well as a maximum frequency excursion

Please note that the previous small−signal VCO slope has now been reduced to 300k / 4.1 = 71 kHz / V on M_{upper} and M_{lower} outputs. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Due to this option, we will see how it becomes possible to observe the feedback level and implement skip cycle at light loads. It is important to note that the frequency evolution does not have a real linear relationship with the feedback voltage. This is due to the deadtime presence which stays constant as the switching period changes.

The selection of the three setting resistors (F_{max}, F_{min} and deadtime) requires the usage of the selection charts displayed below:

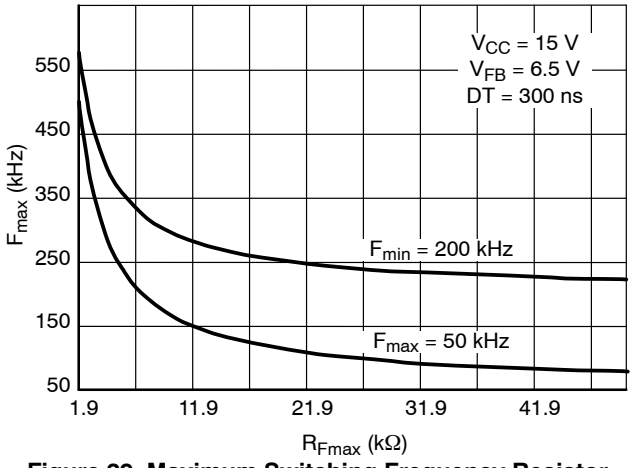


Figure 29. Maximum Switching Frequency Resistor Selection Depending on the Adopted Minimum Switching Frequency

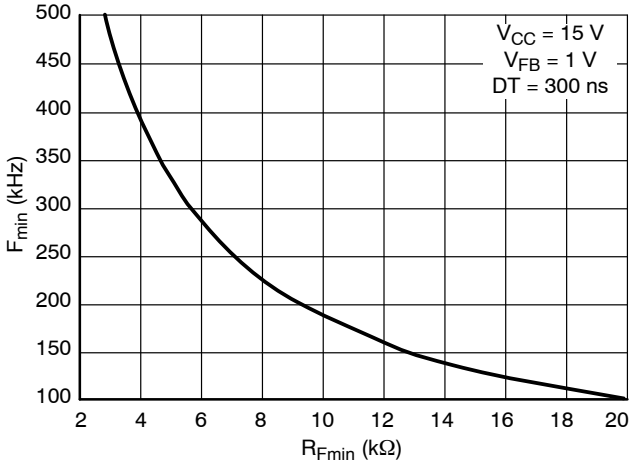


Figure 30. Minimum Switching Frequency Resistor Selection (F_{min} = 100 kHz to 500 kHz)

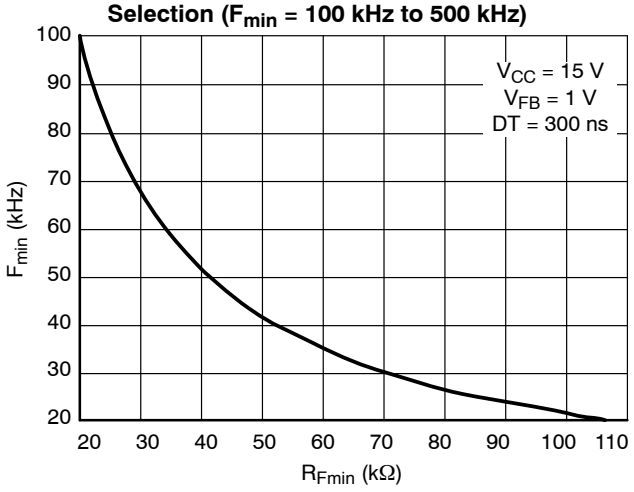


Figure 31. Minimum Switching Frequency Resistor Selection (F_{min} = 20 kHz to 100 kHz)

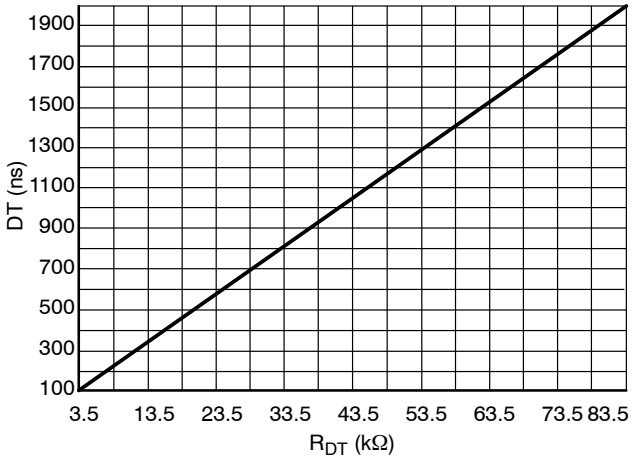


Figure 32. Deadtime Resistor Selection

ORing capability and optocoupler connection configurations

If for any particular reason, there is a need for a frequency variation linked to an event appearance (instead of abruptly stopping pulses), then the FB pin lends itself very well to the addition of other sweeping loops. Several diodes can easily be used perform the job in case of reaction to a fault event or to regulate on the output current (CC operation). Figure 33 shows how to do it.

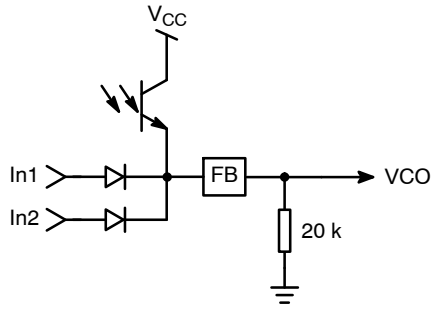


Figure 33. Thanks to the FB Configuration, Loop ORing is Easy to Implement

The VCO configuration used in this IC also offers an easy way to connect optocoupler (or pulldown bipolar) directly to the Rt pin instead of FB pin (refer to Figures 34 and 35). The optocoupler is then configured as “common emitter” and the operating frequency is controlled by the current that is taken out from the Rt pin – we have current controller oscillator (CCO). If one uses this configuration it is needed to maintain FB pin voltage between 0.3 V and 1 V otherwise the FB fault will be detected. The FB pin can be still used for open FB loop detection in some applications – to do so it is needed to keep optcoupler emitter voltage higher then 0.3 V for nominal load conditions. One needs to take R_{FB} pulldown resistor into account when using this configuration. It is possible to implement skip mode using Skip/disable input and emitter resistors R_{skip1} and R_{skip2}.

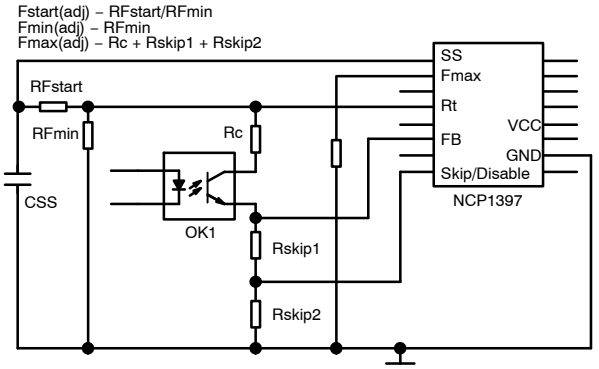


Figure 34. Feedback Configuration Using Direct Connection to the Rt Pin

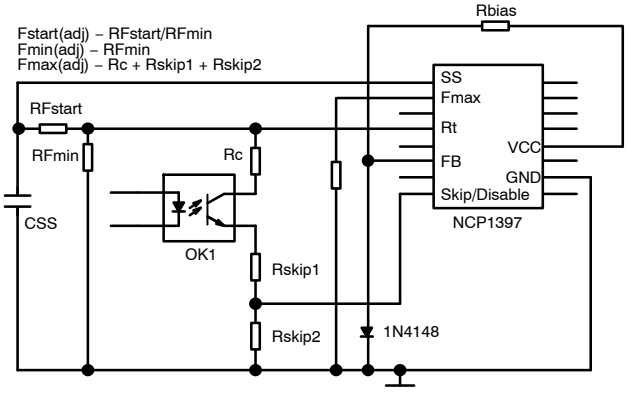


Figure 35. Feedback Configuration Using Direct Connection to the Rt Pin – No Open FB Loop Detection

Dead−Time Control

Deadtime control is an absolute necessity when the half−bridge configuration comes to play. The deadtime technique consists in inserting a period during which both high and low side switches are off. Of course, the deadtime amount differs depending on the switching frequency, hence the ability to adjust it on this controller. The option ranges between 100 ns and 2 μs. The deadtime is actually made by controlling the oscillator discharge current. Figure 36 portrays a simplified VCO circuit based on Figure 25. During the discharge time, the clock comparator is high and invalidates the AND gates: both outputs are low. When the comparator goes back to the low level, during the timing capacitor Ct recharge time, A and B outputs are validated. By connecting a resistor R_{DT} to ground, it creates a current whose image serves to discharge the Ct capacitor: we control the dead−time. The typical range evolves between 100 ns (R_{DT} = 3.5 kΩ) and 2 μs (R_{DT} = 83.5 kΩ). Figure 39 shows the typical waveforms.

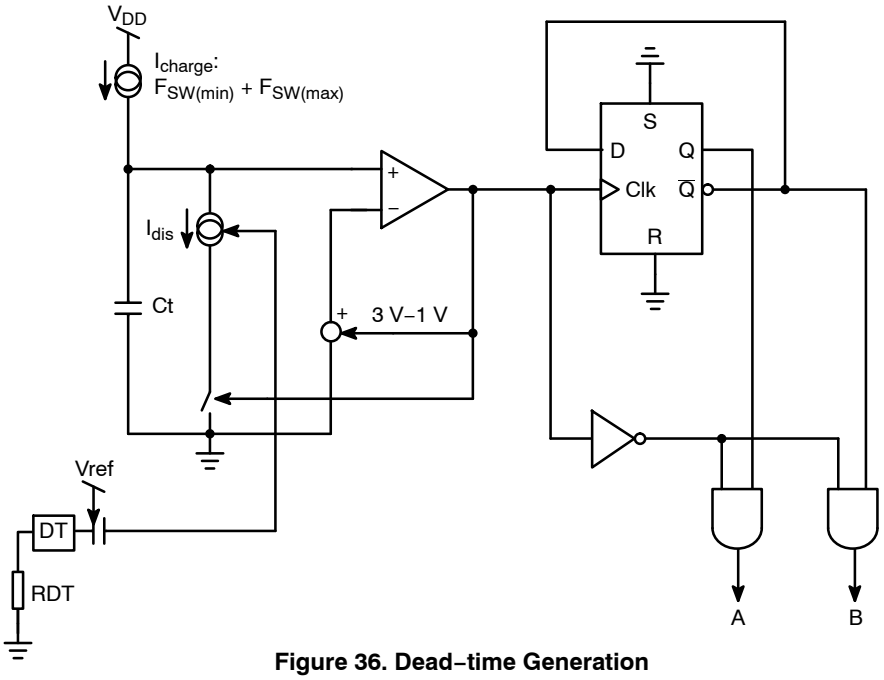


Figure 36. Dead−time Generation

Soft−Start Sequence

In resonant controllers, a soft−start is needed to avoid suddenly applying the full current into the resonating circuit. With this controller the soft−start duration is fully adjustable using eternal components. The purpose of the Soft−Start pin is to discharge Soft−Start capacitor before IC restart and in case of fault conditions detected by Fault input.

Once the controller starts operation, the Soft−Start capacitor (refer to Figure 37) is fully discharged and thus it starts charging from the Rt pin. The charging current increases operating frequency of the controller above F_{min}. As the soft−start capacitor charges, the frequency smoothly decreases down to F_{min}. Of course, practically, the feedback loop is supposed to take over the VCO lead as soon as the output voltage has reached the target. If not, then the minimum switching frequency is reached and a fault is detected on the feedback pin (typically below 300 mV). Figure 38 depicts a typical LLC startup using NCP1397A/B controller.

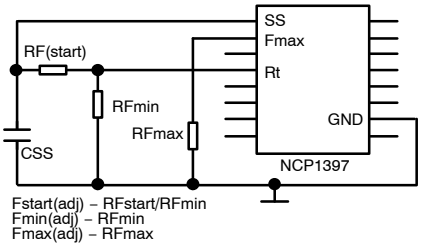


Figure 37. Soft−Start Components Arrangement

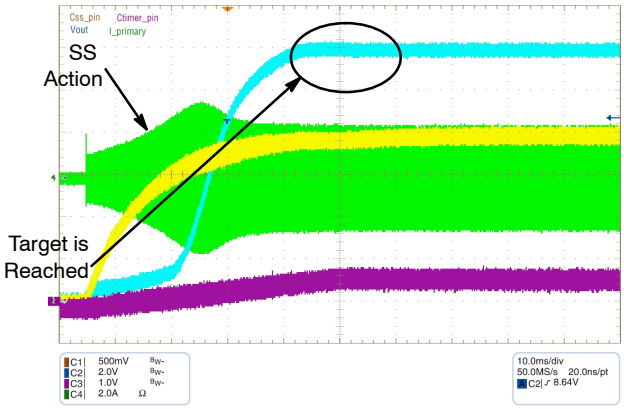


Figure 38. A Typical Startup Sequence on a LLC Converter Using NCP1397

Please note that the soft−start capacitor is discharged in the following conditions:

- A startup sequence
- During auto−recovery burst mode
- A brown−out recovery
- A temperature shutdown recovery

The skip/disable input undergoes a special treatment. Since we want to implement skip cycle using this input, we cannot activate the soft−start every time the feedback pin stops the operations in low power mode. Therefore, when the skip/enable pin is released, no soft−start occurs to offer the best skip cycle behavior. However, it is very possible to combine skip cycle and true disable, e.g. via ORing diodes driving Pin 8. In that case, if a signal maintains the skip/disable input high long enough to bring the feedback level down (below 0.3 V) since the output voltage starts to fall down, then the soft−start discharge switch is activated.

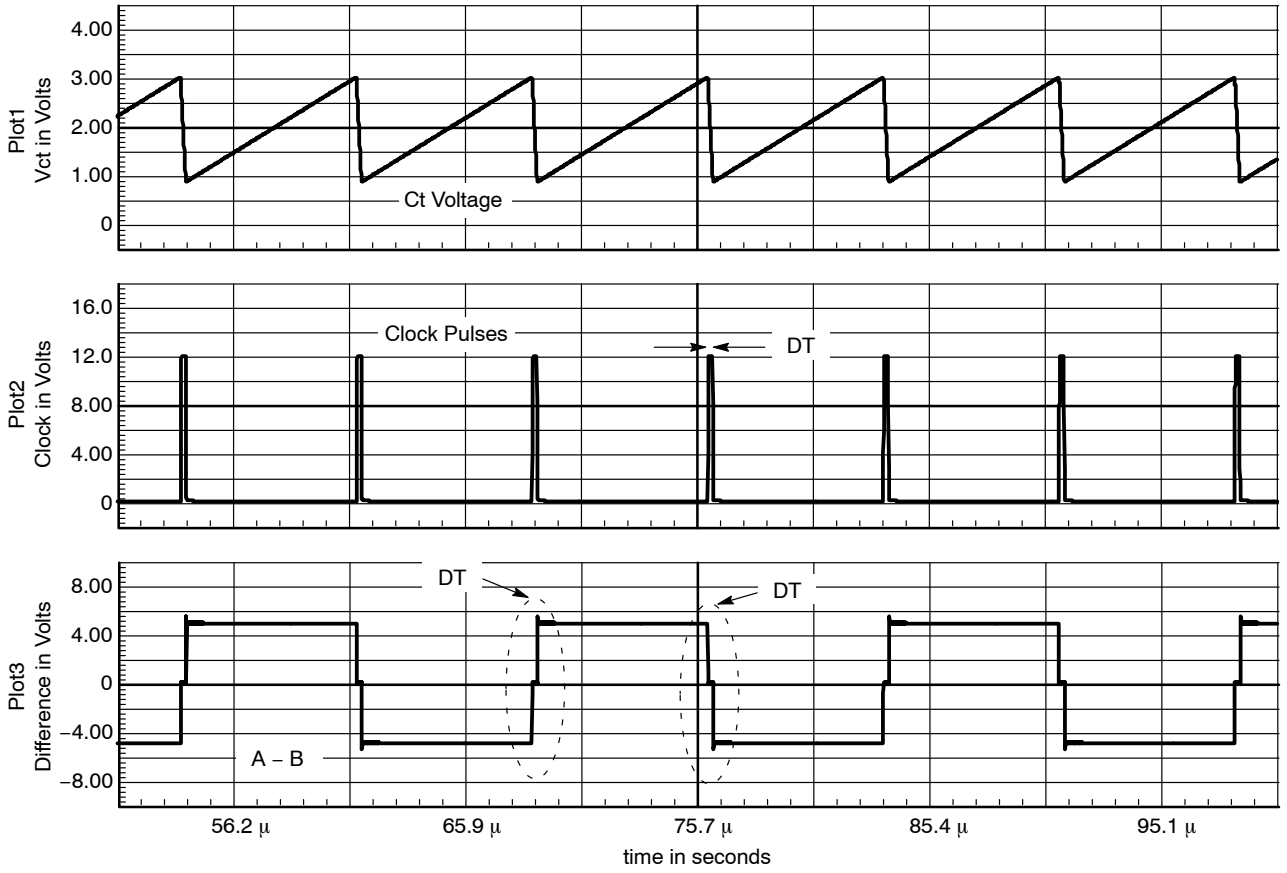


Figure 39. Typical Oscillator Waveforms

Brown−Out protection

The Brown−Out circuitry (BO) offers a way to protect the resonant converter from low DC input voltages. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 40, offers a way to observe the high−voltage (HV) rail. A resistive divider made of R_{upper} and R_{lower}, brings a portion of the HV rail on Pin 5. Below the turn−on level, the 28 μA current source IBO is off. Therefore, the turn−on level solely depends on the division ratio brought by the resistive divider.

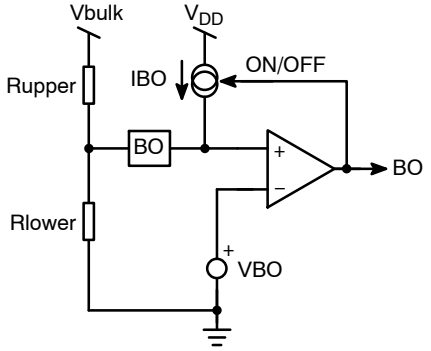


Figure 40. The Internal Brown−out Configuration with an Offset Current Source

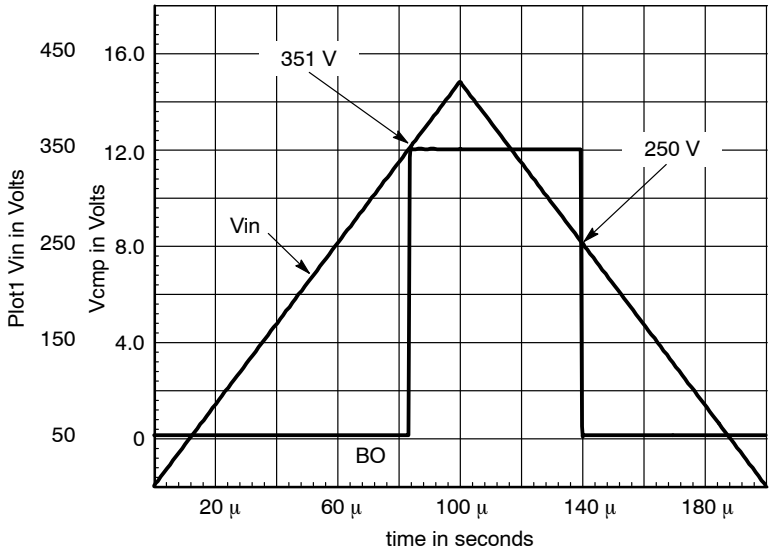


Figure 41. Simulation Results for 350 / 250 ON / OFF Levels

To the contrary, when the internal BO signal is high (M_{lower} and M_{upper} pulse), the IBO source is activated and creates a hysteresis. As a result, it becomes possible to select the turn−on and turn−off levels via a few lines of algebra:

IBO is off

$$V(+) = V_{bulk1} \times \frac{R_{lower}}{R_{lower} + R_{upper}} \qquad \text{(eq. 1)}$$

IBO is on

$$V(+) = V_{bulk2} \times \frac{R_{lower}}{R_{lower} + R_{upper}} + IBO \times \left(\frac{R_{lower} \times R_{upper}}{R_{lower} + R_{upper}}\right) \qquad \text{(eq. 2)}$$

We can now extract R_{lower} from Equation 1 and plug it into Equation 2, then solve for Rupper:

$$R_{upper} = R_{lower} \times \frac{V_{bulk1} - VBO}{VBO}$$

$$R_{lowerer} = VBO \times \frac{V_{bulk1} - V_{bulk2}}{IBO \times (V_{bulk1} - VBO)}$$

If we decide to turn−on our converter for Vbulk1 equals 350 V and turn it off for V_{bulk2} equals 250 V, then we obtain:

R_{upper} = 3.57 MΩ
R_{lower} = 10.64 kΩ

The bridge power dissipation is 400^2 / 3.781 MΩ = 45 mW when front−end PFC stage delivers 400 V.

Figure 41 simulation result confirms our calculations.

Latchoff Protection

There are some situations where the converter shall be fully turned−off and stay latched. This can happen in presence of an overvoltage (the feedback loop is drifting) or when an over temperature is detected. Thanks to the addition of a comparator on the BO pin, a simple external circuit can lift up this pin above V_{latch} (4 V typical) and permanently disable pulses. The V_{CC} needs to be cycled down below 6.5 V typically to reset the controller.

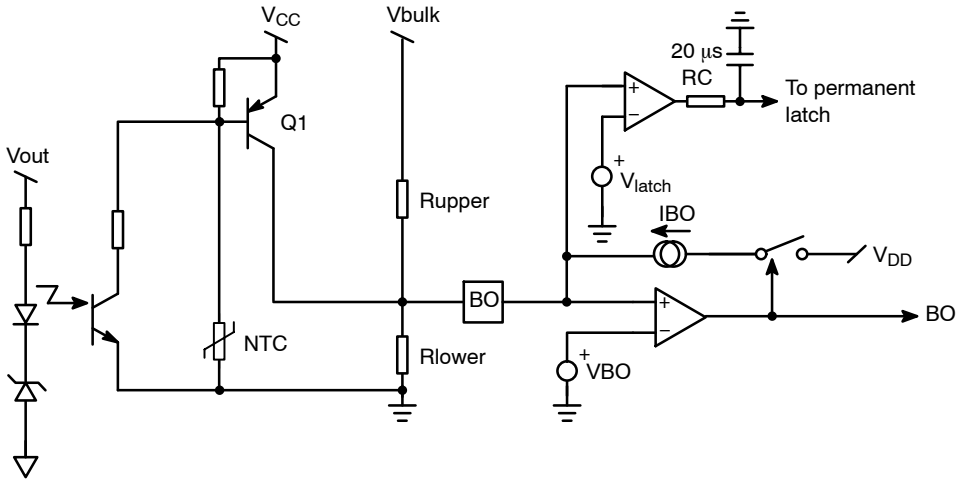


Figure 42. Adding a Comparator on the BO Pin Offers a way to Latch−off the Controller

On Figure 42, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is brought to ground and the BO pin goes up, permanently latching off the controller.

Protection Circuitry

This resonant controller offers a dedicated input (Fault input) to detect primary overcurrent conditions and protect power stage from damage.

Once the voltage on the Fault input exceeds 1.04 V threshold the external timer capacitor starts charging by I_{timer1} current. Simultaneously the Soft−Start discharge switch is activated to shift operating frequency up to keep primary current at acceptable level. In case the overload disappears fast enough the Soft−Start discharge switch is open, I_{timer1} current turned−off and timer capacitor discharges via an external parallel resistor. In case the overload lasts for more than timer duration (given by I_{timer}, V_{timer}, C_{timer} and R_{timer}) the IC stops the operation and waits until the C_{timer} will discharge to 1 V. The application then restarts via Soft−Start.

In case of heavy overload, like transformer short circuit, the primary current grows very fast and thus could reach danger level prior the fault timer elapses. The NCP1397B therefore features additional comparator (1.55 V) on the Fault input to permanently latch the application and protect against destruction. Figure 44 depicts the architecture of the fault circuitry for NCP1397B controller.

The NCP1397A features second fault comparator as well but in this case it doesn't latches off the IC but speeds up the Fault timer capacitor charging by turning on additional current source I_{timer2} – refer to Figure 43. The NCP1397A can thus be used in applications that have to recover automatically from any fault conditions.

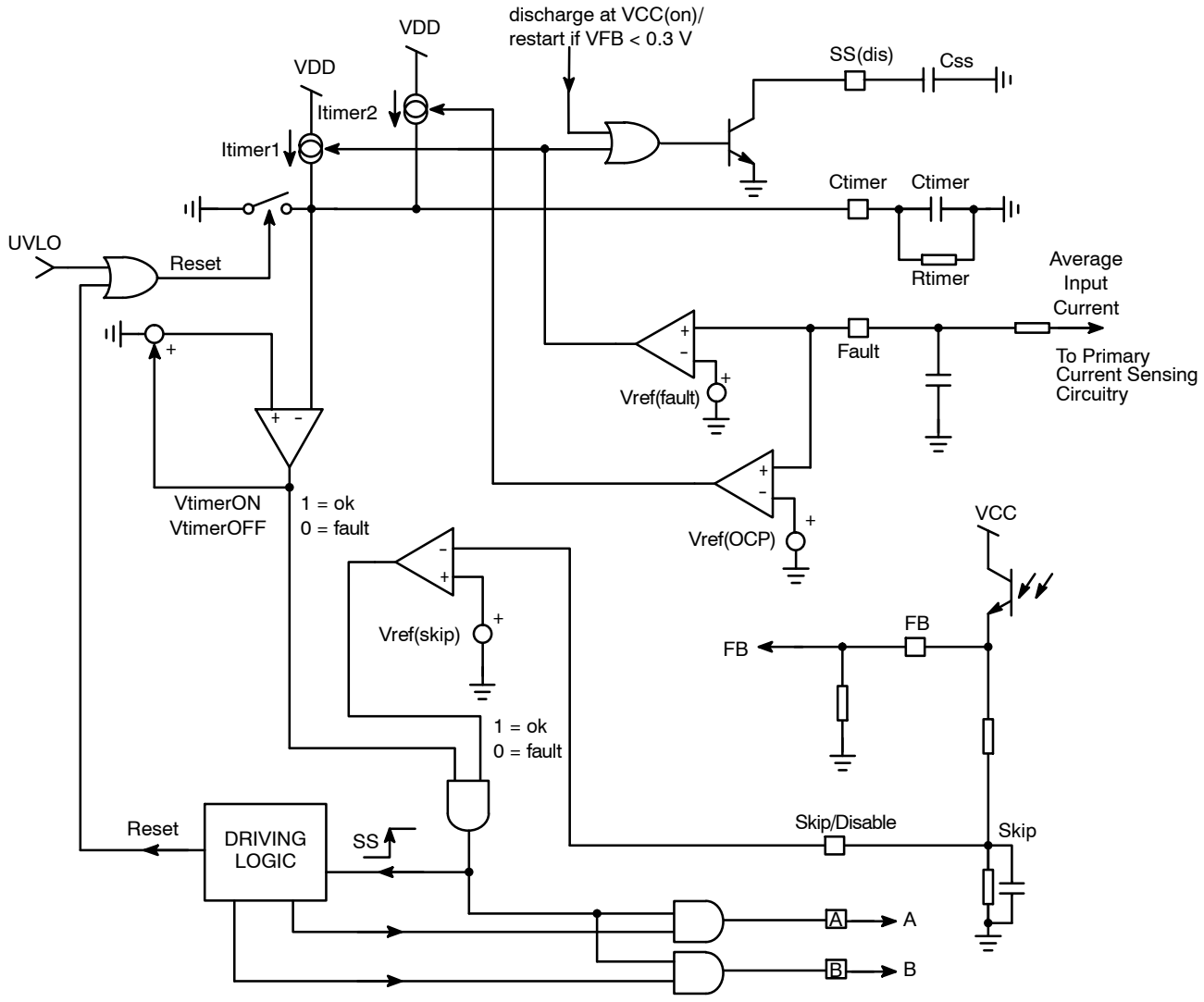


Figure 43. Fault Input Logic for NCP1397A

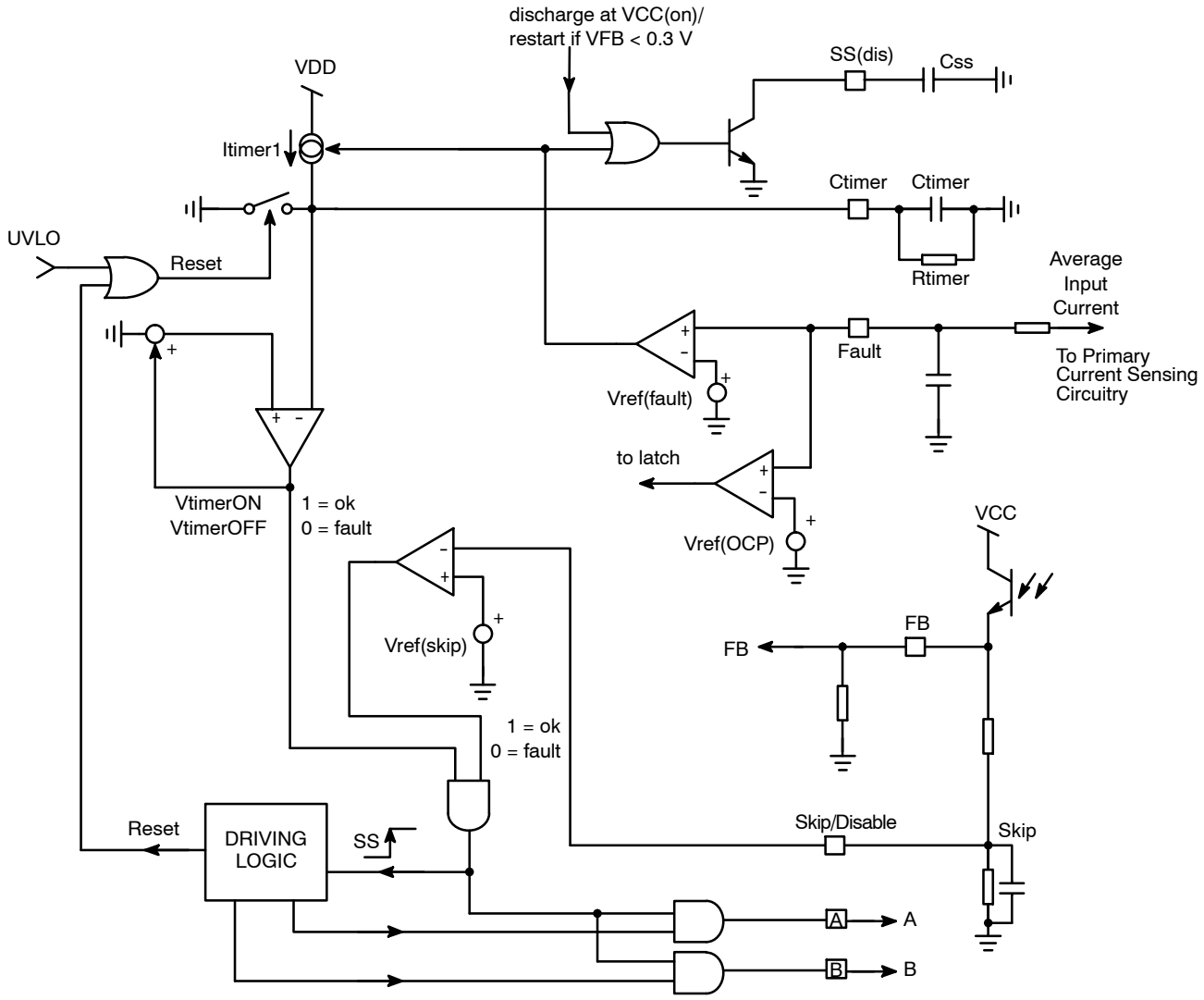


Figure 44. Fault Input Logic for NCP1397B

On Figures 43 and 44 examples, a voltage proportional to primary current, once averaged, gives an image of the input power in case V_{in} is kept constant via a PFC circuit. If the output loading increases above a certain level, the voltage on this pin will pass the 1 V threshold and start the timer. If the overload stays there, after a few tens of milli −seconds, switching pulses will disappear and a protective auto−recovery cycle will take place. Adjusting the resistor R in parallel with the timer capacitor will give the flexibility to adjust the fault burst mode (refer to Figure 45).

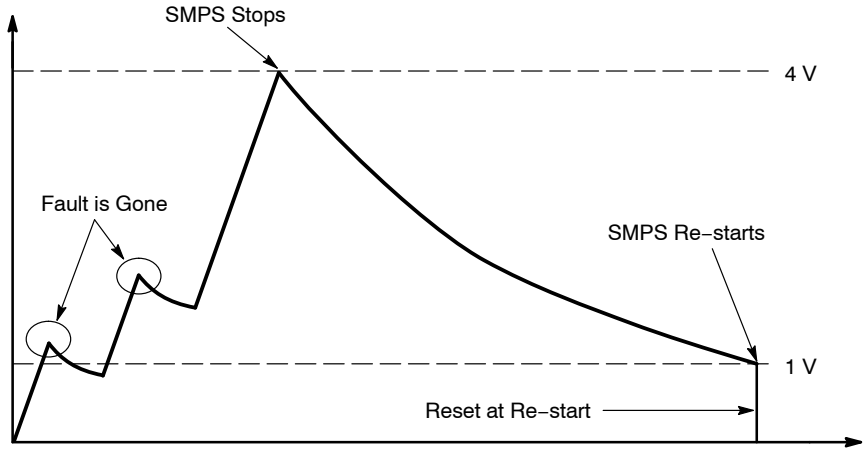


Figure 45. A Resistor Can Easily Program the Capacitor Discharge Time

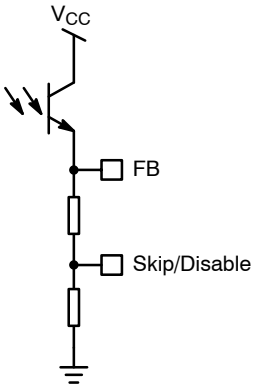


Figure 46. Skip Cycle Can Be Implemented Via Two Resistors on the FB Pin to the Fast Fault Input

Skip/Disable

The Skip/Disable input is not affected by a delayed action. As soon as its voltage exceeds 0.66 V typical, all pulses are off and maintained off as long as the fault is present. When the pin is released, pulses come back and the soft−start is activated (in case the V_{FB} < 0.3 V).

Thanks to the low activation level, this pin can observe the feedback pin via a resistive divided and thus implement skip cycle operation. The resonant converter can be designed to lose regulation in light load conditions, forcing the FB level to increase. When it reaches the programmed level, it triggers the skip input and stops pulses. Then V_{out} slowly drops, the loop reacts by decreasing the feedback level which, in turn, unlocks the pulses, V_{out} goes up again and so on: we are in *skip cycle* mode. As the feedback voltage does not drop below 0.3 V the Soft−Start discharge switch is not activated in this case. Please refer also to Figure 35 for skip mode function implementation when optocoupler is connected directly to Rt pin.

Startup Behavior

When the V_{CC} voltage increases, the internal current consumption is kept below I_{strup}. When V_{CC} reaches the $V_{CC(on)}$ level, output Mlower goes high first and then output Mupper. This sequence will always be the same whatever triggers the pulse delivery: fault, OFF to ON etc… Pulsing the output M_{lower} high first gives an immediate charge of the bootstrap capacitor. Then, the rest of pulses follow, delivered at the highest switching value, set by the R_{Fstart} resistor in parallel with R_{Fmin} resistor on Pin 4. The soft−start capacitor ensures a smooth frequency decrease to either the programmed minimum value (in case of fault) or to a value corresponding to the operating point if the feedback loop closes first. Figure 47 shows typical signals evolution at power on.

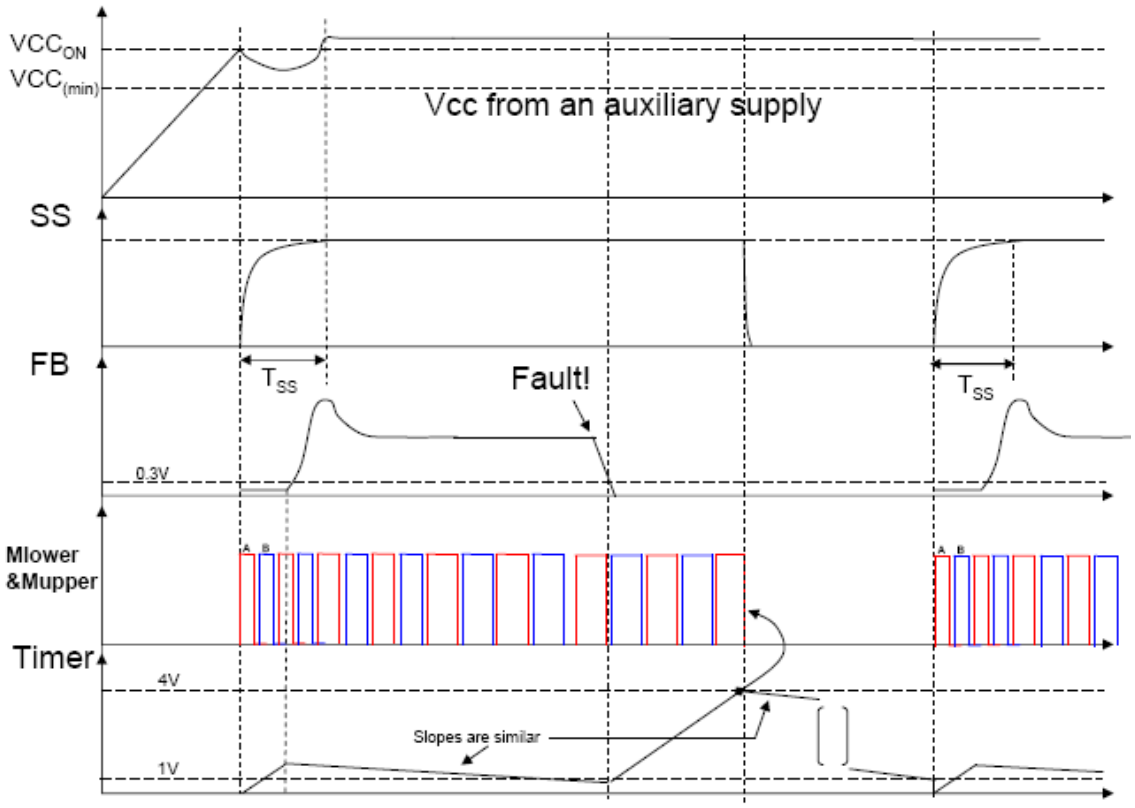


Figure 47. At Power On, Output A is First Activated and the Frequency Slowly Decreases Based on the Soft−Start Capacitor Voltage

Figure 47 depicts an auto−recovery situation, where the timer has triggered the end of output pulses. In that case, the V_{CC} level was given by an auxiliary power supply, hence its stability during the hiccup. A similar situation can arise if the user selects a more traditional startup method, with an auxiliary winding. In that case, the $V_{CC(min)}$ comparator stops the output pulses whenever it is activated, that is to say, when V_{CC} falls below 9.5 V typical. At this time, the V_{CC} pin still receives its bias current from the startup resistor and increases toward $V_{CC(on)}$. When the voltage reaches $V_{CC(on)}$, a standard sequence takes place, involving a soft−start. Figure 48 portrays this behavior.

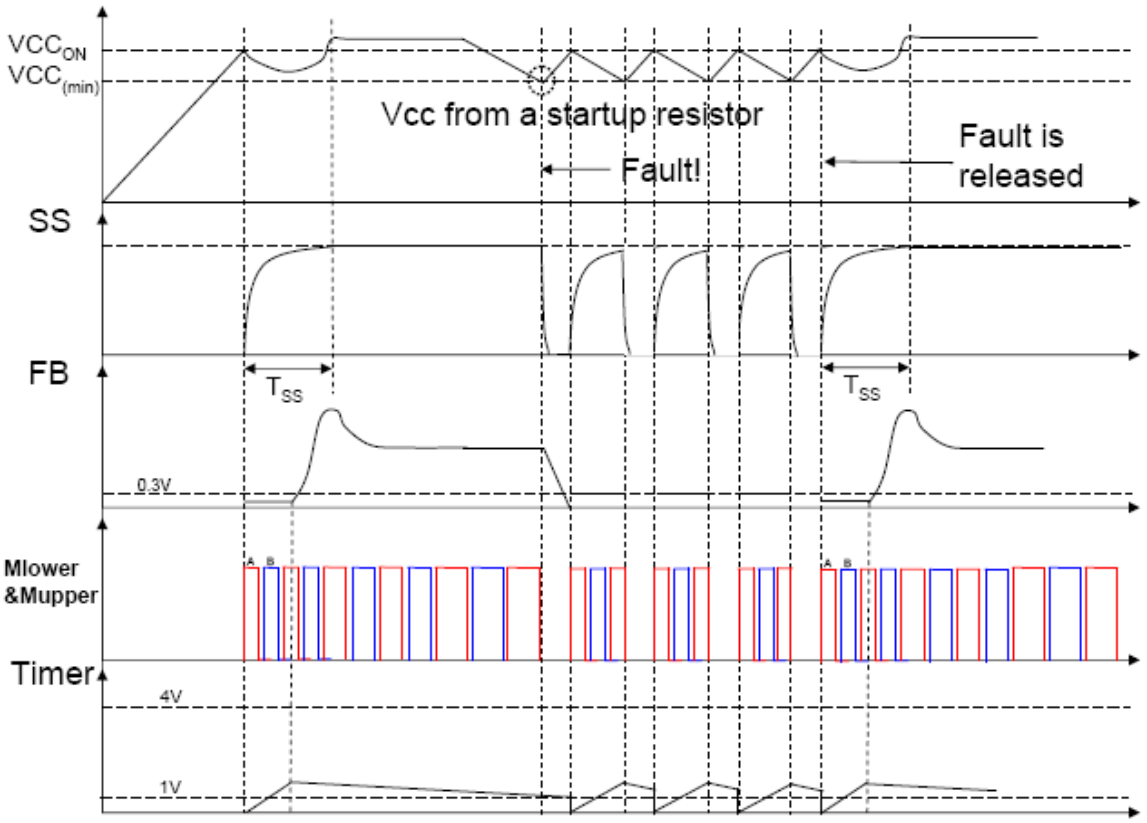


Figure 48. When the V_{CC} is to Low, All Pulses are Stopped Until V_{CC} Goes Back to the Startup Voltage

The High−Voltage Driver

The driver features a traditional bootstrap circuitry, requiring an external high−voltage diode for the capacitor refueling path. Figure 49 shows the internal architecture of the high−voltage section.

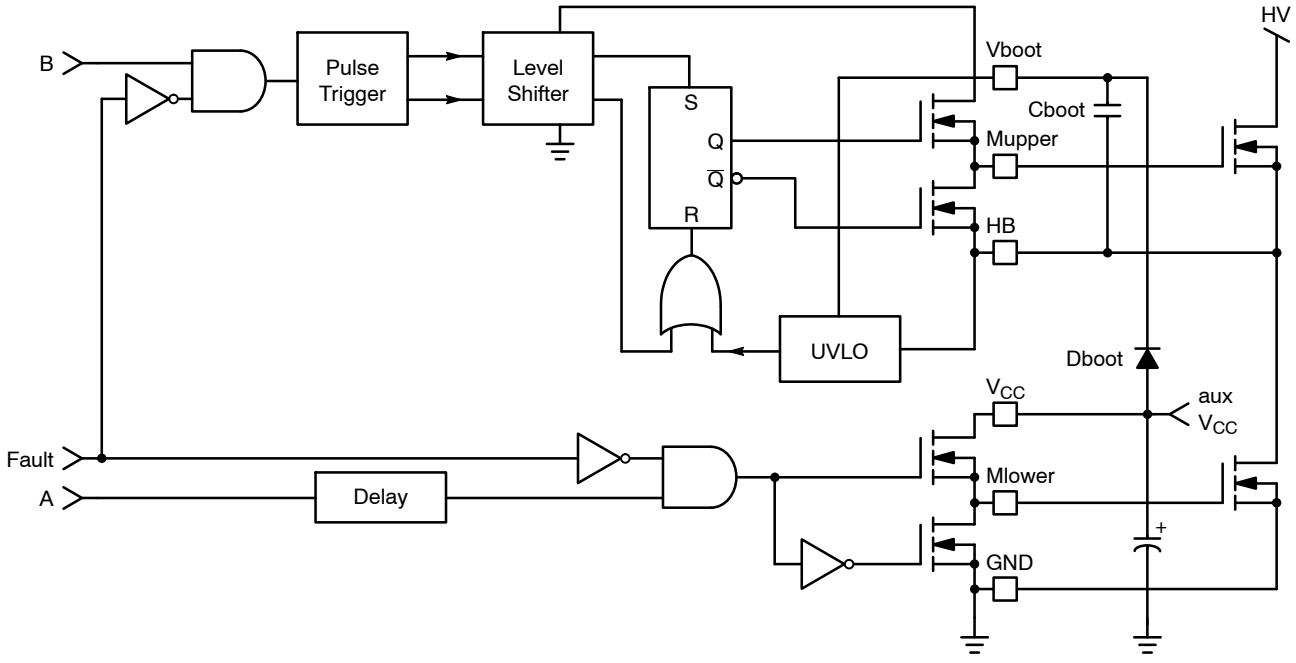


Figure 49. The Internal High−voltage Section of the NCP1397

The device incorporates an upper UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The B and A outputs are delivered by the internal logic, as Figure 43 testifies. A delay is inserted in the lower rail to ensure good matching between these propagating signals.

As stated in the maximum rating section, the floating portion can go up to 600 VDC and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

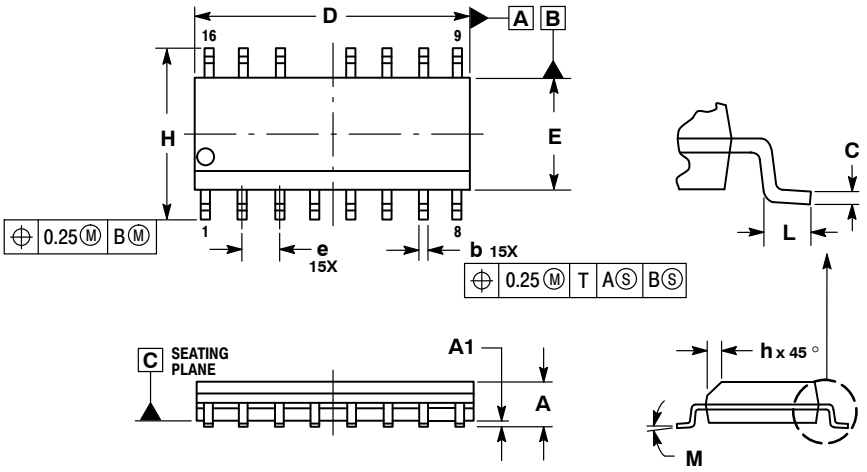
ORDERING INFORMATION

Device	Package	Shipping†
NCP1397ADR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel
NCP1397BDR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

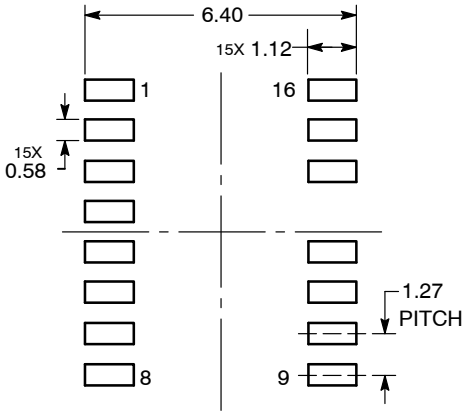
SOIC−16 NB, LESS PIN 13
CASE 751AM−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The product described herein (NCP1397A/B), is covered by U.S. patent: 6,097, 075; 7176723; 6,362, 067. There may be some other patent pending.

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