# 2.5V / 3.3V 1:2 Differential LVPECL Clock / Data Fanout Buffer

# Multi-Level Inputs with Internal Termination

#### **Description**

The NB6L611 is a differential 1:2 clock or data fanout buffer. The differential inputs incorporate internal 50  $\Omega$  termination resistors that are accessed through the VTD pins and will accept LVPECL, CML, LVDS, LVCMOS or LVTTL logic levels.

The  $V_{REFAC}$  reference output can be used to rebias capacitor–coupled differential or single–ended input signals. When used, decouple  $V_{REFAC}$  with a 0.01  $\mu F$  capacitor and limit current sourcing or sinking to 0.5 mA. When used, decouple  $V_{REFAC}$  with a 0.01  $\mu F$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{REFAC}$  output should be left open.

The device is housed in a small 3x3 mm 16 pin QFN package.

The NB6L611 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

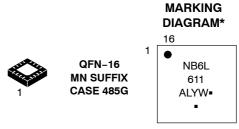
#### **Features**

- Input Clock Frequency > 4.0 GHz
- 280 ps Typical Propagation Delay
- 100 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- Differential LVPECL Outputs, 780 mV Amplitude, typical
- LVPECL Operating Range:  $V_{CC} = 2.375 \text{ V}$  to 3.63 V with  $V_{EE} = 0 \text{ V}$
- NECL Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -2.375 \text{ V}$  to -3.63 V
- $\bullet$  Internal Input Termination Resistors, 50  $\Omega$
- V<sub>REFAC</sub> Reference Output Voltage
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



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A = Assembly Location

L = Wafer Lot Y = Year W = Work Week • Pb-Free Package

(Note: Microdot may be in either location)

<sup>\*</sup>For additional marking information, refer to Application Note AND8002/D.

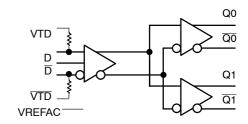


Figure 1. Simplified Logic Diagram

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

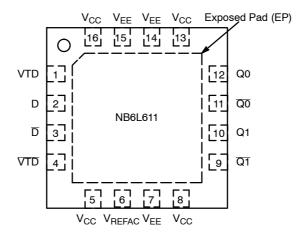


Figure 2. Pin Configuration (Top View)

#### **Table 1. PIN DESCRIPTION**

Pin	Name	I/O	Description	
1	VTD	-	Internal 50 $\Omega$ Termination Pin for D input.	
2	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Note1. Internal 50 $\Omega$ Resistor to Termination Pin, VTD.	
3	D	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Note 1. Internal 50 $\Omega$ Resistor to Termination Pin, $\overline{\text{VTD}}$ .	
4	VTD	ı	Internal 50 $\Omega$ Termination Pin for $\overline{\mathrm{D}}$ input.	
5	V <sub>CC</sub>	-	Positive Supply Voltage	
6	V <sub>REFAC</sub>		Output Reference Voltage for direct or capacitor coupled inputs	
7	V <sub>EE</sub>	-	Negative Supply Voltage	
8	V <sub>CC</sub>	-	Positive Supply Voltage	
9	Q1	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>CC</sub> – 2.0 V.	
10	Q1	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>CC</sub> – 2.0 V.	
11	Q0	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V $_{CC}$ – 2.0 V.	
12	Q0	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to V <sub>CC</sub> – 2.0 V.	
13	V <sub>CC</sub>	-	Positive Supply Voltage	
14	V <sub>EE</sub>	-	Negative Supply Voltage	
15	V <sub>EE</sub>	-	Negative Supply Voltage	
16	V <sub>CC</sub>	-	Positive Supply Voltage	
_	EP	-	The Exposed Pad (EP) on the QFN–16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat–sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to V <sub>EE</sub> on the PC board.	

<sup>1.</sup> In the differential configuration when the input termination pins (VTD, VTD) are connected to a common termination voltage or left open, and if no signal is applied on D/D input, then, the device will be susceptible to self–oscillation.

2. All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to a power supply for proper operation.

**Table 2. ATTRIBUTES** 

Cha	Value			
ESD Protection	Human Body Model Machine Model	> 2 kV > 200V		
Moisture Sensitivity	16-QFN	Level 1		
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
Transistor Count				
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test				

For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS** 

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	V <sub>EE</sub> = 0 V		4.0	V
V <sub>EE</sub>	Negative Power Supply	V <sub>CC</sub> = 0 V		-4.0	V
V <sub>IO</sub>	Positive Input/Output Voltage Negative Input/Output Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	$ \begin{array}{l} -0.5 \leq V_{IO} \leq V_{CC} + 0.5 \\ +0.5 \geq V_{IO} \geq V_{EE} - 0.5 \end{array} $	4.5 -4.5	V V
V <sub>INPP</sub>	Differential Input Voltage  D - D			V <sub>CC</sub> -V <sub>EE</sub>	V
I <sub>IN</sub>	Input Current Through R <sub>T</sub> (50 Ω Resistor)	Static Surge		45 80	mA mA
I <sub>OUT</sub>	Output Current (LVPECL Output)	Continuous Surge		50 100	mA mA
I <sub>VREFAC</sub>	V <sub>REFAC</sub> Sink/Source Current			±2.0	mA
T <sub>A</sub>	Operating Temperature Range	16 QFN		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 35	°C/W °C/W
θJC	Thermal Resistance (Junction-to-Case)	(Note 3)	QFN-16	4	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

 $\textbf{Table 4. DC CHARACTERISTICS, Multi-Level Inputs} \ V_{CC} = 2.375 \ V \ to \ 3.63 \ V, \ V_{EE} = 0 \ V, \ or \ V_{CC} = 0 \ V, \ V_{EE} = -2.375 \ V \ to \ Solve = -2.37$  $-3.63 \text{ V}, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ 

Symbol	Characteristic	Min	Тур	Max	Unit		
POWER S	UPPLY CURRENT						
I <sub>CC</sub>	Power Supply Current (Inputs and Outputs Open)	30	45	60	mA		
LVPECL OUTPUTS (Notes 4 and 5)							
V <sub>OH</sub>	Output HIGH Voltage $ \begin{array}{c} V_{CC} = 3.3 \ V \\ V_{CC} = 2.5 \ V \end{array} $	V <sub>CC</sub> – 1075 2225 1425	V <sub>CC</sub> – 950 2350 1550	V <sub>CC</sub> - 825 2475 1675	mV		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> – 1875 1475 675	V <sub>CC</sub> – 1725 1575 775	V <sub>CC</sub> - 1625 1675 875	mV		
DIFFERE	NTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 9 and 10) (Note 6	i)					
V <sub>th</sub>	Input Threshold Reference Voltage Range (Note 7)	V <sub>EE</sub> + 1050		V <sub>CC</sub> – 150	mV		
V <sub>IH</sub>	Single-ended Input HIGH Voltage	V <sub>th</sub> + 150		V <sub>CC</sub>	mV		
V <sub>IL</sub>	Single-ended Input LOW Voltage	$V_{EE}$		V <sub>th</sub> – 150	mV		
V <sub>ISE</sub>	Single-ended Input Voltage Amplitude (V <sub>IH</sub> - V <sub>IL</sub> )	300		$V_{CC}$ - $V_{EE}$	mV		
V <sub>REFAC</sub>							
V <sub>REFAC</sub>	Output Reference Voltage (V <sub>CC</sub> ≥ 25 V)	V <sub>CC</sub> – 1.525	V <sub>CC</sub> – 1.425	V <sub>CC</sub> – 1.325	mV		
DIFFERE	NTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 11, 12 and 13)	(Note 8)					
$V_{IHD}$	Differential Input HIGH Voltage	V <sub>EE</sub> + 1200		V <sub>CC</sub>	mV		
$V_{ILD}$	Differential Input LOW Voltage	V <sub>EE</sub>		V <sub>CC</sub> – 150	mV		
$V_{\text{ID}}$	Differential Input Voltage (V <sub>IHD</sub> – V <sub>ILD</sub> )	V <sub>EE</sub> + 150		$V_{CC}$ - $V_{EE}$	mV		
V <sub>CMR</sub>	Input Common Mode Range (Differential Configuration) (Note9)	V <sub>EE</sub> + 950		V <sub>CC</sub> – 75	mV		
I <sub>IH</sub>	Input HIGH Current D/D, (VTD/VTD Open)	-150		150	μΑ		
I <sub>IL</sub>	Input LOW Current D/D, (VTD/VTD Open)	-150		150	μΑ		
TERMINA	TION RESISTORS						
R <sub>TIN</sub>	Internal Input Termination Resistor (Measured from D to VTD)	40	50	60	Ω		

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 4. LVPECL outputs loaded with 50  $\Omega$  to  $V_{CC}$  2.0 V for proper operation. 5. Input and output parameters vary 1:1 with  $V_{CC}$ .

- V<sub>th</sub>, V<sub>IH</sub>, V<sub>IL</sub>, and V<sub>ISE</sub> parameters must be complied with simultaneously.
   V<sub>th</sub> is applied to the complementary input when operating in single-ended mode.
- 8. V<sub>IHD</sub>, V<sub>ILD</sub>, V<sub>ID</sub> and V<sub>CMR</sub> parameters must be complied with simultaneously.
- V<sub>CMR</sub> minimum varies 1:1 with V<sub>EE</sub>, V<sub>CMR</sub> maximum varies 1:1 with V<sub>CC</sub>. The V<sub>CMR</sub> range is referenced to the most positive side of the differential input signal.

**Table 5. AC CHARACTERISTICS**  $V_{CC} = 2.375 \text{ V}$  to 3.63 V,  $V_{EE} = 0 \text{ V}$ , or  $V_{CC} = 0 \text{ V}$ ,  $V_{EE} = -2.375 \text{ V}$  to -3.63 V,  $V_{A} = -40 \text{ C}$  to +85°C; (Note 10)

Symbol	Characteristic			Тур	Max	Unit
V <sub>OUTPP</sub>	Output Voltage Amplitude (@ V <sub>INPP</sub> )  (Note 14) (See Figure 3)	$\begin{aligned} &f_{\text{in}} \leq 1.5 \text{ GHz} \\ &f_{\text{in}} = 2.0 \text{ GHz} \\ &f_{\text{in}} = 3.0 \text{ GHz} \\ &f_{\text{in}} = 4.0 \text{ GHz} \end{aligned}$	725 520 320 170	780 680 500 400		mV
t <sub>PD</sub>	Propagation Delay	D to Q	225	280	375	ps
t <sub>SKEW</sub>	Duty Cycle Skew (Note 11) Within Device Skew Device to Device Skew (Note 12)			3	15 15 80	ps
t <sub>DC</sub>	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	f <sub>in</sub> ≤ 4.0 GHz	40	50	60	ps
t <sub>JITTER</sub>	RMS Random Clock Jitter (Note 13)	f <sub>in</sub> ≤ 4.0 GHz		0.2	0.5	ps
V <sub>INPP</sub>	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14)		150		V <sub>CC</sub> – V <sub>EE</sub>	mV
t <sub>r</sub> ,t <sub>f</sub>	Output Rise/Fall Times @ 0.5 GHz (20% - 80%)	Q, $\overline{Q}$		100	170	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 10. Measured by forcing  $V_{INPP}$  (MIN) from a 50% duty cycle clock source. All loading with an external  $R_L$  = 50  $\Omega$  to  $V_{CC}$  2.0 V. Input edge rates 40 ps (20% 80%).
- 11. Duty cycle skew is measured between differential outputs using the deviations of the sum of T<sub>pw</sub>- and T<sub>pw</sub>+ @ 0.5GHz.
- 12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
- 13. Additive RMS jitter with 50% duty cycle clock signal.
- 14. Input and output voltage swing is a single-ended measurement operating in differential mode.

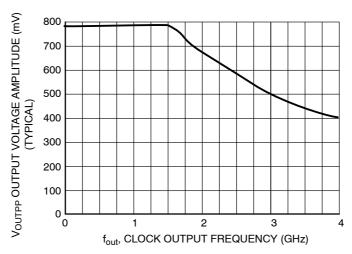


Figure 3. Output Voltage Amplitude (V<sub>OUTPP</sub>) versus Output Frequency at Ambient Temperature (Typical)

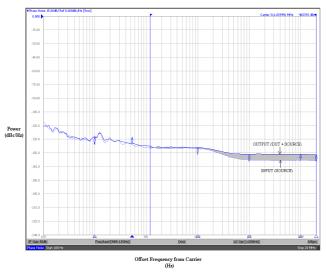


Figure 4. Typical Phase Noise Plot at f<sub>carrier</sub> = 311.04 MHz

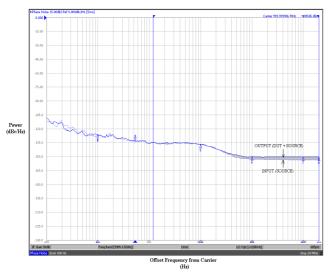


Figure 6. Typical Phase Noise Plot at f<sub>carrier</sub> = 1 GHz

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L611 device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the

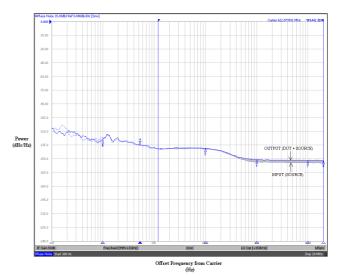


Figure 5. Typical Phase Noise Plot at f<sub>carrier</sub> = 622.08 MHz

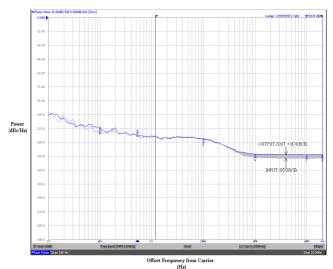


Figure 7. Typical Phase Noise Plot at f<sub>carrier</sub> = 2 GHz

device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 44 fs, 11 fs, 8 fs and 6 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

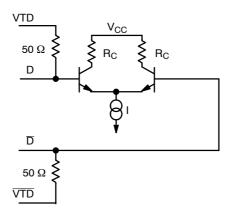


Figure 8. Input Structure

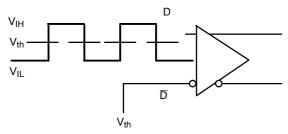


Figure 9. Differential Input Driven Single-Ended

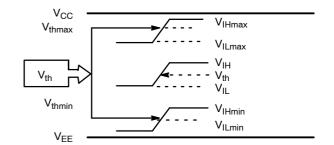


Figure 10. V<sub>th</sub> Diagram

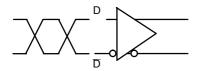


Figure 11. Differential Inputs Driven Differentially

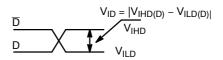


Figure 12. Differential Inputs Driven Differentially

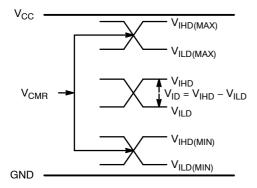


Figure 13. V<sub>CMR</sub> Diagram

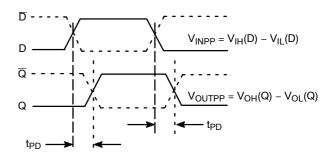


Figure 14. AC Reference Measurement

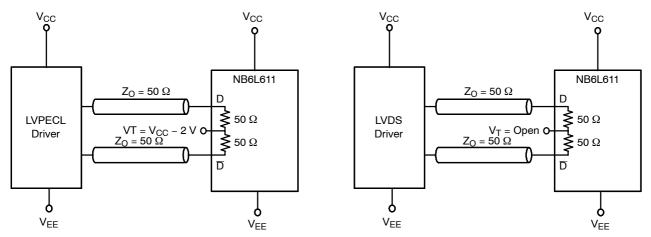


Figure 15. LVPECL Interface

Figure 16. LVDS Interface

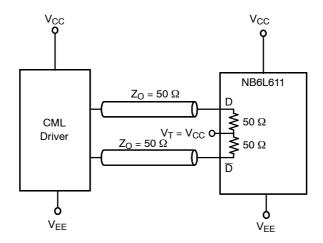
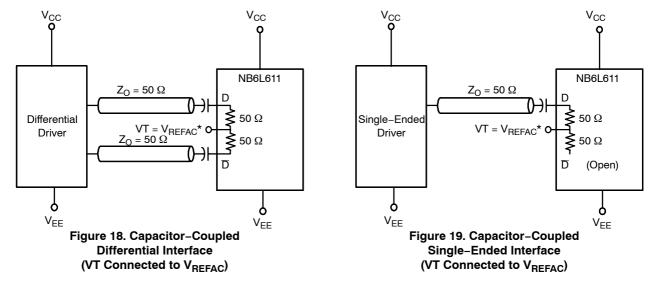


Figure 17. Standard 50  $\Omega$  Load CML Interface



<sup>\*</sup>V\_REFAC bypassed to ground with a 0.01  $\mu\text{F}$  capacitor

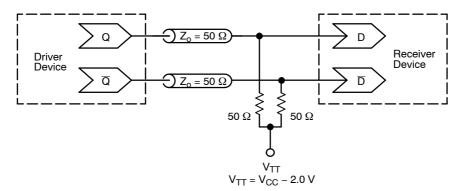


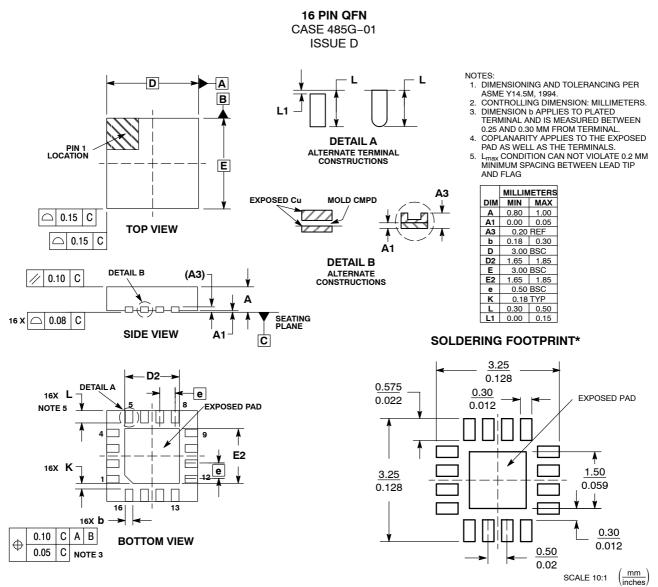
Figure 20. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NB6L611MNG	QFN-16 (Pb-free)	123 Units / Rail
NB6L611MNR2G	QFN-16 (Pb-free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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