High Speed Low Power CAN Transceiver

Description

The NCV7340 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7340 is a new addition to the CAN high–speed transceiver family and is an improved drop–in replacement for the AMIS–42665.

Due to the wide common-mode voltage range of the receiver inputs, the NCV7340 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Features

- Compatible with the ISO 11898 Standard (ISO 11898–2, ISO 11898–5 and SAE J2284)
- Low Quiescent Current
- High Speed (up to 1 Mbps)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Extremely Low Current Standby Mode with Wakeup via the Bus
- Low EME Common-Mode Choke is No Longer Required
- Voltage Source via V_{SPLIT} Pin for Stabilizing the Recessive Bus Level (Further EMC Improvement)
- No Disturbance of the Bus Lines with an Un-powered Node
- Transmit Data (TxD) Dominant Time-out Function
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Bus and V_{SPLIT} Pins Short–Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- Up to 110 Nodes can be Connected to the Same Bus in Function of Topology
- These are Pb-Free Devices

Typical Applications

- Automotive
- Industrial Networks

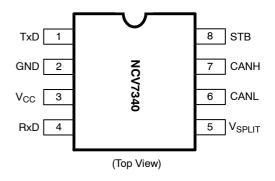


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PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Power supply voltage		4.75	5.25	V
V _{STB}	DC voltage at pin STB		0	V_{CC}	٧
V_{TxD}	DC voltage at pin TxD		0	V_{CC}	٧
V _{RxD}	DC voltage at pin RxD		0	V_{CC}	V
V _{CANH}	DC voltage at pin CANH	0 < V _{CC} < 5.25 V; no time limit	-50	+50	V
V _{CANL}	DC voltage at pin CANL	0 < V _{CC} < 5.25 V; no time limit	-50	+50	V
V _{SPLIT}	DC voltage at pin V _{SPLIT}	0 < V _{CC} < 5.25 V; no time limit	-40	+40	V
V _{O(dif)(bus_dom)}	Differential bus output voltage in dominant state	$42.5 \Omega < R_{LT} < 60 \Omega$	1.5	3	V
CM-range	Input common–mode range for comparator	Guaranteed differential receiver threshold and leakage current	-35	+35	V
C _{load}	Load capacitance on IC outputs			15	pF
t _{pd(rec-dom)}	Propagation delay TxD to RxD	See Figure 7	75	230	ns
t _{pd(dom-rec)}	Propagation delay TxD to RxD	See Figure 7	75	245	ns
T _J	Junction temperature		-40	150	°C

BLOCK DIAGRAM

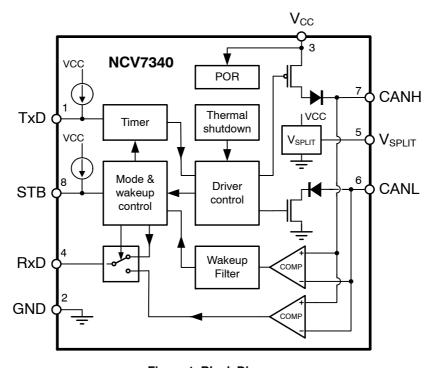


Figure 1. Block Diagram

TYPICAL APPLICATION

Application Schematics

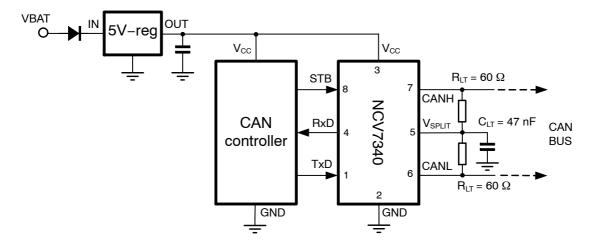


Figure 2. Application Diagram

Pin Description

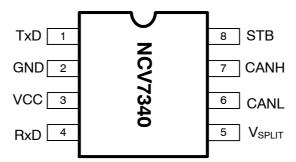


Figure 3. NCV7340 Pin Assignment

Table 2. PIN FUNCTION DESCRIPTION

Pin	Name	Description	
1	TxD	Transmit data input; low input $ ightarrow$ dominant driver; internal pullup current	
2	GND	Ground	
3	VCC	Supply voltage	
4	RxD	Receive data output; dominant transmitter $ ightarrow$ low output	
5	V _{SPLIT}	Common-mode stabilization output	
6	CANL	Low-level CAN bus line (low in dominant mode)	
7	CANH	High-level CAN bus line (high in dominant mode)	
8	STB	Standby mode control input	

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7340 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

Table 3. OPERATING MODES

Pin		Pin RXD			
STB	Mode	Low	High		
Low	Normal	Bus dominant	Bus recessive		
High	Standby	Wakeup request detected	No wakeup request detected		

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low-power differential receiver monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μ A. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of t_{dbus} , the RxD pin is driven low by the transceiver to inform the controller of the wake-up request.

Split Circuit

The V_{SPLIT} pin is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} can be connected as shown in Figure 2 or, if it's not used, can be left floating. Its purpose is to provide a stabilized DC voltage of 0.5 x V_{CC} to the bus avoiding possible steps in the common–mode signal therefore reducing EME. These unwanted steps could be caused by an un–powered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal 0.5 x V_{CC} voltage.

Wakeup

When a valid wakeup (dominant state longer than t_{dbus}) is received during the standby mode the RxD pin is driven low. The wakeup detection is not latched: RxD returns to High state after t_{dbus} when the bus signal is released back to recessive - see Figure 4. Wake-up behavior in case of a permanent dominant - due to, for example, a bus short represents the only difference between the circuit functional sub-versions listed in the Ordering Information table. When the standby mode is entered while a dominant is present on the bus, the "unconditioned bus wake-up" versions will signal a bus-wakeup immediately after the state transition (signal RxD₁ in Figure 4). The other version will signal bus-wakeup only after the initial dominant is released (signal RxD₂ in Figure 4). In this way it's ensured, that a CAN bus can be put to a low-power mode even if the nodes have a level sensitivity to RxD pin and a permanent dominant is present on the bus.

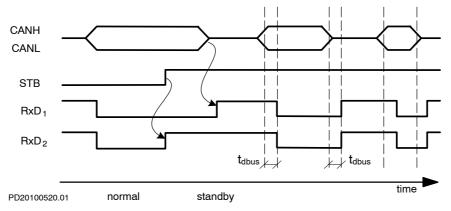


Figure 4. NCV7340 Wakeup Behavior

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off–state resets when the temperature decreases below the shutdown

threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on pin TxD exceeds the

internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant time–out time $(t_{dom(TxD)})$ defines the minimum possible bit rate to 40 kbps.

Fail Safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to

either positive or negative supply voltage, although power dissipation increases during this fault condition.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see Figure 5). Pins TxD and STB are pulled high internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the $V_{\rm CC}$ supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Absolute Maximum Ratings

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage		-0.3	+6	V
V _{CANH}	DC voltage at pin CANH	0 < V _{CC} < 5.25 V; no time limit	-50	+50	V
V _{CANL}	DC voltage at pin CANL	0 < V _{CC} < 5.25 V; no time limit	-50	+50	V
V _{SPLIT}	DC voltage at pin V _{SPLIT}	0 < V _{CC} < 5.25 V; no time limit	-40	+40	V
V_{TxD}	DC voltage at pin TxD		-0.3	6	V
V_{RxD}	DC voltage at pin RxD		-0.3	6	V
V_{STB}	DC voltage at pin STB		-0.3	6	V
V _{esd}	Electrostatic discharge voltage at all pins	Note 1 Note 2	-6 -500	6 500	kV V
	Electrostatic discharge voltage at CANH and CANL pins	Note 3	-12	12	kV
Latchup	Static latchup at all pins	Note 4		120	mA
T _{stg}	Storage temperature		-55	+150	°C
T _A	Ambient temperature		-40	+125	°C
TJ	Maximum junction temperature		-40	+170	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA–JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

Standardized charged device model ESD pulses when tested according to ESD-STM5.3.1–1999.

^{3.} System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.

^{4.} Static latchup immunity: Static latchup protection level when tested according to EIA/JESD78.

Table 5. CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = -40 to +150 °C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
SUPPLY (Pin V_C	c)					
I _{CC}	Supply current	Dominant; V _{TxD} = 0 V Recessive; V _{TxD} = V _{CC}		35 5	75 10	mA
I _{CCS}	Supply current in standby mode	T _{J,max} = 100°C		10	15	μΑ
TRANSMITTER	DATA INPUT (Pin TxD)					
V _{IH}	High-level input voltage	Output recessive	2.0	-	V _{CC}	V
V _{IL}	Low-level input voltage	Output dominant	-0.3	-	+0.8	V
I _{IH}	High-level input current	$V_{TxD} = V_{CC}$	-5	0	+5	μΑ
I _{IL}	Low-level input current	$V_{TxD} = 0 V$	-350	-200	-75	μΑ
C _i	Input capacitance	Not tested	-	5	10	pF
TRANSMITTER	MODE SELECT (Pin STB)					
V _{IH}	High-level input voltage	Standby mode	2.0	-	V _{CC}	V
V _{IL}	Low-level input voltage	Normal mode	-0.3	-	+0.8	V
I _{IH}	High-level input current	V _{STB} = V _{CC}	-5	0	+5	μΑ
I _{IL}	Low-level input current	V _{STB} = 0 V	-10	-4	-1	μΑ
C _i	Input capacitance	Not tested	-	5	10	pF
RECEIVER DATA	A OUTPUT (Pin RxD)					
l _{oh}	High-level output current	normal mode V _{RxD} = V _{CC} - 0.4 V	-1	-0.4	-0.1	mA
l _{ol}	Low-level output current	V _{RxD} = 0.4 V	2	6	12	mA
V _{oh}	High-level output voltage	standby mode I _{RxD} = -100 μA	V _{CC} – 1.1	V _{CC} – 0.7	V _{CC} – 0.4	V
BUS LINES (Pin	s CANH and CANL)					
Vo(reces) (norm)	Recessive bus voltage on pins CANH and CANL	V _{TxD} = V _{CC} ; no load normal mode	2.0	2.5	3.0	V
V _{o(reces)} (stby)	Recessive bus voltage on pins CANH and CANL	V _{TxD} = V _{CC} ; no load standby mode	-100	0	100	mV
I _{o(reces)} (CANH)	Recessive output current at pin CANH	-35 V < V _{CANH} < +35 V; 0 V < V _{CC} < 5.25 V	-2.5	-	+2.5	mA
I _{o(reces)} (CANL)	Recessive output current at pin CANL	-35 V < V _{CANL} < +35 V; 0 V < V _{CC} < 5.25 V	-2.5	-	+2.5	mA
I _{LI(CANH)}	Input leakage current to pin CANH	V _{CC} = 0 V V _{CANL} = V _{CANH} = 5 V	-10	0	10	μΑ
I _{LI(CANL_}	Input leakage current to pin CANL	V _{CC} = 0 V V _{CANL} = V _{CANH} = 5 V	-10	0	10	μΑ
V _{o(dom)} (CANH)	Dominant output voltage at pin CANH	V _{TxD} = 0 V	3.0	3.6	4.25	V
V _{o(dom) (CANL)}	Dominant output voltage at pin CANL	V _{TxD} = 0 V	0.5	1.4	1.75	V
Vo(dif) (bus_dom)	Differential bus output voltage (V _{CANH} – V _{CANL})	V_{TxD} = 0 V; dominant; 42.5 Ω < R _{LT} < 60 Ω	1.5	2.25	3.0	V
Vo(dif) (bus_rec)	Differential bus output voltage (V _{CANH} – V _{CANL})	V _{TxD} = V _{CC} ; recessive; no load	-120	0	+50	mV
I _{o(sc)} (CANH)	Short circuit output current at pin CANH	V _{CANH} = 0 V; V _{TxD} = 0 V	-120	-70	-45	mA
I _{o(sc)} (CANL)	Short circuit output current at pin CANL	V _{CANL} = 36 V; V _{TxD} = 0 V	45	70	120	mA
V _{i(dif) (th)}	Differential receiver threshold voltage (see Figure 6)	-5 V < V _{CANL} < +12 V; -5 V < V _{CANH} < +12 V;	0.5	0.7	0.9	V
V _{ihcm(dif)} (th)	Differential receiver threshold voltage for high common–mode (see Figure 6)	-35 V < V _{CANL} < +35 V; -35 V < V _{CANH} < +35 V;	0.40	0.7	1.0	V

Table 5. CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = -40 to +150°C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter Conditions		Min	Тур	Max	Unit
BUS LINES (Pin	s CANH and CANL)	•			•	
V _{i(dif)} (th)_STDBY	Differential receiver threshold voltage in standby mode (see Figure 6)	-12 V < V _{CANL} < +12 V; -12 V < V _{CANH} < +12 V;	0.4	0.8	1.15	V
R _{i(cm) (CANH)}	Common-mode input resistance at pin CANH		15	26	37	kΩ
R _{i(cm) (CANL)}	Common-mode input resistance at pin CANL		15	26	37	kΩ
R _{i(cm) (m)}	Matching between pin CANH and pin CANL common mode input resistance	V _{CANH} = V _{CANL}	-3	0	+3	%
R _{i(dif)}	Differential input resistance		25	50	75	kΩ
C _{i(CANH)}	Input capacitance at pin CANH	V _{TxD} = V _{CC} ; not tested		7.5	20	pF
C _{i(CANL)}	Input capacitance at pin CANL	V _{TxD} = V _{CC} ; not tested		7.5	20	pF
C _{i(dif)}	Differential input capacitance	V _{TxD} = V _{CC} ; not tested		3.75	10	pF
COMMON-MOD	E STABILIZATION (Pin V _{SPLIT})					
V _{SPLIT}	Reference output voltage at pin V _{SPLIT}	Normal mode; -500 μA < I _{SPLIT} < 500 μA	0.3 x V _{CC}	_	0.7 x V _{CC}	
I _{SPLIT(i)}	V _{SPLIT} leakage current	Standby mode	-5		+5	μΑ
I _{SPLIT(lim)}	V _{SPLIT} limitation current Normal mode		1.3		5	mA
THERMAL SHU	rdown					
$T_{J(sd)}$	Shutdown junction temperature	junction temperature rising	150	160	185	°C
TIMING CHARA	CTERISTICS (see Figures 7 and 8)					
t _{d(TxD-BUSon)}	Delay TxD to bus active	C _I = 100 pF between CANH to CANL	20	85	105	ns
t _d (TxD-BUSoff)	Delay TxD to bus inactive	C _I = 100 pF between CANH to CANL	30	60	105	ns
t _{d(BUSon-RXD)}	Delay bus active to RxD	C _{rxd} = 15 pF	25	55	105	ns
t _{d(BUSoff-RXD)}	Delay bus inactive to RxD	C _{rxd} = 15 pF	30	100	105	ns
t _{pd(rec-dom)}	Propagation delay TxD to RxD from recessive to dominant	C _I = 100 pF between CANH to CANL	75		230	ns
t _{d(dom-rec)}	Propagation delay TxD to RxD from dominant to recessive	C _I = 100 pF between CANH to CANL	75		245	ns
t _{d(stb-nm)}	Delay standby mode to normal mode		5	7.5	10	μs
t _{dbus}	Dominant time for wakeup via bus	$V_{dif(dom)} > 1.4 V$	0.75	2.5	5	μs
		V _{dif(dom)} > 1.2 V	0.75	3	5.8	μs
t _{dom(TxD)}	TxD dominant time for time out	V _{TxD} = 0 V	300	650	1000	μs

MEASUREMENT SETUPS AND DEFINITIONS

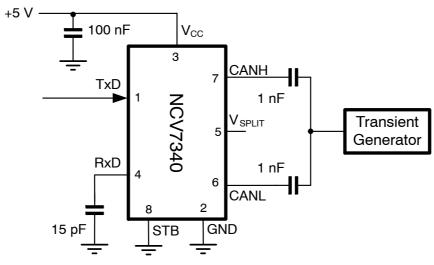


Figure 5. Test Circuit for Automotive Transients

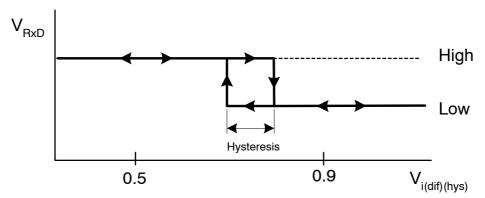


Figure 6. Hysteresis of the Receiver

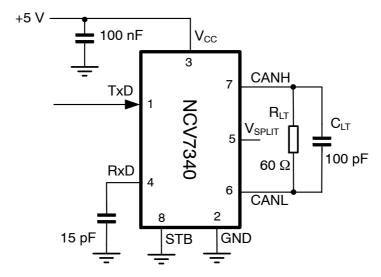


Figure 7. Test Circuit for Timing Characteristics

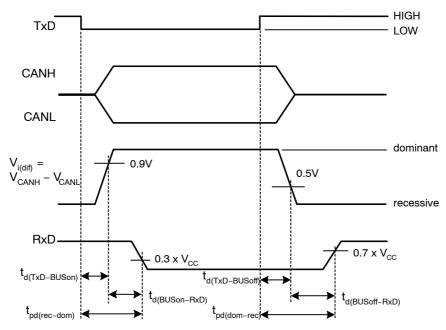


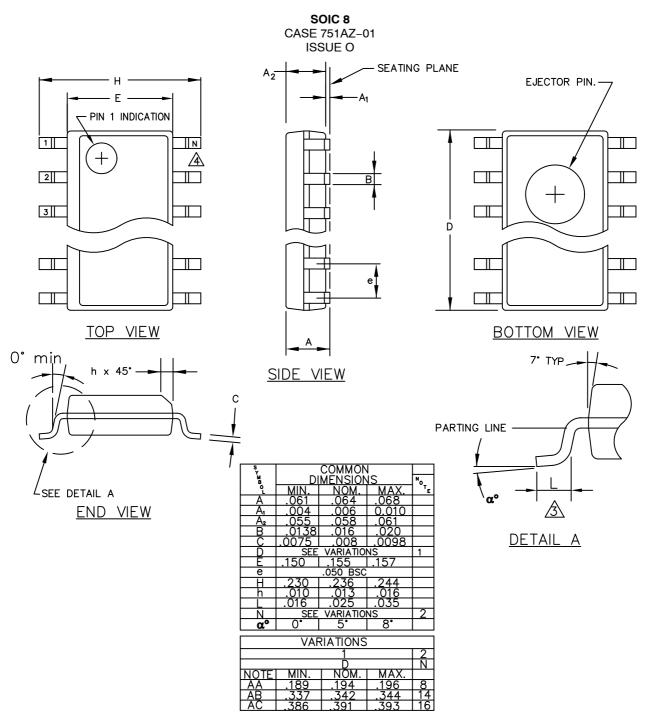
Figure 8. Timing Diagram for AC Characteristics

DEVICE ORDERING INFORMATION

Part Number	Description	Temperature Range	Package Type	Shipping [†]
NCV7340D12G	HS LP CAN Transceiver			96 Tube / Tray
NCV7340D12R2G	(Unconditioned Bus Wakeup)	1,	SOIC 150 8 (Mate Sn, JEDEC	3000 / Tape & Reel
NCV7340D14G	HS LP CAN Transceiver (Bus Wakeup Inactive in	−40°C to +125°C	MS-012) (Pb-Free)	96 Tube / Tray
NCV7340D14R2G	Case of Bus Fault)			3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



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