ON Semiconductor®

FSGM300N
Green-Mode Power Switch

Features

- Advanced Burst-Mode Operation for Low Standby Power
- Random Frequency Fluctuation for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis
- Auto-Restart Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650V
- Built-in Soft-Start: 15ms

Applications

- Power Supply for LCD Monitor, STB and DVD Combination

Description

The FSGM300N is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSGM series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Ordering Information

Part Number	Package	Operating Junction Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Output Power Table[2]				Replaces Device
					$230V_{AC} \pm 15\%$[3]		$85\text{-}265V_{AC}$		
					Adapter[4]	Open Frame[5]	Adapter[4]	Open Frame[5]	
FSGM300N	8-DIP	−40°C ~ +125°C	1.60A	2.2Ω	26W	40W	20W	30W	FSFM300N

Notes:
1. Pb-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. $230V_{AC}$ or $100/115V_{AC}$ with voltage doubler.
4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Application Circuit

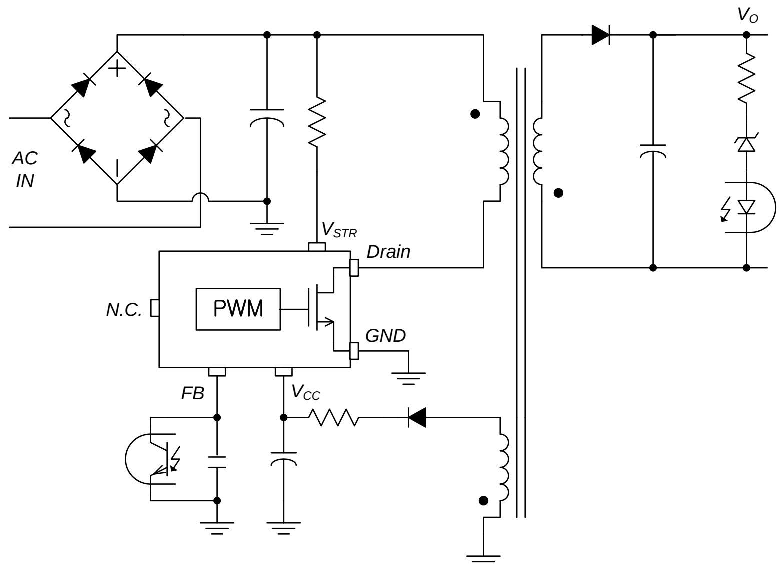


Figure 1. Typical Application Circuit

Internal Block Diagram

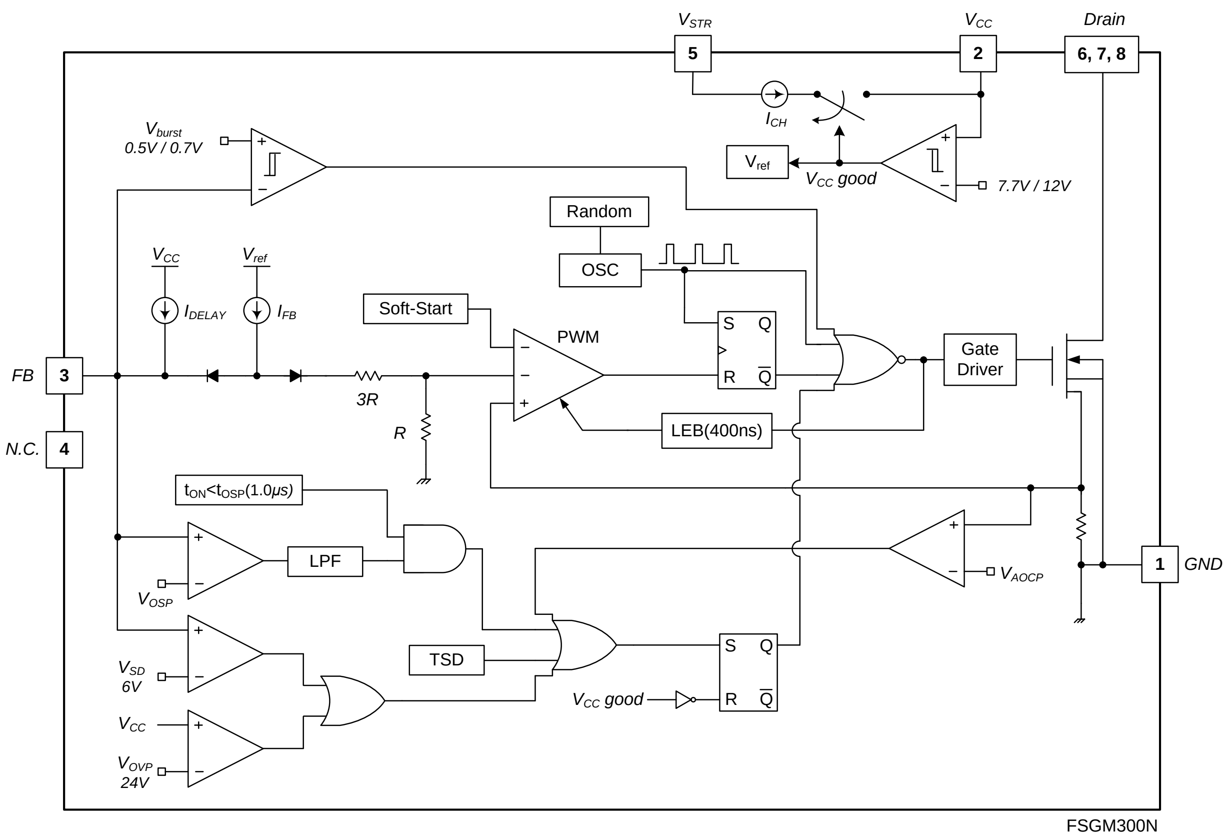


Figure 2. Internal Block Diagram

Pin Configuration

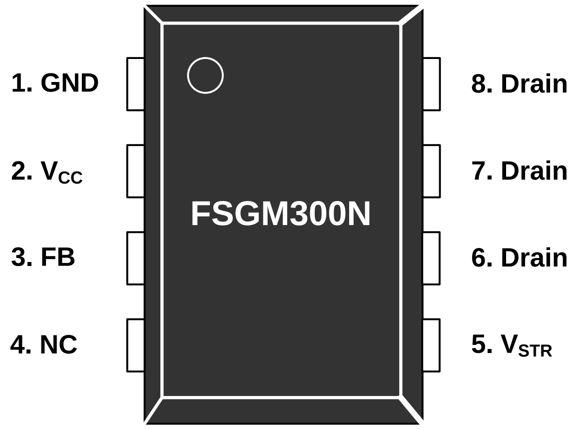


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is the control ground and the SenseFET source.
2	V_{CC}	**Power Supply**. This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
3	FB	**Feedback**. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the power switch.
4	NC	No Connection.
5	V_{STR}	**Startup**. This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source (I_{CH}) is disabled.
6, 7, 8	Drain	**SenseFET Drain.** High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage		650	V
V_{DS}	Drain Pin Voltage		650	V
V_{CC}	V_{CC} Pin Voltage		26	V
V_{FB}	Feedback Pin Voltage	−0.3	8.0	V
I_{DM}	Drain Current Pulsed		4	A

I_{DS}	Continuous Switching Drain Current[6]	T_C=25°C		1.90	A
		T_C=100°C		1.27	A
E_{AS}	Single Pulsed Avalanche Energy[7]			190	mJ
P_D	Total Power Dissipation (T_C=25°C)[8]			1.5	W
T_J	Maximum Junction Temperature			150	°C
	Operating Junction Temperature[9]		−40	+125	°C
T_{STG}	Storage Temperature		−55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2		kV
		Charged Device Model, JESD22-C101	2		

Notes:

6. Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX}=0.83) and junction temperature *(see Figure 4)*.
7. L=45mH, starting T_J=25°C.
8. Infinite cooling condition *(refer to the SEMI G30-88)*.
9. Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

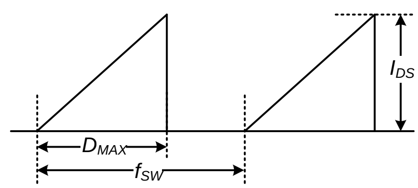


Figure 4. Repetitive Peak Switching Current

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance[10]	80	°C/W
θ_{JC}	Junction-to-Case Thermal Impedance[11]	20	°C/W
Ψ_{JT}	Junction-to-Top Thermal Impedance[12]	35	

Notes:

10. Infinite cooling condition *(refer to the SEMI G30-88)*.
11. Free standing with no heat-sink under natural convection.
12. Measured on the package top surface.

Electrical Characteristics

T_J=25°C unless otherwise specified.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
SenseFET Section							
BV_{DSS}	Drain-Source Breakdown Voltage		V_{CC}=0V, I_D=250μA	650			V
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS}=520V, T_A=125°C			250	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance		V_{GS}=10V, I_D=1A		1.8	2.2	Ω
C_{ISS}	Input Capacitance(13)		V_{DS}=25V, V_{GS}=0V, f=1MHz		515		pF
C_{OSS}	Output Capacitance(13)		V_{DS}=25V, V_{GS}=0V, f=1MHz		75		pF
t_r	Rise Time		V_{DS}=325V, I_D=4A, R_G=25Ω		26		ns
t_f	Fall Time		V_{DS}=325V, I_D=4A, R_G=25Ω		25		ns
$t_{d(on)}$	Turn-On Delay Time		V_{DS}=325V, I_D=4A, R_G=25Ω		14		ns
$t_{d(off)}$	Turn-Off Delay Time		V_{DS}=325V, I_D= 4A, R_G=25Ω		32		ns
Control Section							
f_S	Switching Frequency(13)		V_{CC}=14V, V_{FB}=4V	61	67	73	kHz
Δf_S	Switching Frequency Variation(13)		−25°C < T_J < 125°C		±5	±10	%
D_{MAX}	Maximum Duty Ratio		V_{CC}=14V, V_{FB}=4V	71	77	83	%
D_{MIN}	Minimum Duty Ratio		V_{CC}=14V, V_{FB}=0V			0	%
I_{FB}	Feedback Source Current		V_{FB}=0	120	150	180	μA
V_{START}	UVLO Threshold Voltage		V_{FB}=0V, V_{CC} Sweep	11	12	13	V
V_{STOP}			After Turn-on, V_{FB}=0V	7.0	7.7	8.5	V
V_{OP}	V_{CC} Operating Range			13		22.5	V
$t_{S/S}$	Internal Soft-Start Time		V_{STR}=40V, V_{CC} Sweep		15		ms
Burst-Mode Section							
V_{BURH}	Burst-Mode Voltage		V_{CC}=14V, V_{FB} Sweep	0.6	0.7	0.8	V
V_{BURL}				0.4	0.5	0.6	V
Hys					200		mV
Protection Section							
I_{LIM}	Peak Drain Current Limit		di/dt=300mA/μs	1.44	1.60	1.76	A
V_{SD}	Shutdown Feedback Voltage		V_{CC}=14V, V_{FB} Sweep	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{CC}=14V, V_{FB}=4V	2.0	2.7	3.4	μA
t_{LEB}	Leading-Edge Blanking Time(13)(15)				400		ns
V_{OVP}	Over-Voltage Protection		V_{CC} Sweep	22.5	24.0	25.5	V
t_{OSP}	Output-Short Protection(13)	Threshold Time	OSP Triggered when t_{ON}<t_{OSP} & V_{FB}>V_{OSP} (Lasts Longer than t_{OSP_FB})	0.7	1.0	1.3	μs
V_{OSP}		Threshold V_{FB}		1.4	1.6	1.8	V
t_{OSP_FB}		V_{FB} Blanking Time		2.0	2.5	3.0	μs

T_{SD}	Thermal Shutdown Temperature[13]	Shutdown Temperature	125	135	145	°C
Hys		Hysteresis		40		°C

Continued on the following page…

Electrical Characteristics (Continued)

T_J=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Section						
I_{OP}	Operating Supply Current, (Control Part in Burst Mode)	V_{CC}=14V, V_{FB}=0V	1.0	1.5	2.0	mA
I_{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V_{CC}=14V, V_{FB}=2V	2.1	2.5	2.9	mA
I_{START}	Start Current	V_{CC}=11V (Before V_{CC} Reaches V_{START})	400	500	600	μA
I_{CH}	Startup Charging Current	V_{CC}=V_{FB}=0V, V_{STR}=40V	0.95	1.10	1.25	mA
V_{STR}	Minimum V_{STR} Supply Voltage	V_{CC}=V_{FB}=0V, V_{STR} Sweep		26		V

Notes:

13. Although these parameters are guaranteed, they are not 100% tested in production.
14. Average value
15. t_{LEB} includes gate turn-on time.

Comparison of FSFM300N and FSGM300N

Function	FSFM300N	FSGM300N	Advantages of FSGM300N
Random Frequency Fluctuation		Built-in	Low EMI
Operating Current	3mA	1.4mA	Very low stand-by power
Protections	OLP OVP AOCP TSD	OLP OVP OSP AOCP TSD with Hysteresis	Enhanced protections and high reliability
Power Balance	Long T_{CLD}	Very Short T_{CLD}	The difference of input power between the low and high input voltage is quite small

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

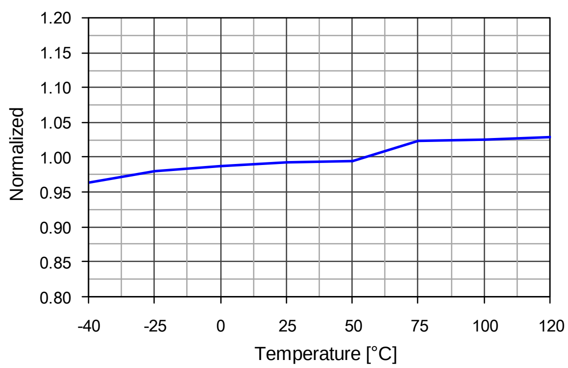


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

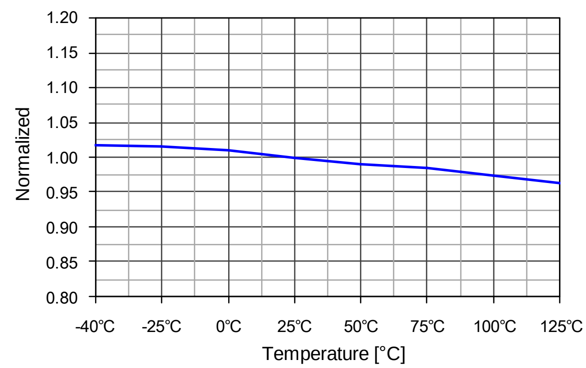


Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

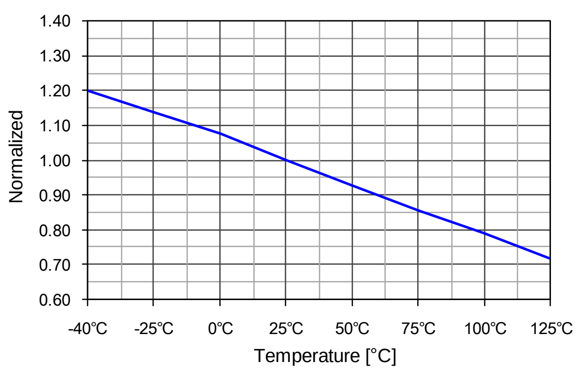


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

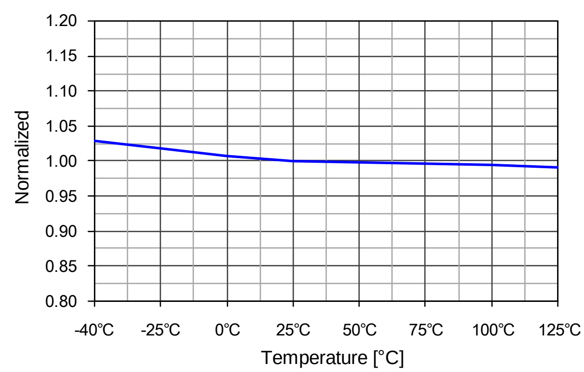


Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

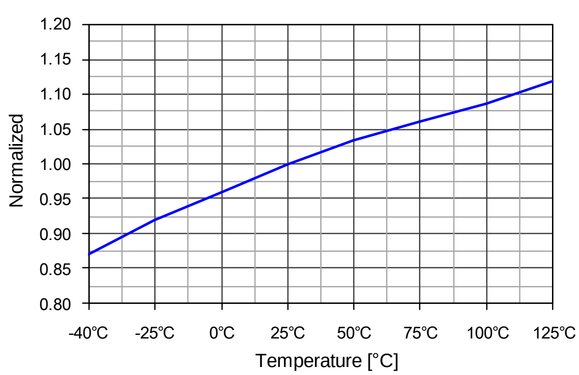


Figure 9. Feedback Source Current (I_{FB}) vs. T_A

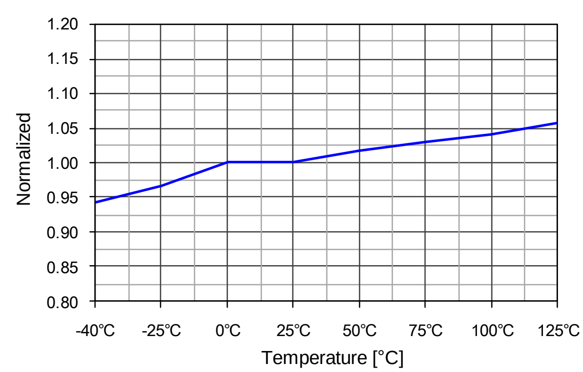


Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at T_A=25°C.

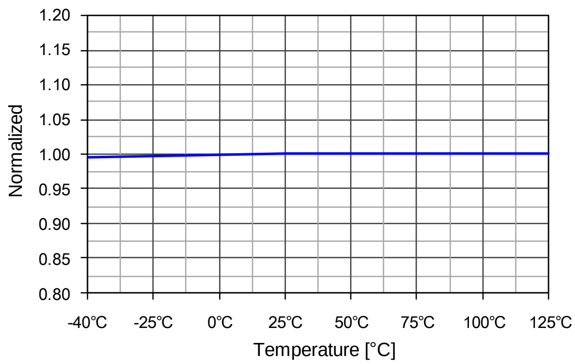


Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

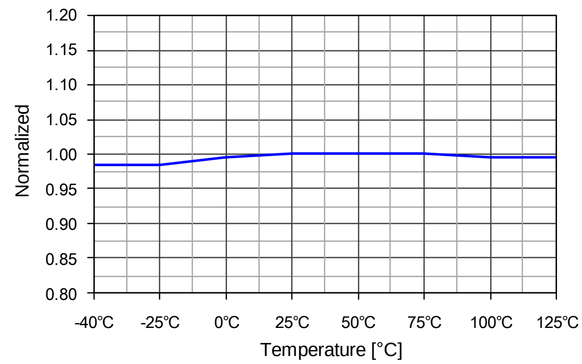


Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

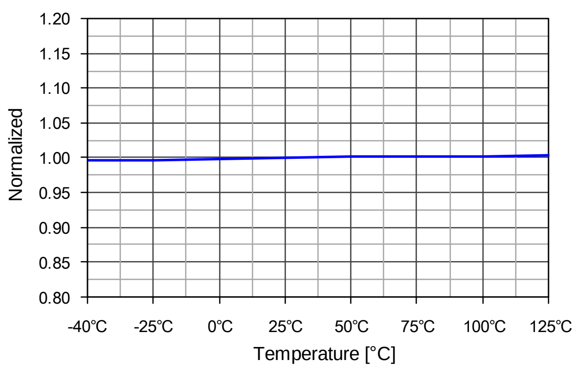


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

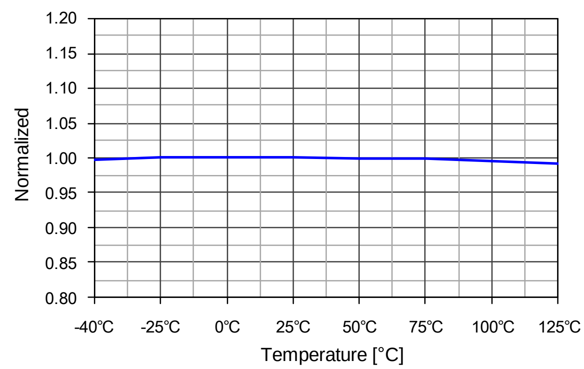


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

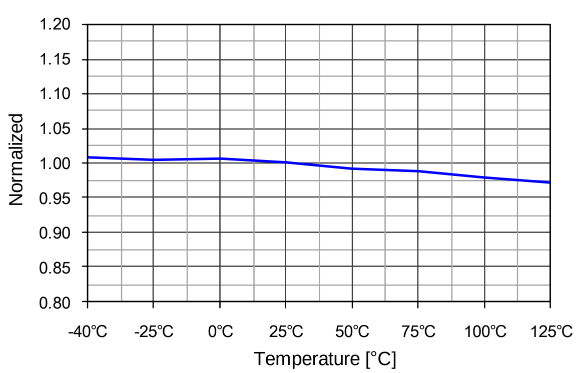


Figure 15. Switching Frequency (f_S) vs. T_A

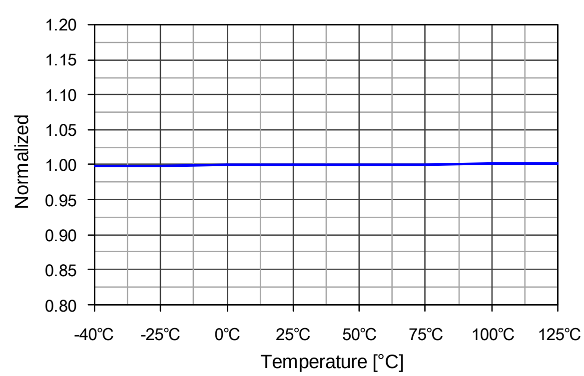


Figure 16. Maximim Duty Ratio (D_{MAX}) vs. T_A

Functional Description

1. Startup: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_{Vcc}) connected to the V_{CC} pin, as illustrated in Figure 17. When V_{CC} reaches 12V, the FSGM300N begins switching and the internal high-voltage current source is disabled. The FSGM300N continues normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 7.7V.

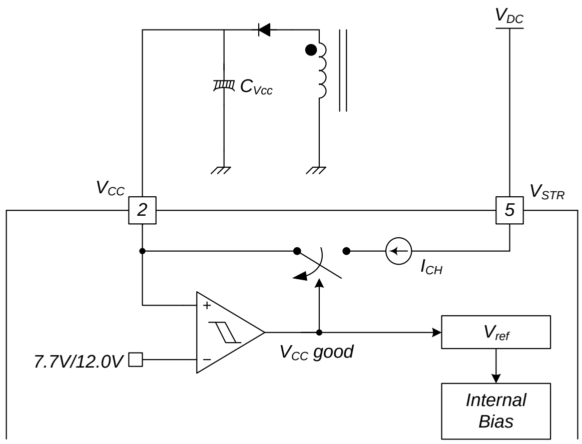


Figure 17. Startup Block

2. Soft-Start: The FSGM300N has an internal soft-start circuit that increases PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

3. Feedback Control: This device employs current-mode control, as shown in Figure 18. An opto-coupler (such as the FOD817) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing drain current. This typically occurs when the input voltage is increased or the output load is decreased.

3.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 18. Assuming that the 150μA current source flows only through the internal resistor (3R + R =16kΩ), the cathode voltage of diode D2 is about 2.4V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.4V, the maximum voltage of the cathode of D2 is clamped at this voltage. Therefore, the peak value of the current through the SenseFET is limited.

3.2 Leading-Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike usually occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor leads to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSGM300N employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for t_{LEB} (400ns) after the SenseFET is turned on.

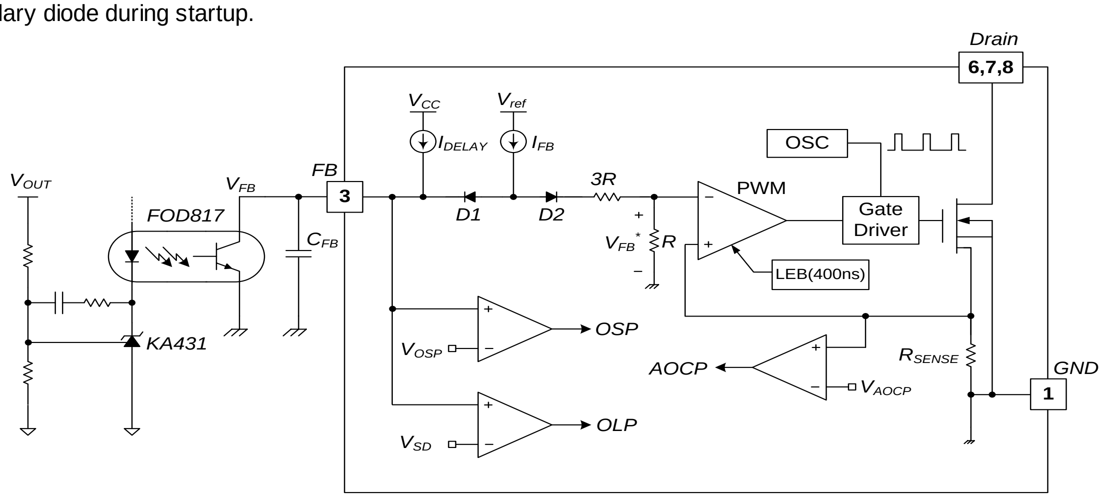


Figure 18. Pulse Width Modulation Circuit

4. Protection Circuits: The FSGM300N has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.7V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSGM300N resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

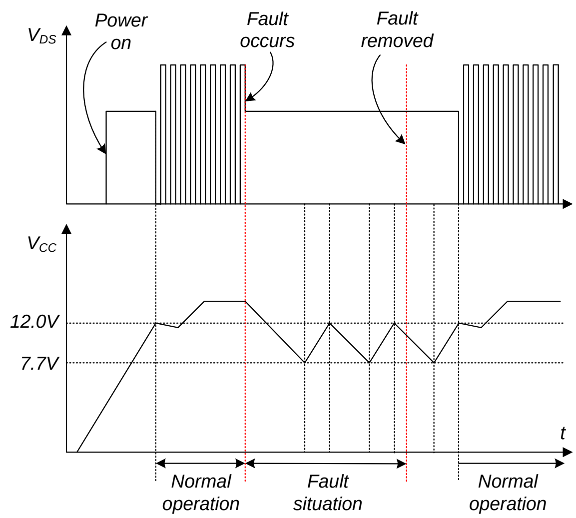


Figure 19. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.4V, D1 is blocked and the 2.7μA current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues increasing until it reaches 6.0V, when the switching operation is terminated, as shown in Figure 20. The delay time for shutdown is the time required to charge C_{FB} from 2.4V to 6.0V with 2.7μA. A 25 ~ 50ms delay is typical for most applications. This protection is implemented in auto-restart mode.

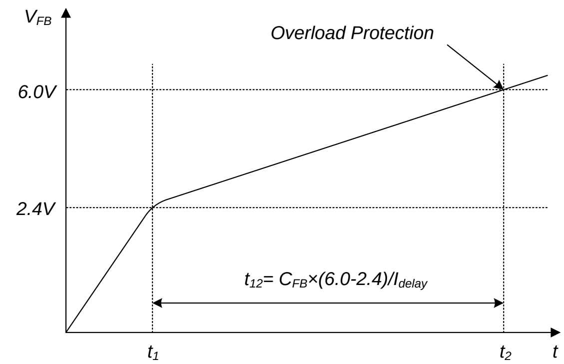


Figure 20. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSGM300N has overload protection, it is not enough to protect the FSGM300N in that abnormal case; since severe current stress is imposed on the SenseFET until OLP is triggered. The FSGM300N internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S−R latch, resulting in the shutdown of the SMPS.

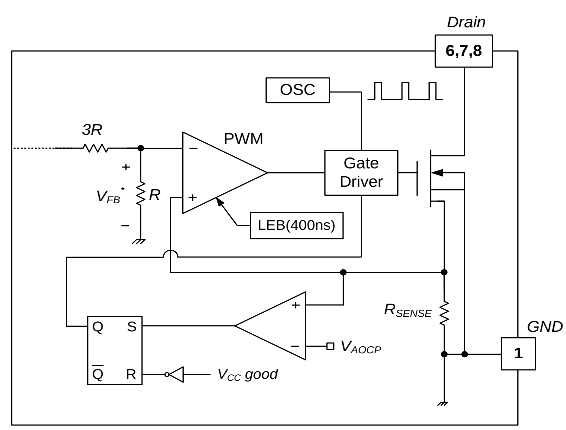


Figure 21. Abnormal Over-Current Protection

4.3. Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 1.6V and the SenseFET turn-on time is lower than 1.0μs, the FSGM300N recognizes this condition as an abnormal error and shuts down PWM switching until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.

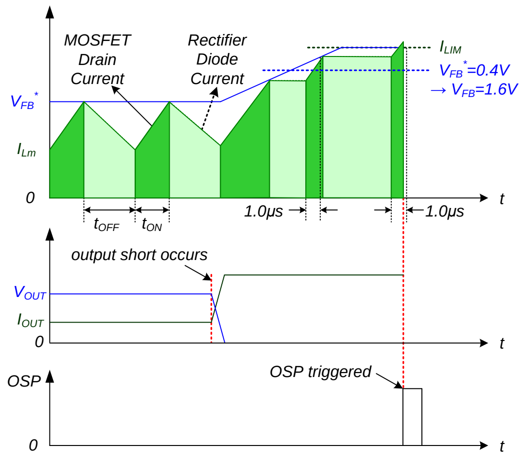


Figure 22. Output-Short Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSGM300N uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.0V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.0V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SenseFET. If the temperature exceeds ~135°C, the thermal shutdown is triggered and stops operation. The FSGM300N operates in auto-restart mode until the temperature decreases to around 95°C, when normal operation resumes.

5. Soft Burst-Mode Operation: To minimize power dissipation in standby mode, the FSGM300N enters burst-mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (500mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (700mV), switching resumes. The feedback voltage then falls and the process repeats. Burst-mode operation alternately enables and disables switching of the SenseFET, thereby reducing switching loss in standby mode.

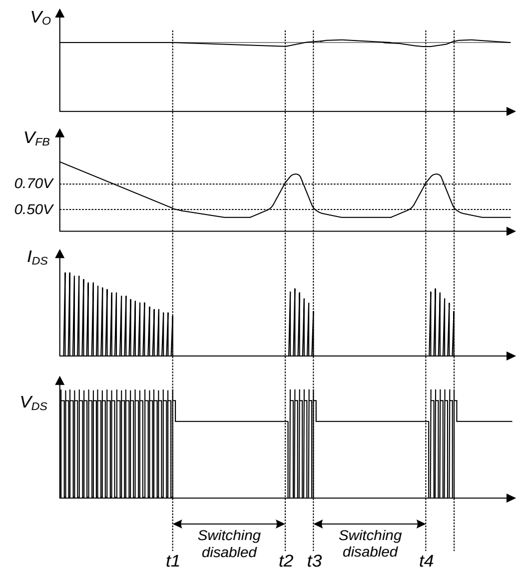


Figure 23. Burst-Mode Operation

6. Random Frequency Fluctuation (RFF): Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and internal free-running oscillator at every switching instant. This Random Frequency Fluctuation scatters the EMI noise around typical switching frequency (67kHz) effectively and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

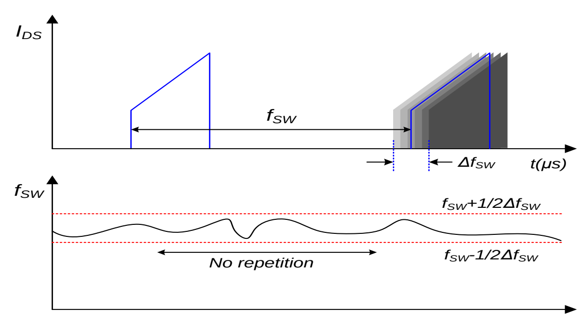


Figure 24. Random Frequency Fluctuation

Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
LCD Monitor Power Supply	85 ~ 265V$_{AC}$	5.0V(2A) 14.0V(1.2A)	26.8W

Key Design Notes:

1. The delay time for overload protection is designed to be about 30ms with C105 (22nF). OLP time between 25ms (18nF) and 50ms (39nF) is recommended.
2. The SMD-type capacitor (C106) must be placed as close as possible to the V$_{CC}$ pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100nF and 220nF is recommended.

1. Schematic

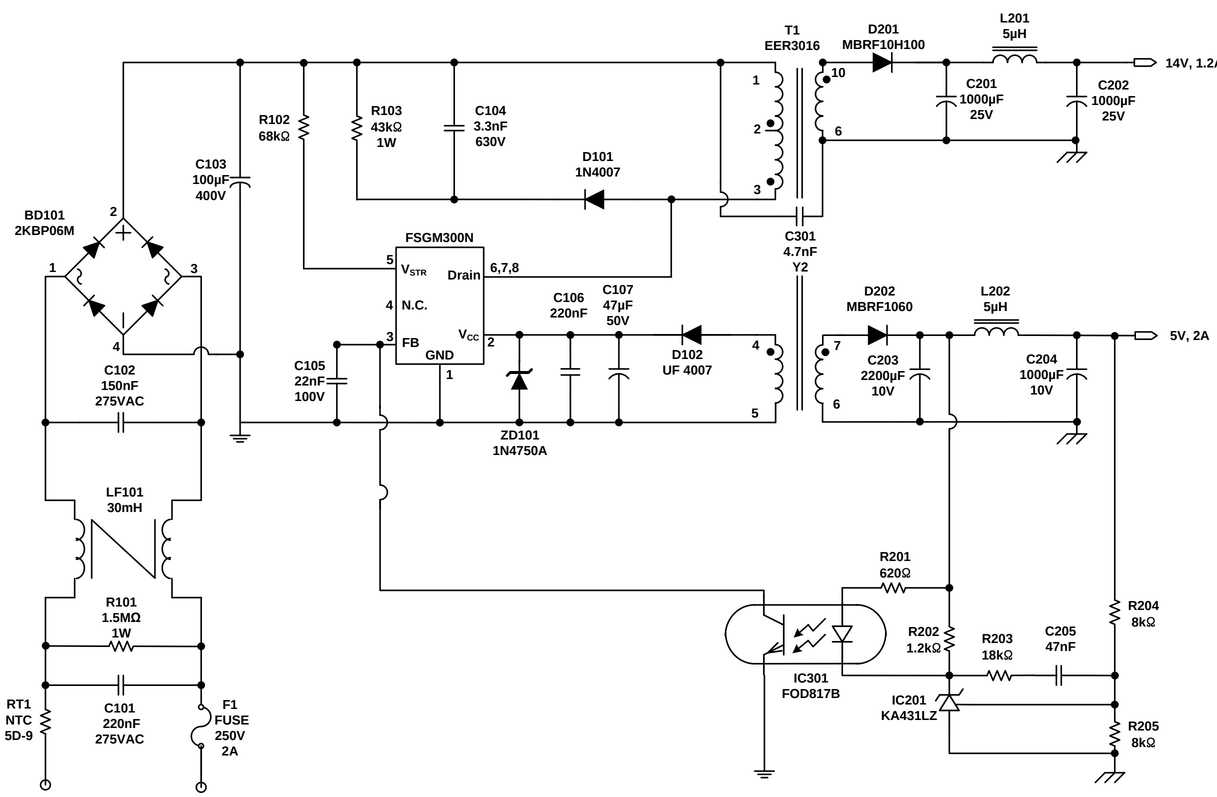


Figure 25. Schematic of Demonstration Board

2. Transformer

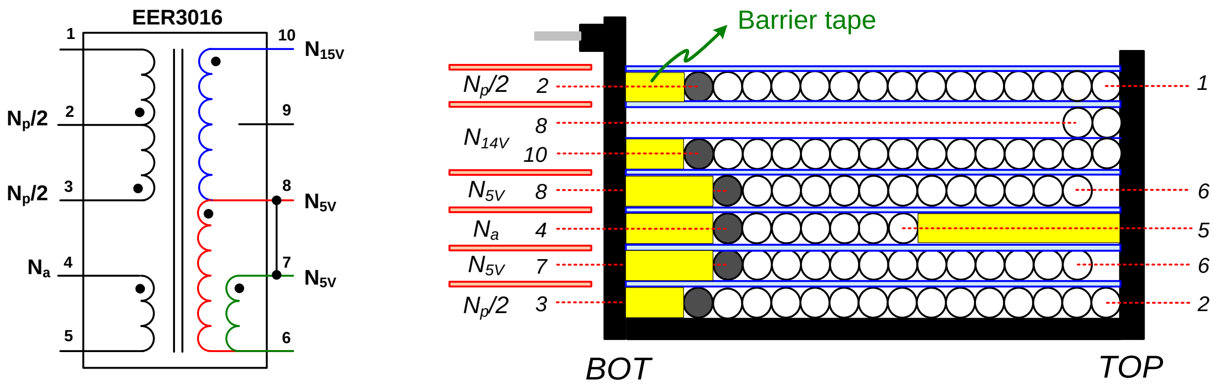


Figure 26. Schematic of Transformer

3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method	Barrier Tape		
					TOP	BOT	Ts
$N_p/2$	3 → 2	0.25φ×1	21	Solenoid Winding		2.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							
N_{5V}	7 → 6	0.4φ×2 (TIW)	3	Solenoid Winding		3.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							
N_a	4 → 5	0.2φ×1	7	Solenoid Winding	4.0mm	3.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							
N_{5V}	8 → 6	0.4φ×2 (TIW)	3	Solenoid Winding		3.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							
N_{14V}	10 → 8	0.4φ×2 (TIW)	5	Solenoid Winding		2.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							
$N_p/2$	2 → 1	0.25φ×1	21	Solenoid Winding		2.0mm	1
Insulation: Polyester Tape t=0.025mm, 2 Layers							

4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1 - 3	900μH ± 6%	67kHz, 1V
Leakage	1 - 3	15μH Maximum	Short All Other Pins

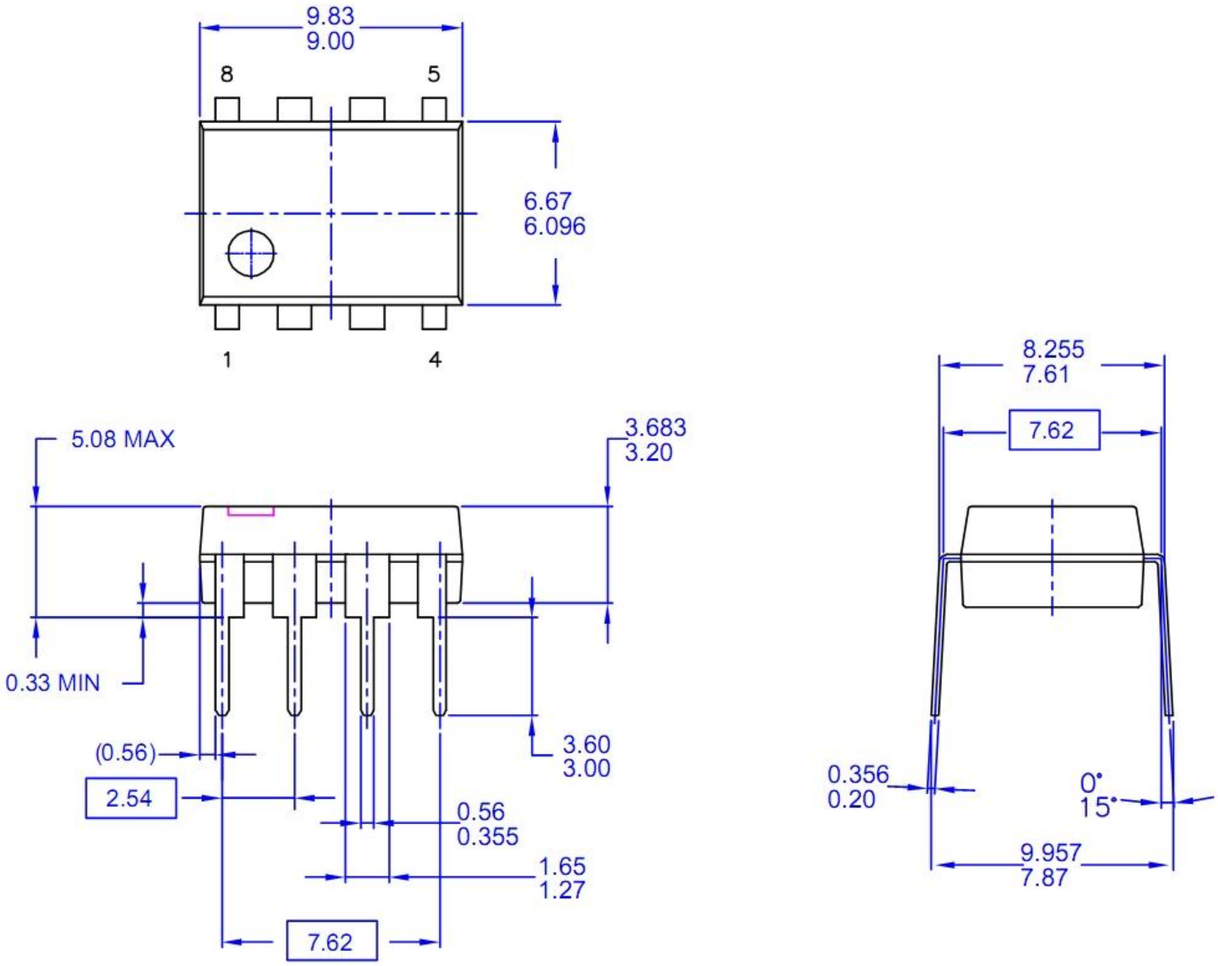
5. Core & Bobbin

- Core: EER3016 (A_e=109.7mm^2)
- Bobbin: EER3016

6. Bill of Materials

Part #	Value	Note	Part #	Value	Note
Fuse			**Capacitor**		
F101	250V 2A		C101	220nF/275V	Box (Pilkor)
NTC			C102	150nF/275V	Box (Pilkor)
NTC101	5D-9	DSC	C103	100µF/400V	Electrolytic (SamYoung)
Resistor			C104	3.3nF/630V	Film (Sehwa)
R101	1.5MΩ, J	1W	C105	22nF/100V	Film (Sehwa)
R102	68kΩ, J	1/2W	C106	220nF	SMD (2012)
R103	43kΩ, J	1W	C107	47µF/50V	Electrolytic (SamYoung)
R201	620Ω, F	1/4W, 1%	C201	1000µF/25V	Electrolytic (SamYoung)
R202	1.2kΩ, F	1/4W, 1%	C202	1000µF/25V	Electrolytic (SamYoung)
R203	18kΩ, F	1/4W, 1%	C203	2200µF/10V	Electrolytic (SamYoung)
R204	8kΩ, F	1/4W, 1%	C204	1000µF/16V	Electrolytic (SamYoung)
R205	8kΩ, F	1/4W, 1%	C205	47nF/100V	Film (Sehwa)
			C301	4.7nF/Y2	Y-cap (Samhwa)
IC			**Inductor**		
FSGM300N	FSGM300N	ON Semiconductor	LF101	30mH	Line filter 0.5Ø
IC201	KA431LZ	ON Semiconductor	L201	5µH	5A Rating
IC301	FOD817B	ON Semiconductor	L202	5µH	5A Rating
Diode			**Transformer**		
D101	1N4007	Vishay	T101	900µH	
D102	UF4007	Vishay			
ZD101	1N4750	Vishay			
D201	MBRF10H100	ON Semiconductor			
D202	MBRF1060	ON Semiconductor			
BD101	2KBP06	Vishay			

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 27. 8 Lead Dual Inline Package (DIP)

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