FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD
SEMICONDUCTOR®

October 2013

FDPC8016S

PowerTrench® Power Clip
25V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 3.8 mΩ at V_{GS} = 10 V, I_D = 20 A

- Max $r_{DS(on)}$ = 4.7 mΩ at V_{GS} = 4.5 V, I_D = 18 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.4 mΩ at V_{GS} = 10 V, I_D = 35 A

- Max $r_{DS(on)}$ = 1.7 mΩ at V_{GS} = 4.5 V, I_D = 32 A

- Low inductance packaging shortens rise/fall times, resulting in lower switching losses

- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing

- RoHS Compliant

General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing

- Communications

- General Purpose Point of Load

Top   **Power Clip 5X6**   **Bottom**
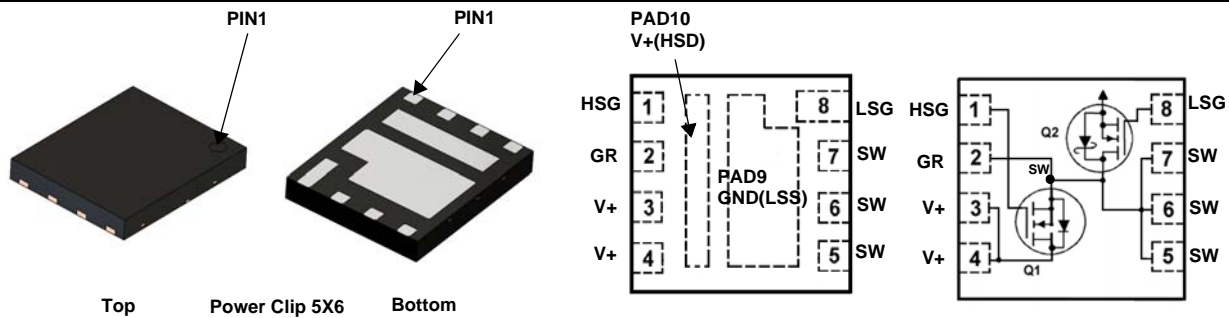
Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DS}	Drain to Source Voltage		25[Note5]	25	V
V_{GS}	Gate to Source Voltage		±12	±12	V
I_D	Drain Current -Continuous	T_C = 25 °C	60	100	A
	-Continuous	T_A = 25 °C	20[Note1a]	35[Note1b]	
	-Pulsed	T_A = 25 °C (Note 4)	75	140	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	73	216	mJ
P_D	Power Dissipation for Single Operation	T_C = 25 °C	21	42	W
	Power Dissipation for Single Operation	T_A = 25 °C	2.1[Note1a]	2.3[Note1b]	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		6.0	3.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		60[Note1a]	55[Note1b]	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		130[Note1c]	120[Note1d]	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
05OD/15OD	FDPC8016S	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	25 25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		24 28		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V V_{DS} = 20 V, V_{GS} = 0 V	Q1 Q2			1 500	µA µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 12 V/-8 V, V_{DS}= 0 V V_{GS} = 12 V/-8 V, V_{DS}= 0 V	Q1 Q2			±100 ±100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	0.8 1.1	1.3 1.5	2.5 2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C I_D = 10 mA, referenced to 25 °C	Q1 Q2		-4 -3		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 20 A V_{GS} = 4.5 V, I_D = 18 A V_{GS} = 10 V, I_D = 20 A,T_J =125 °C	Q1		2.8 3.4 3.9	3.8 4.7 5.3	mΩ
		V_{GS} = 10V, I_D = 35 A V_{GS} = 4.5 V, I_D = 32 A V_{GS} = 10 V, I_D = 35 A ,T_J =125 °C	Q2		1.1 1.3 1.5	1.4 1.7 1.9	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 20 A V_{DS} = 5 V, I_D = 35 A	Q1 Q2		182 241		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ Q2: V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2		1695 4715	2375 6600	pF
C_{oss}	Output Capacitance		Q1 Q2		495 1195	710 1675	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		54 159	100 290	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.4 0.5	1.2 1.5	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 13 V, I_D = 20 A, R_{GEN} = 6 Ω Q2: V_{DD} = 13 V, I_D = 35 A, R_{GEN} = 6 Ω		Q1 Q2		8 13	16 24	ns
t_r	Rise Time			Q1 Q2		2 4	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time			Q1 Q2		24 38	38 61	ns
t_f	Fall Time			Q1 Q2		2 3	10 10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1 V_{DD} = 13 V, I_D = 20 A Q2 V_{DD} = 13 V, I_D = 35 A	Q1 Q2		25 67	35 94	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V		Q1 Q2		11 31	16 44	nC
Q_{gs}	Gate to Source Gate Charge			Q1 Q2		3.4 10		nC
Q_{gd}	Gate to Drain "Miller" Charge			Q1 Q2		2.2 6.3		nC

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A (Note 2) V_{GS} = 0 V, I_S = 35 A (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 20 A, di/dt = 100 A/μs	Q1 Q2		25 33	40 53	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 35 A, di/dt = 200 A/μs	Q1 Q2		10 31	20 50	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
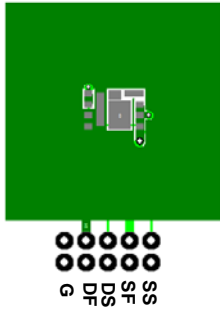
a. 60 °C/W when mounted on a 1 in^2 pad of 2 oz copper
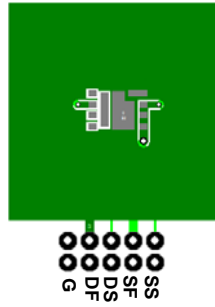
b. 55 °C/W when mounted on a 1 in^2 pad of 2 oz copper
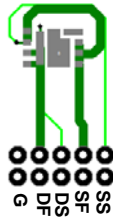
c. 130 °C/W when mounted on a minimum pad of 2 oz copper
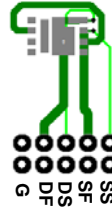
d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Q1 :E_{AS} of 73 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 7 A, V_{DD} = 30 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 24 A.
   Q2: E_{AS} of 216 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 12 A, V_{DD} = 25 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 39 A.

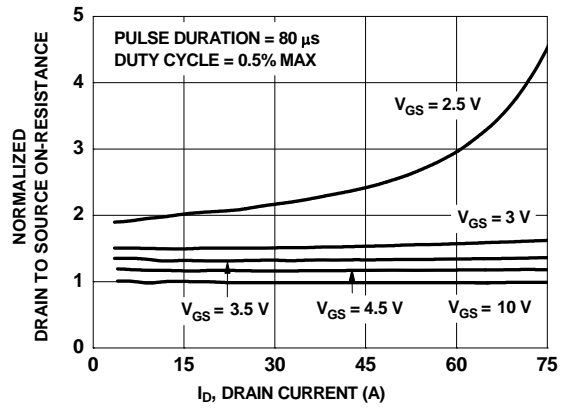4. Pulsed Id limited by junction temperature, td<=10 us. Please refer to SOA curve for more details.

5. The continuous V_{DS} rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.
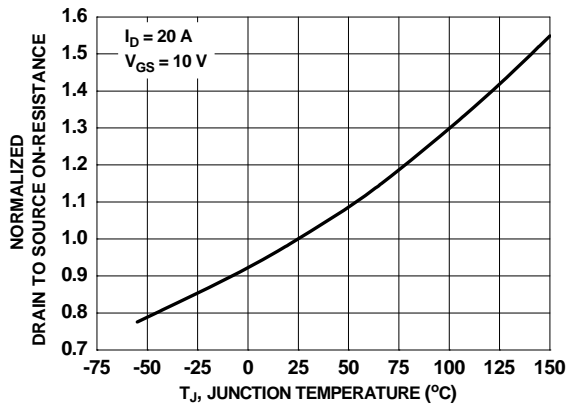
Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted
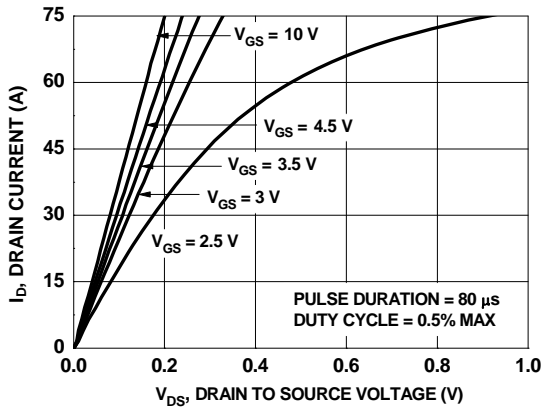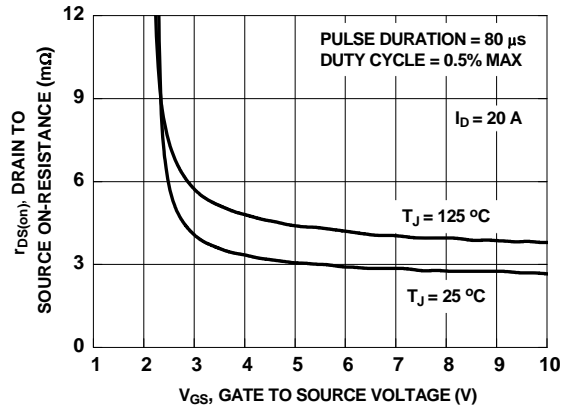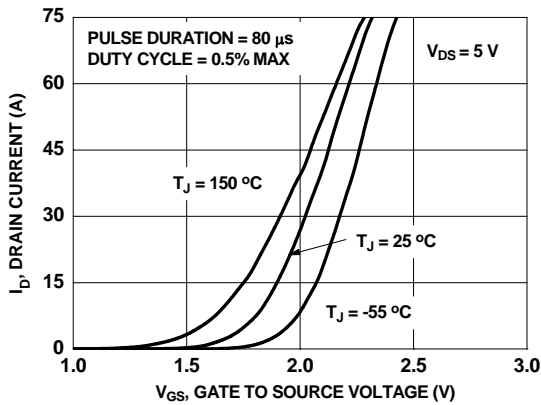
Figure 1. On Region Characteristics

Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage
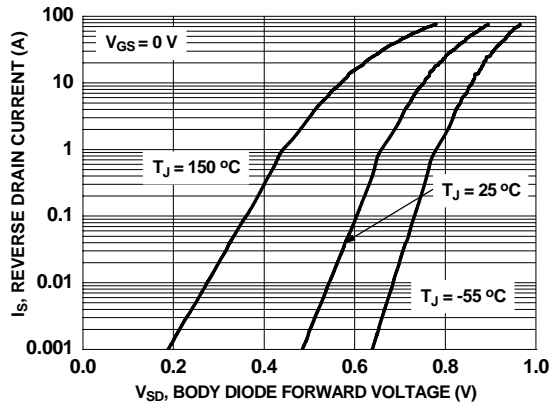
Figure 3. Normalized On Resistance vs. Junction Temperature

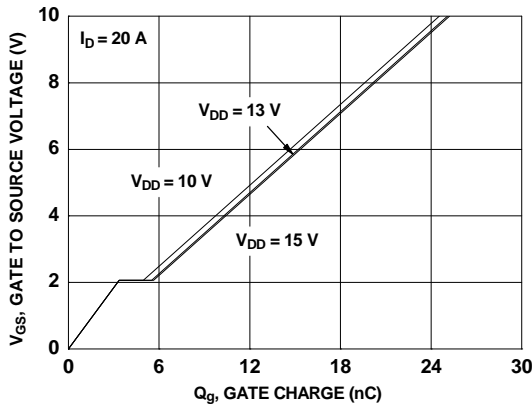**Figure 4. On-Resistance vs. Gate to Source Voltage**
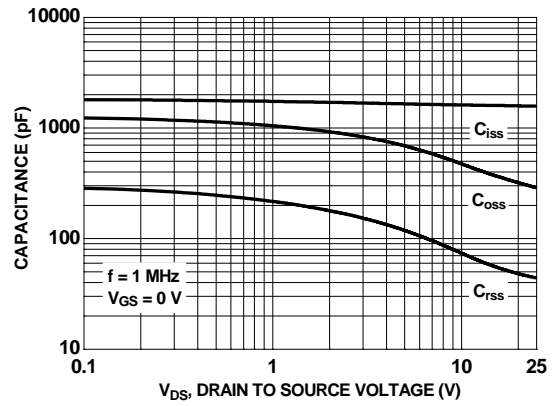
Figure 5. Transfer Characteristics

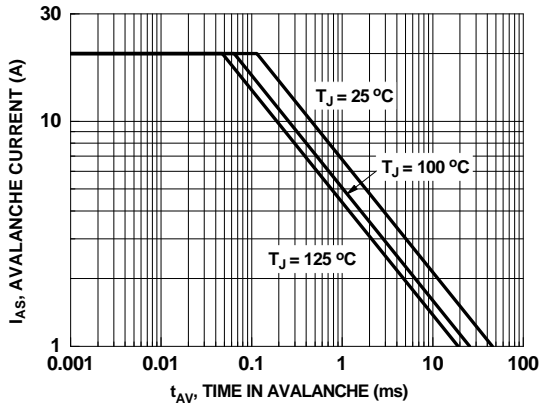**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

Typical Characteristics (Q1 N-Channel) $T_J = 25°C$ unless otherwise noted
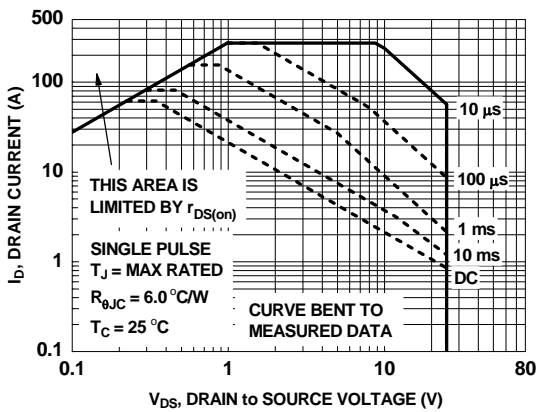

Figure 7. Gate Charge Characteristics
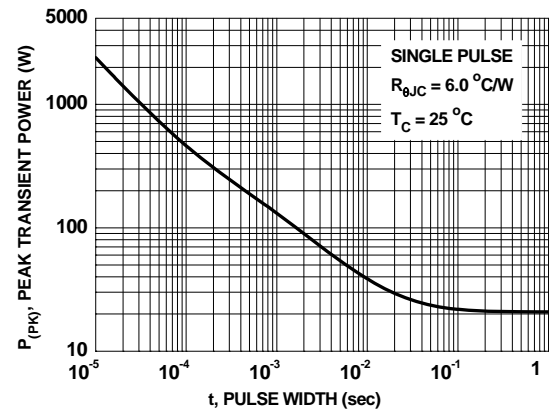

Figure 8. Capacitance vs. Drain to Source Voltage

Figure 9. Unclamped Inductive Switching Capability
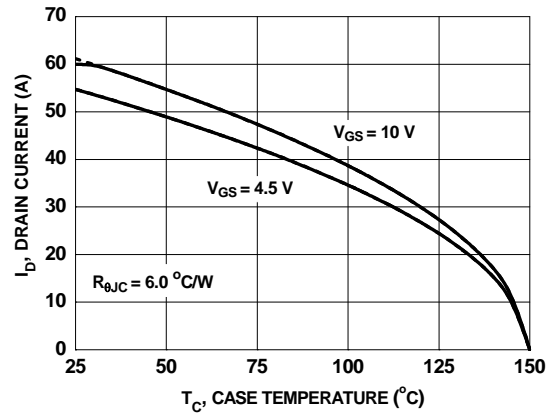
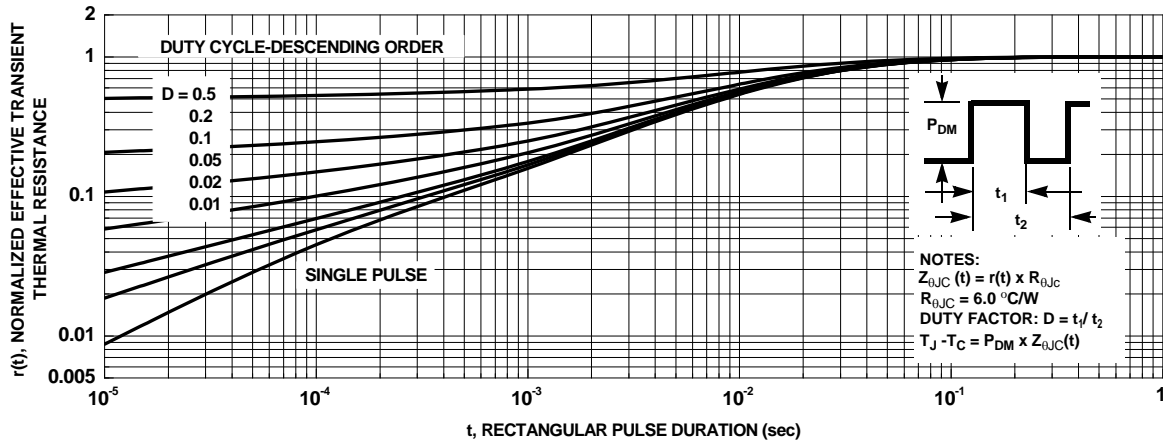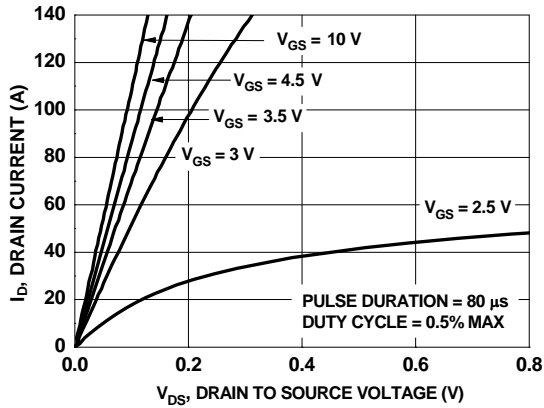Figure 10. Maximum Continuous Drain Current vs. Case Temperature

Figure 11. Forward Bias Safe Operating Area

Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

NOTES:
$Z_{\theta JC}$ (t) = r(t) x $R_{\theta Jc}$
$R_{\theta JC}$ = 6.0 °C/W
DUTY FACTOR: D = t_1/ t_2
T_J -T_C = P_{DM} x $Z_{\theta JC}$(t)

r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

t, RECTANGULAR PULSE DURATION (sec)

Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) T$_J$ = 25 °C unless otherwise noted

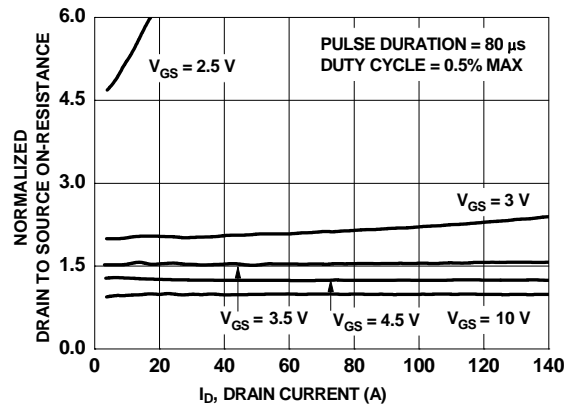**Figure 14. On- Region Characteristics**

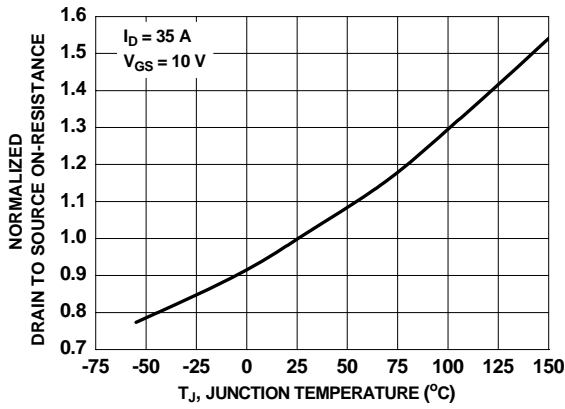**Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage**

Figure 16. Normalized On-Resistance vs. Junction Temperature
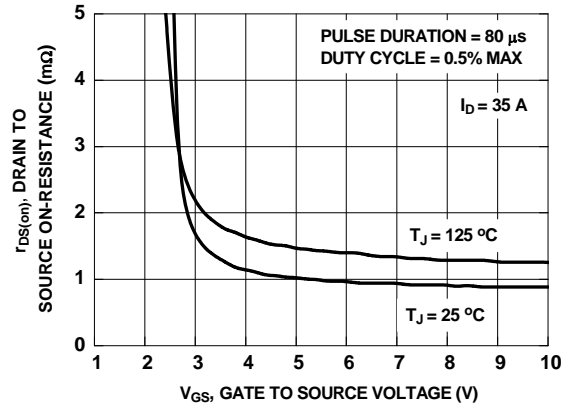
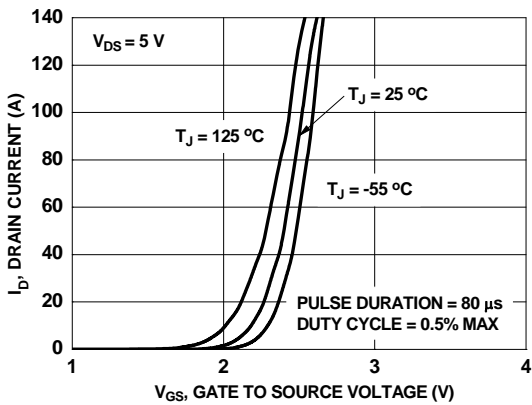**Figure 17. On-Resistance vs. Gate to Source Voltage**
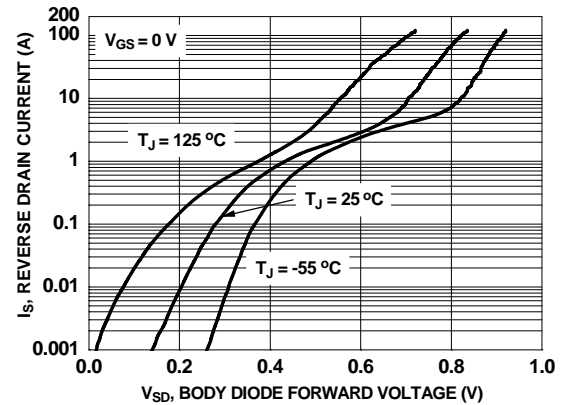
Figure 18. Transfer Characteristics

Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25°C$ unless otherwise noted

$I_D = 35$ A
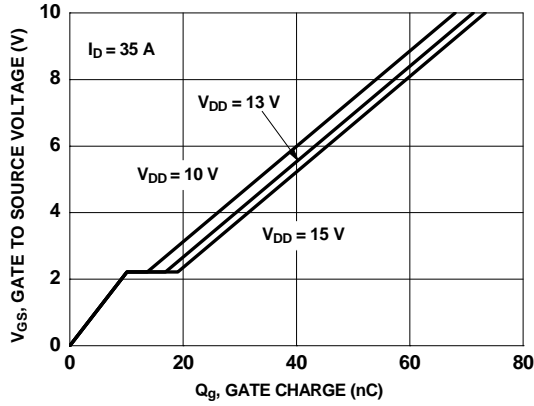
$V_{DD} = 13$ V

$V_{DD} = 10$ V

$V_{DD} = 15$ V

Figure 20. Gate Charge Characteristics

C_{iss}

C_{oss}

f = 1 MHz
$V_{GS} = 0$ V

C_{rss}
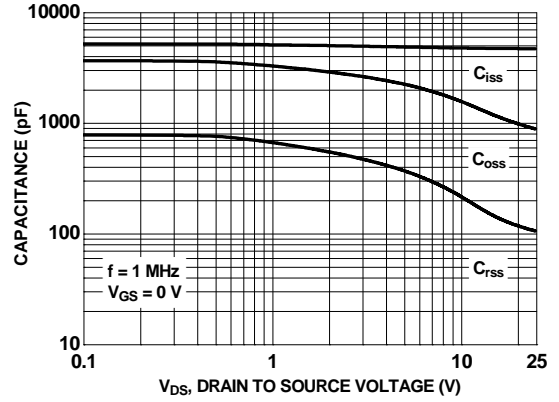
**Figure 21. Capacitance vs. Drain
to Source Voltage**

$T_J = 25$ °C

$T_J = 100$ °C

$T_J = 125$ °C
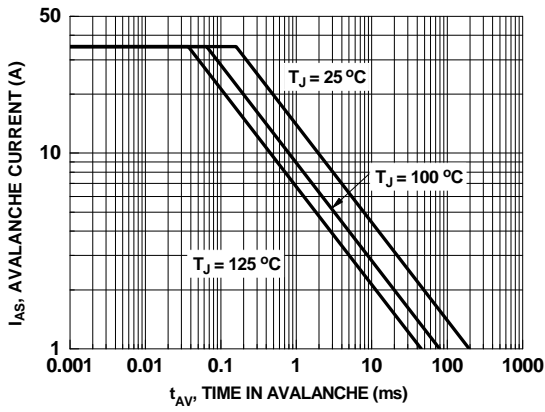
**Figure 22. Unclamped Inductive
Switching Capability**

$V_{GS} = 10$ V

Limited by Package

$R_{\theta JC} = 3.0$ °C/W

$V_{GS} = 4.5$ V
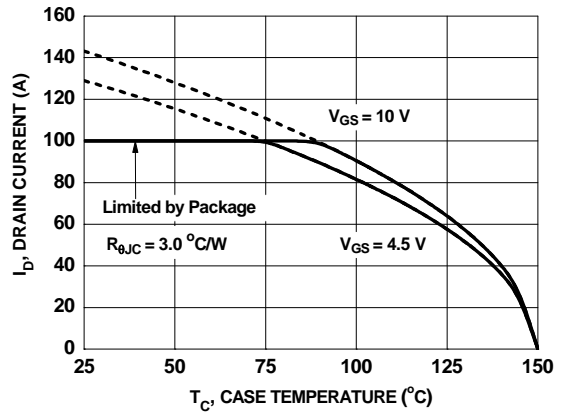
**Figure 23. Maximum Continuous Drain
Current vs. Case Temperature**

10 µs

100 µs

1 ms

10 ms

DC

THIS AREA IS
LIMITED BY $r_{DS(on)}$

SINGLE PULSE
T_J = MAX RATED
$R_{\theta JC} = 3.0$ °C/W
$T_C = 25$ °C

CURVE BENT TO
MEASURED DATA
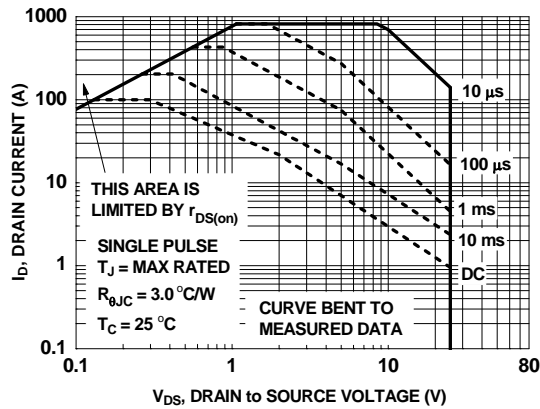
**Figure 24. Forward Bias Safe
Operating Area**

SINGLE PULSE
$R_{\theta JC} = 3.0$ °C/W
$T_C = 25$ °C

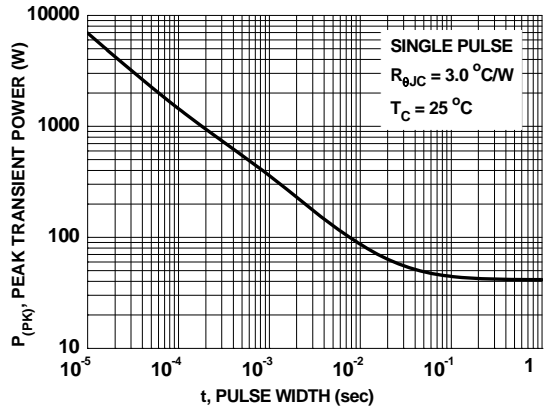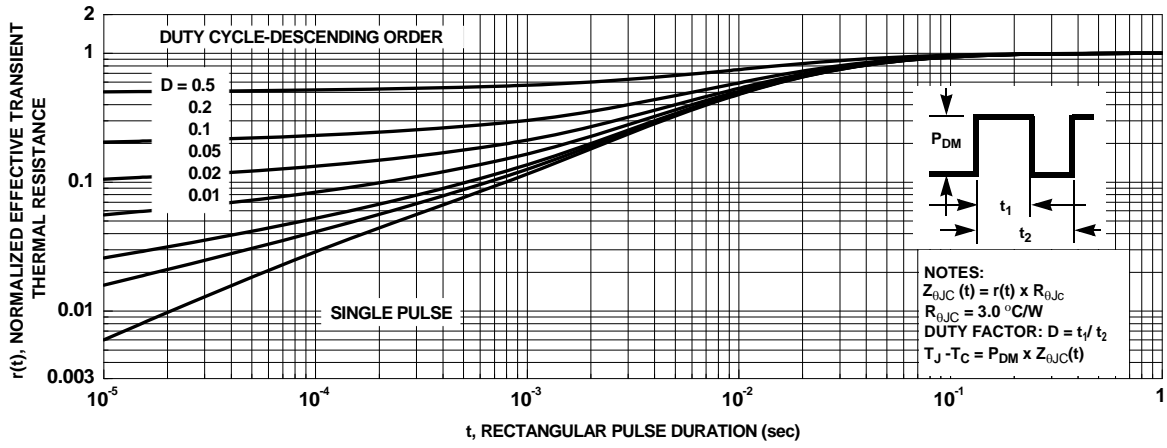**Figure 25. Single Pulse Maximum
Power Dissipation**

## Typical Characteristics (Q2 N-Channel) T_J = 25 °C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

t, RECTANGULAR PULSE DURATION (sec)

NOTES:
$Z_{\theta JC}(t) = r(t) \times R_{\theta Jc}$
$R_{\theta JC}$ = 3.0 °C/W
DUTY FACTOR: D = t_1 / t_2
$T_J - T_C = P_{DM} \times Z_{\theta JC}(t)$

Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverses recovery characteristic of the FDPC8016S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
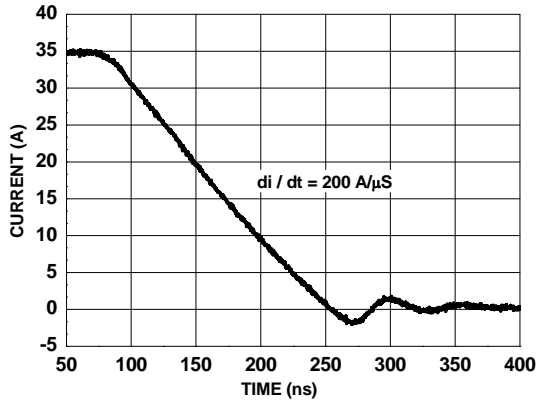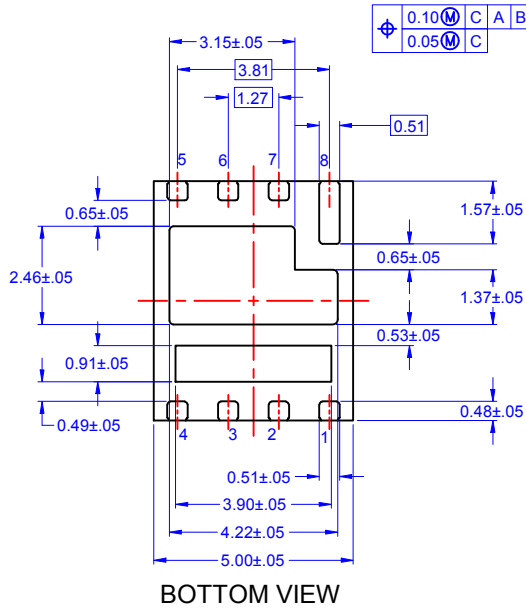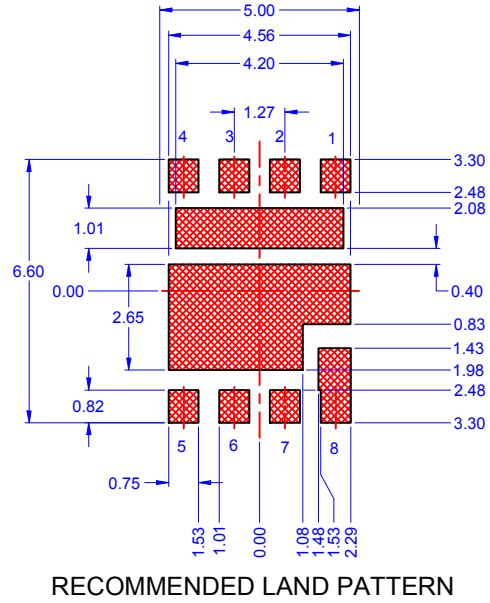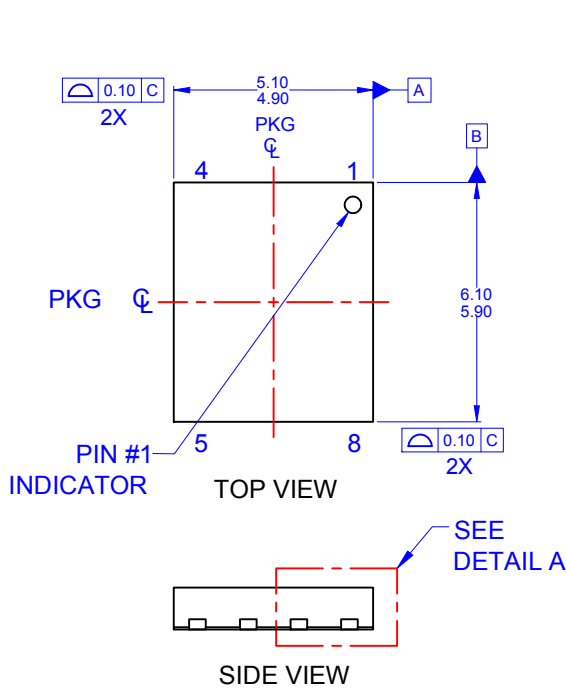

Figure 27. FDPC8016S SyncFET™ Body Diode Reverse Recovery Characteristic
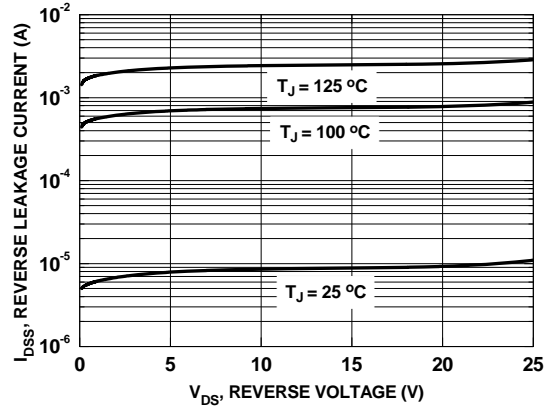
Figure 28. SyncFET™ Body Diode Reverse Leakage vs. Drain-source Voltage

Dimensional Outline and Pad Layout

0.10 C
2X

5.10
4.90
PKG
C̵L

A

B

4   1

PKG   C̵L

6.10
5.90

PIN #1
INDICATOR

5   8

0.10 C
2X

TOP VIEW

SEE
DETAIL A

SIDE VIEW

5.00
4.56
4.20

1.27

4   3   2   1

3.30
2.48
2.08

1.01

6.60   0.00   0.40
2.65   0.83
1.43
1.98
2.48
3.30

0.82

5   6   7   8

0.75

1.53 1.01 0.00 1.08 1.48 1.53 2.29

RECOMMENDED LAND PATTERN

⌖ 0.10 Ⓜ C A B
0.05 Ⓜ C

3.15±.05
3.81
1.27
0.51

5   6   7   8

0.65±.05

1.57±.05

2.46±.05

0.65±.05

1.37±.05

0.91±.05

0.53±.05

0.49±.05

0.48±.05

4   3   2   1

0.51±.05
3.90±.05
4.22±.05
5.00±.05

BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) DOES NOT FULLY CONFORM TO
    JEDEC REGISTRATION, MO-229,
    DATED 11/2001.
B) ALL DIMENSIONS ARE IN
    MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE
    BURRS OR MOLD FLASH. MOLD
    FLASH OR BURRS DOES NOT
    EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING
    PER ASME Y14.5M-1994.
E) DRAWING FILE NAME:

⫽ 0.10 C

⌒ 0.08 C

0.80
0.70

0.30
0.20

0.05
0.00

C

SEATING
PLANE

DETAIL A
(SCALE: 2X)
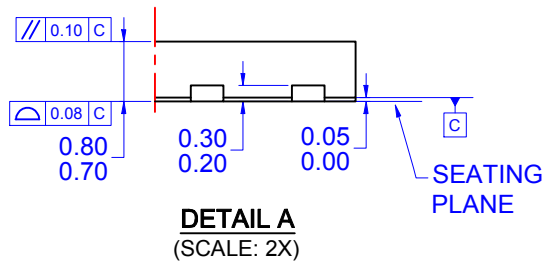
TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™	F-PFS™	®	Sync-Lock™
AX-CAP®*	FRFET®		**SYSTEM** ®*
BitSiC™	Global Power Resource℠	PowerTrench®	**GENERAL**
Build it Now™	GreenBridge™	PowerXS™	TinyBoost®
CorePLUS™	Green FPS™	Programmable Active Droop™	TinyBuck®
CorePOWER™	Green FPS™ e-Series™	QFET®	TinyCalc™
CROSSVOLT™	G*max*™	QS™	TinyLogic®
CTL™	GTO™	Quiet Series™	TINYOPTO™
Current Transfer Logic™	IntelliMAX™	RapidConfigure™	TinyPower™
DEUXPEED®	ISOPLANAR™	™	TinyPWM™
Dual Cool™	Marking Small Speakers Sound Louder		TinyWire™
EcoSPARK®	and Better™	Saving our world, 1mW/W/kW at a time™	TranSiC™
EfficentMax™	MegaBuck™	SignalWise™	TriFault Detect™
ESBC™	MICROCOUPLER™	SmartMax™	TRUECURRENT®*
	MicroFET™	SMART START™	µSerDes™
®	MicroPak™	Solutions for Your Success™	
	MicroPak2™	SPM®	
Fairchild®	MillerDrive™	STEALTH™	UHC®
Fairchild Semiconductor®	MotionMax™	SuperFET®	Ultra FRFET™
FACT Quiet Series™	mWSaver®	SuperSOT™-3	UniFET™
FACT®	OptoHiT™	SuperSOT™-6	VCX™
FAST®	OPTOLOGIC®	SuperSOT™-8	VisualMax™
FastvCore™	OPTOPLANAR®	SupreMOS®	VoltagePlus™
FETBench™		SyncFET™	XS™
FPS™			

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER
FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY
FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY
Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC   www.onsemi.com