



ON Semiconductor®

# FDS8958B

## Dual N & P-Channel PowerTrench® MOSFET

Q1-N-Channel: 30 V, 6.4 A, 26 mΩ Q2-P-Channel: -30 V, -4.5 A, 51 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 26 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 6.4\text{ A}$
- Max  $r_{DS(on)}$  = 39 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 5.2\text{ A}$

Q2: P-Channel

- Max  $r_{DS(on)}$  = 51 mΩ at  $V_{GS} = -10\text{ V}$ ,  $I_D = -4.5\text{ A}$
- Max  $r_{DS(on)}$  = 80 mΩ at  $V_{GS} = -4.5\text{ V}$ ,  $I_D = -3.3\text{ A}$
- HBM ESD protection level > 3.5 kV (Note 3)
- RoHS Compliant



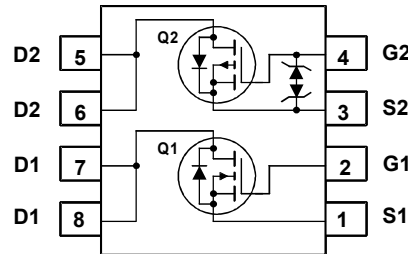
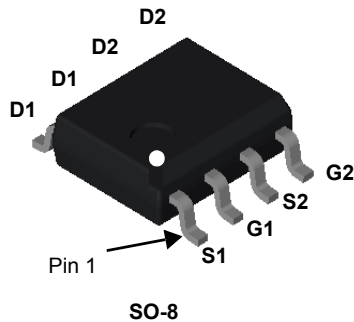
### General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Application

- DC-DC Conversion
- BLU and motor drive inverter



### MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	-30	V
$V_{GS}$	Gate to Source Voltage	±20	±25	V
$I_D$	Drain Current - Continuous $T_A = 25\text{ °C}$	6.4	-4.5	A
	- Pulsed	30	-30	
$P_D$	Power Dissipation for Dual Operation	2.0		W
	Power Dissipation for Single Operation $T_A = 25\text{ °C}$ (Note 1a)	1.6		
	$T_A = 25\text{ °C}$ (Note 1b)	0.9		
$E_{AS}$	Single Pulse Avalanche Energy (Note 4)	18	5	mJ
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8958B	FDS8958B	SO-8	13"	12 mm	2500 units

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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#### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ $I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		24 -21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 -1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			$\pm 100$ $\pm 10$	nA $\mu\text{A}$

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	Q1 Q2	1.0 -1.0	2.0 -1.9	3.0 -3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$ $I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-6 5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 6.4\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 5.2\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 6.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q1		21 29 31	26 39 39	m $\Omega$
		$V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.3\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -4.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q2		38 60 53	51 80 72	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 6.4\text{ A}$ $V_{DD} = -5\text{ V}, I_D = -4.5\text{ A}$	Q1 Q2		20 10		S

#### Dynamic Characteristics

$C_{iss}$	Input Capacitance	Q1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		405 570	540 760	pF
$C_{oss}$	Output Capacitance	Q2	Q1 Q2		75 115	100 155	pF
$C_{riss}$	Reverse Transfer Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		55 100	80 150	pF
$R_g$	Gate Resistance		Q1 Q2		2.4 4.4		$\Omega$

#### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1	Q1 Q2		4.3 6.0	10 12	ns
$t_r$	Rise Time	$V_{DD} = 15\text{ V}, I_D = 6.4\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1		2.0	10	ns
			Q2		6.0	12	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -15\text{ V}, I_D = -4.5\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1		12	22	ns
			Q2		17	30	
$t_f$	Fall Time	$V_{DD} = -15\text{ V}, I_D = -4.5\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1		2.0	10	ns
			Q2		7.0	14	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}$ $V_{GS} = -10\text{ V}$	Q1		8.3	12	nC
			Q2		14	19	
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}$ $V_{GS} = -4.5\text{ V}$	Q1	$V_{DD} = 15\text{ V},$ $I_D = 6.4\text{ A}$	4.1	5.8	nC
			Q2		7.0	9.6	
$Q_{gs}$	Gate to Source Charge		Q1		1.3		nC
			Q2		1.9		
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1		1.7		nC
			Q2		3.6		

### Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)	Q2		-0.8	-1.2	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 6.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		17	30	ns
			Q2		20	36	
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = -4.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		6	12	nC
			Q2		8	16	

**NOTES:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



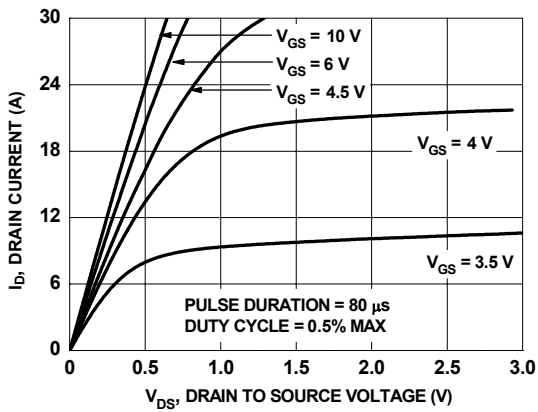
a) 78 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



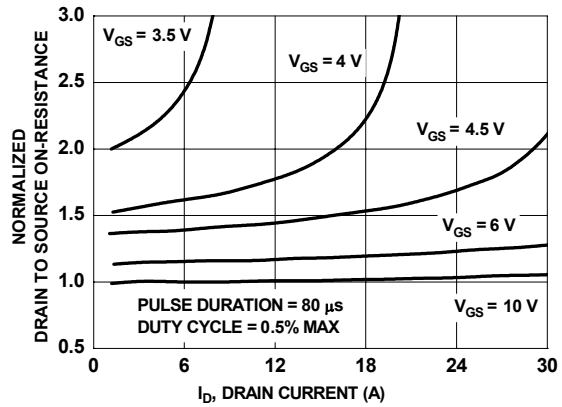
b) 135 °C/W when mounted on a minimum pad

- 2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- 4. UIL condition: Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 6\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . (Q1)  
Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = -4\text{ A}$ ,  $V_{DD} = -27\text{ V}$ ,  $V_{GS} = -10\text{ V}$ . (Q2)

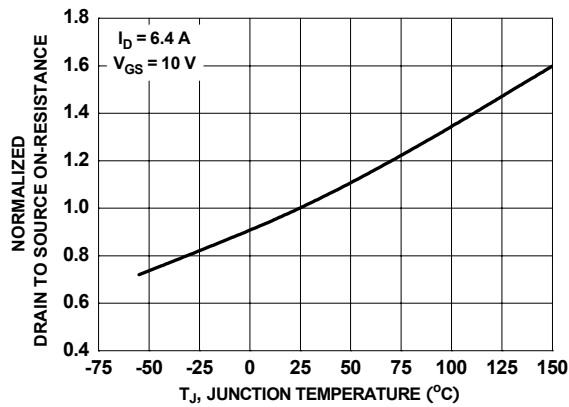
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



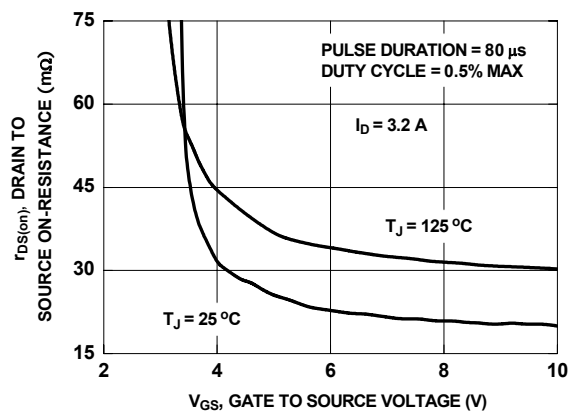
**Figure 1. On Region Characteristics**



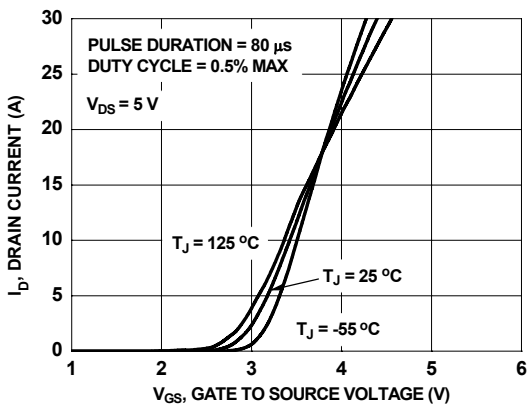
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



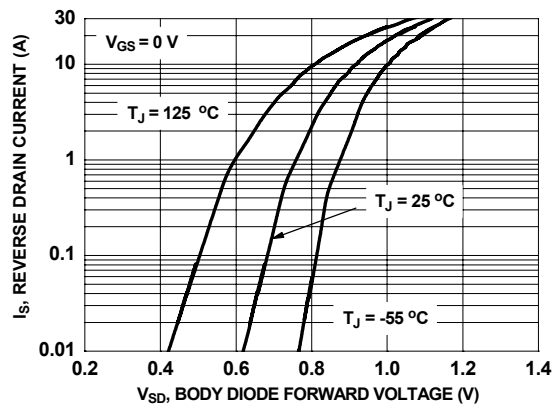
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

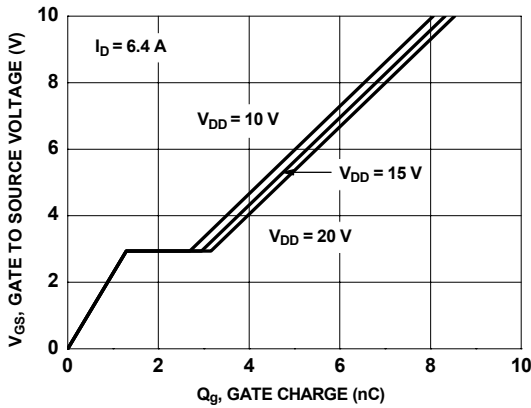


**Figure 5. Transfer Characteristics**

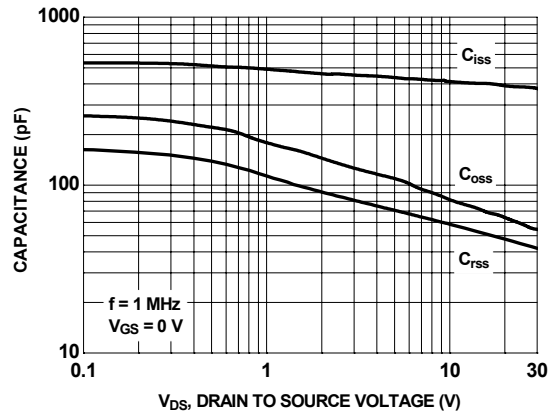


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

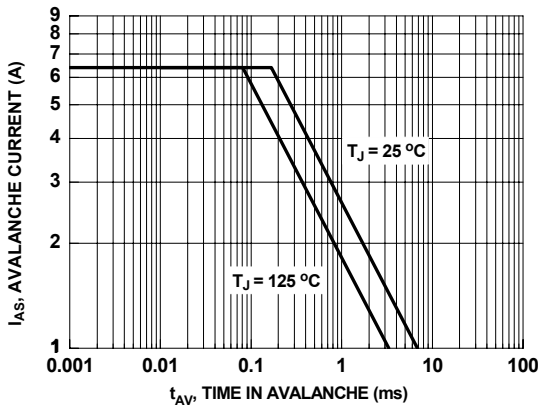
**Typical Characteristics (Q1 N-Channel)**  $T_J = 25^\circ\text{C}$  unless otherwise noted



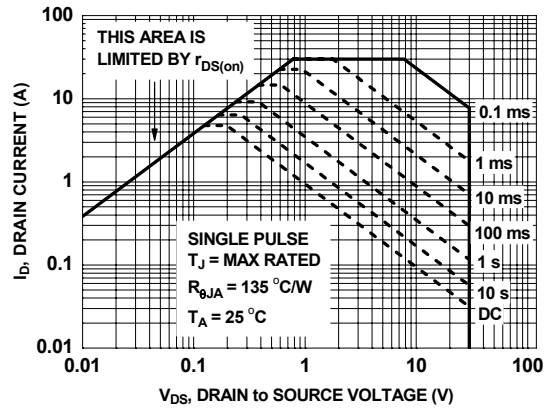
**Figure 7. Gate Charge Characteristics**



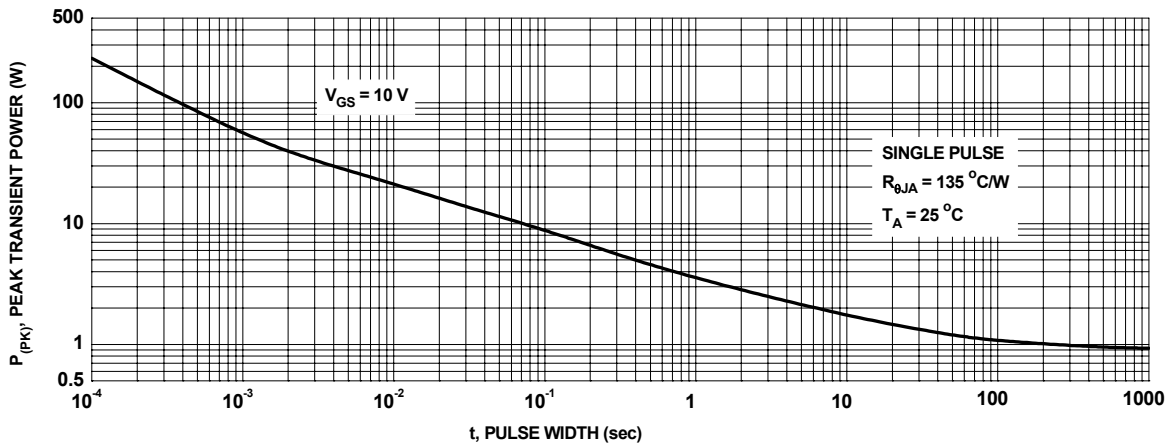
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**

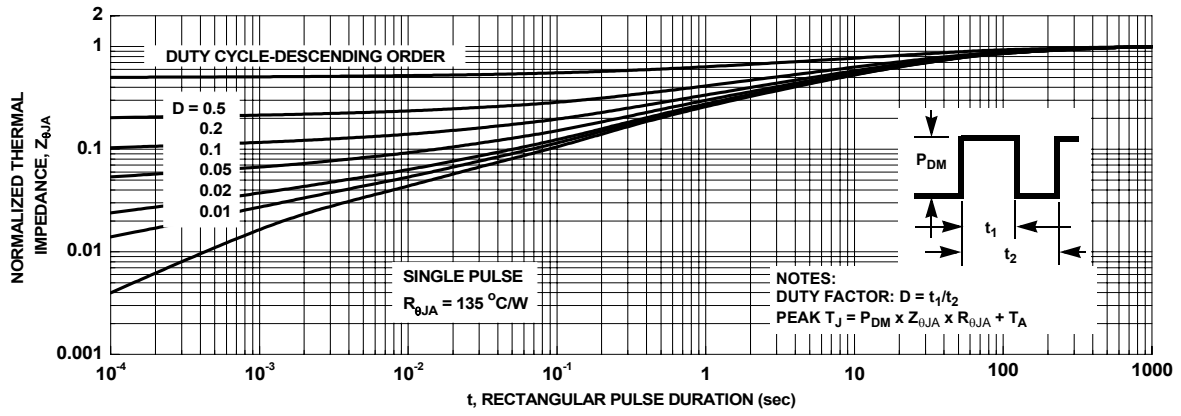


**Figure 10. Forward Bias Safe Operating Area**



**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics (Q1 N-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

**Typical Characteristics (Q2 P-Channel)**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

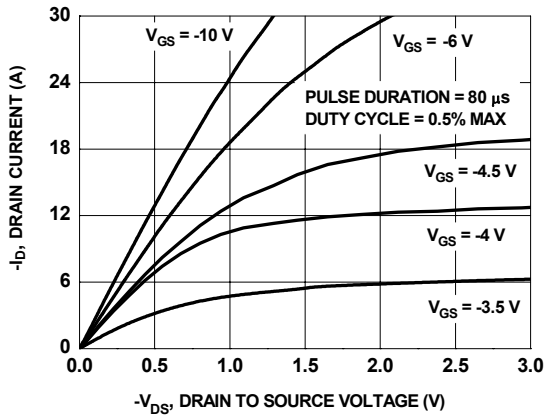


Figure 15. On-Region Characteristics

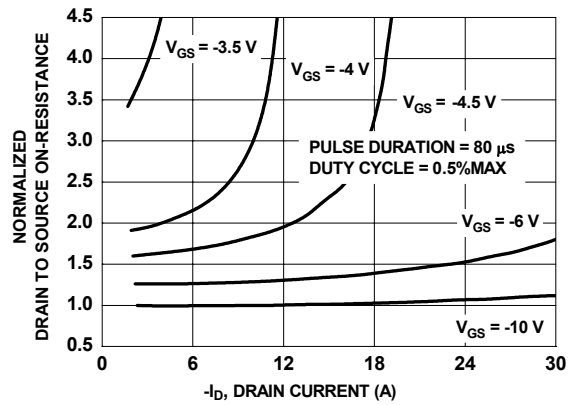


Figure 16. Normalized on-Resistance vs Drain Current and Gate Voltage

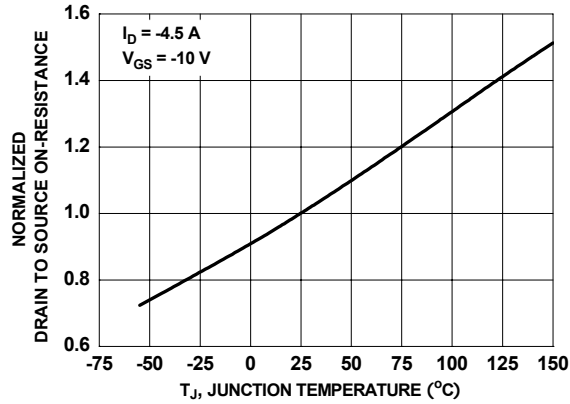


Figure 17. Normalized On-Resistance vs Junction Temperature

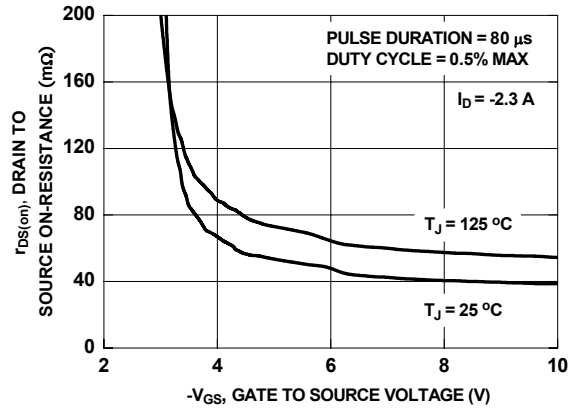


Figure 18. On-Resistance vs Gate to Source Voltage

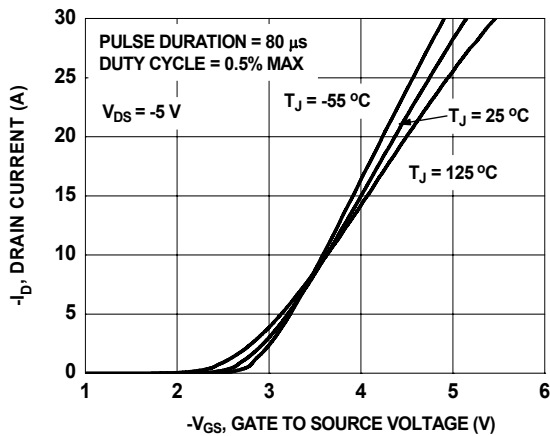


Figure 19. Transfer Characteristics

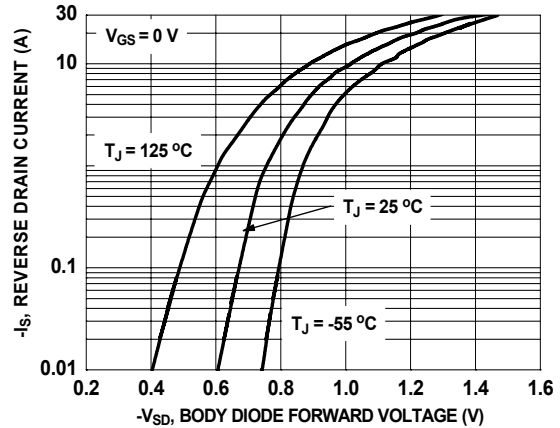
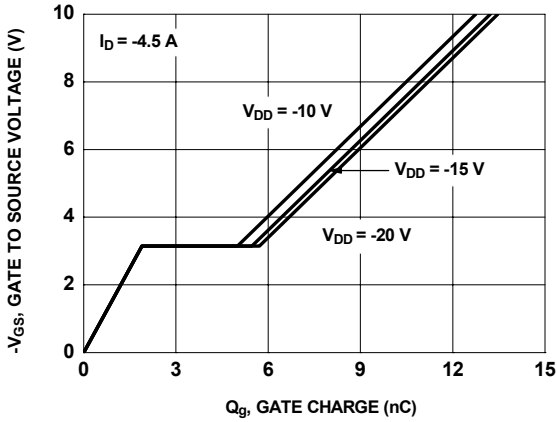
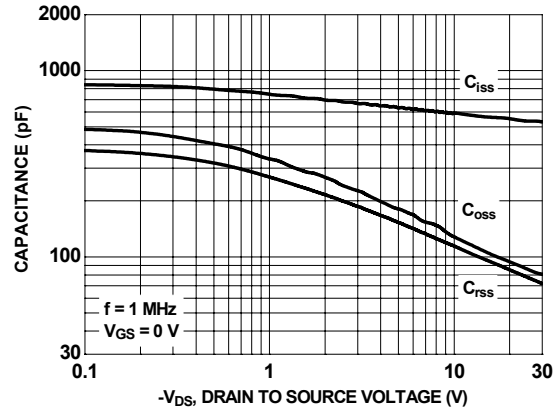


Figure 20. Source to Drain Diode Forward Voltage vs Source Current

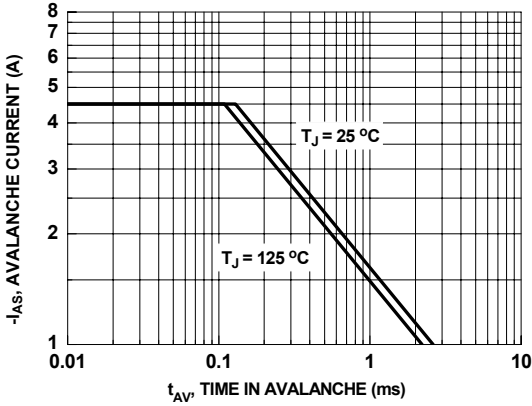
**Typical Characteristics (Q2 P-Channel)  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted**



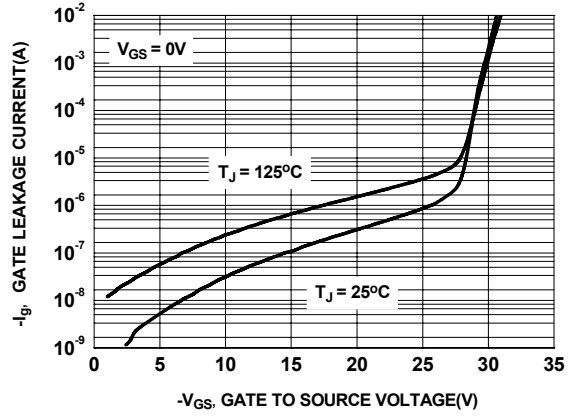
**Figure 21. Gate Charge Characteristics**



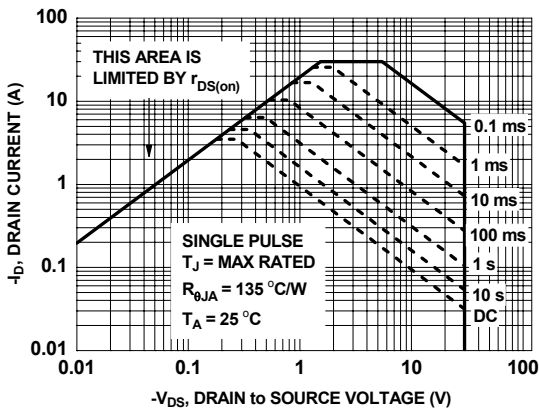
**Figure 22. Capacitance vs Drain to Source Voltage**



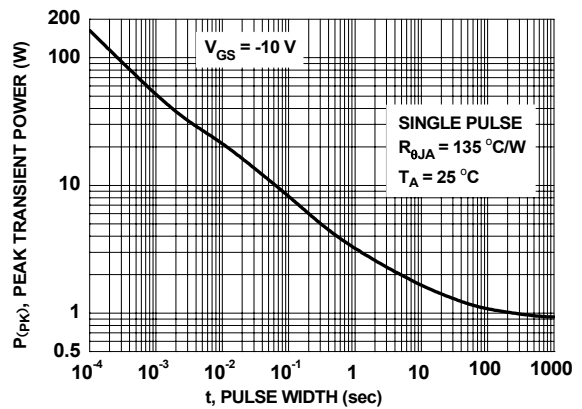
**Figure 23. Unclamped Inductive Switching Capability**



**Figure 24.  $I_g$  vs  $V_{GS}$**



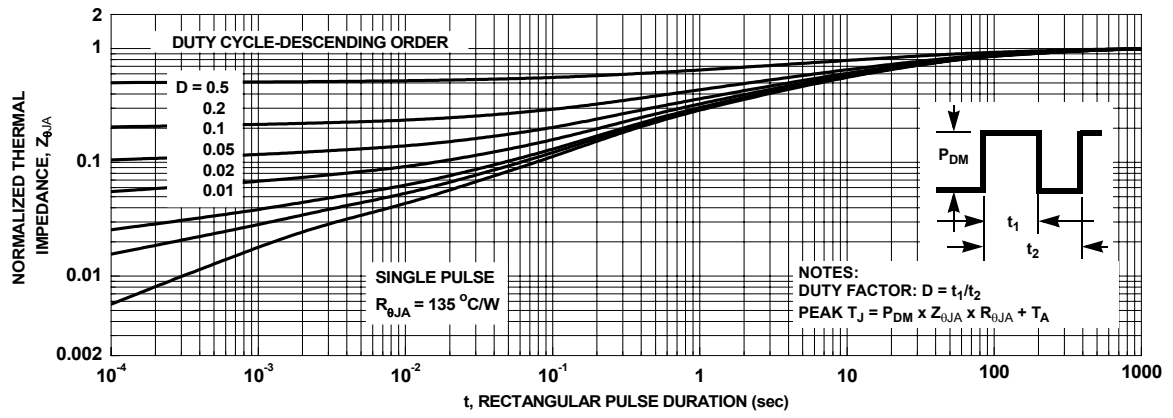
**Figure 25. Forward Bias Safe Operating Area**



**Figure 26. Single Pulse Maximum Power Dissipation**

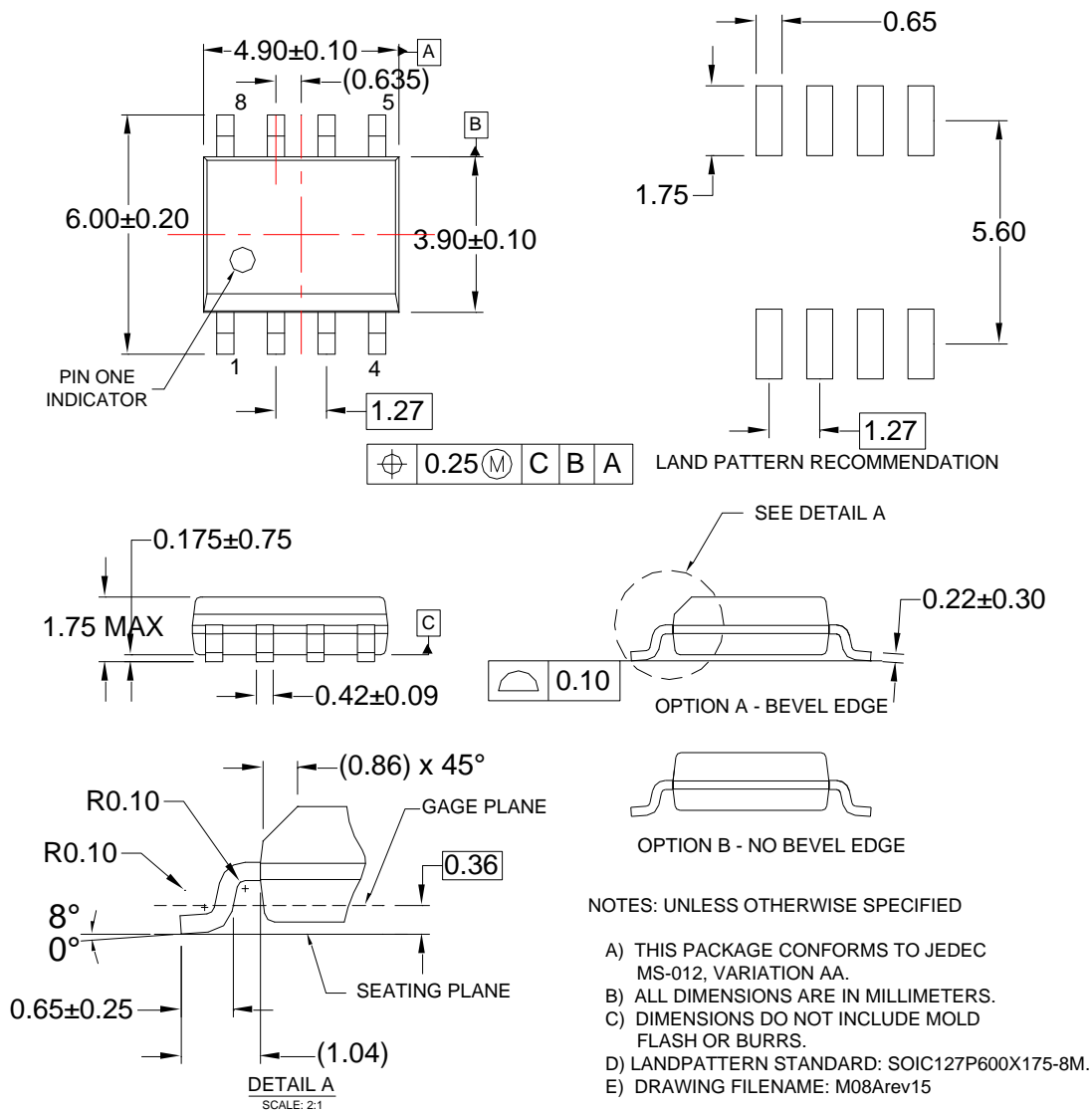


**Typical Characteristics (Q2 P-Channel)  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted**




**Figure 27. Junction-to-Ambient Transient Thermal Response Curve**

### Physical Dimensions



**Figure 16. 8-Lead, SOIC, JEDEC MS-012, .150-inch Narrow Body**

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