NCV8664C

Linear Regulator, Low Dropout, Very Low I_q

The NCV8664C is a precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 22 μA.

NCV8664C is pin and functionally compatible with NCV4264−2C and could replace this part when lower quiescent current is required.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 3.3 V, 5.0 V Fixed Output
- ±2.0 % Output Accuracy, Over Full Temperature Range
- 22 μA Typical Quiescent Current
- 600 mV Maximum Dropout Voltage at 150 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- EMC Compliant
- These are Pb−Free Devices

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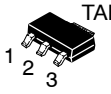
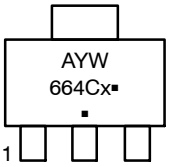
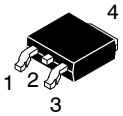
MARKING DIAGRAMS

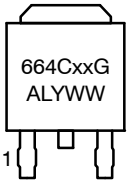


SOT−223
ST SUFFIX
CASE 318E





DPAK
DT SUFFIX
CASE 369C



xx	= Voltage Rating DPAK (50 = 5.0 V Version) (33 = 3.3 V Version)
x	= Voltage Rating SOT223 (5 = 5.0 V Version) (3 = 3.3 V Version)
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
▪ or G	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS

(SOT−223/DPAK)

PIN	FUNCTION
1	V_{IN}
2,4,TAB	GND
3	V_{OUT}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

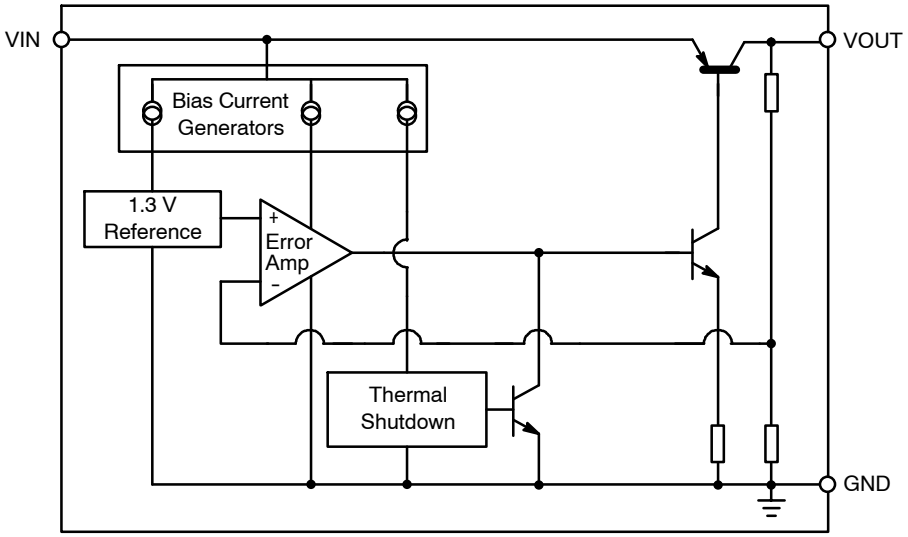


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. DPAK/SOT−223	Symbol	Function
1	V_{IN}	Unregulated input voltage; 4.5 V to 45 V.
2	GND	Ground; Must be connected to GND potential.
3	V_{OUT}	Regulated output voltage.
4, TAB	GND	Ground; substrate and best thermal connection to the die.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, DC Input Operating Voltage	V_{IN}	4.5	+45	V
Junction Temperature Operating Range	T_J	−40	+150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
V_{IN}, DC Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+32	V
Storage Temperature	T_{stg}	−55	+150	°C
ESD Capability, Human Body Model (Note 1)	V_{ESDHBM}	4	–	kV
ESD Capability, Machine Model (Note 1)	V_{ESDMIM}	200	–	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)

THERMAL RESISTANCE

Parameter		Symbol	Condition	Min	Max	Unit
Junction−to−Ambient	DPAK SOT−223	$R_{\theta JA}$		− −	87.4 (Note 2) 109 (Note 2)	°C/W
Junction−to−Tab	DPAK SOT−223	$R_{\psi JT}$		− −	3.5 10.9	°C/W

2. 1 oz copper, 100 mm^2 copper area, FR4.

LEAD SOLDERING TEMPERATURE AND MSL

Rating		Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD Styles Only), Lead Free (Note 3)		T_{sld}	−	265 pk	°C
Moisture Sensitivity Level	SOT223 DPAK	MSL	3 1	− −	−

3. Lead Free, 60 sec − 150 sec above 217°C, 40 sec max at peak.

ELECTRICAL CHARACTERISTICS (V_{IN} = 13.5 V, Tj = −40°C to +150°C, unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage 5.0 V Version	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 6.0 V ≤ V_{IN} ≤ 28 V	4.900	5.0	5.100	V
Output Voltage 5.0 V Version	V_{OUT}	0 mA ≤ I_{OUT} ≤ 150 mA 5.5 V ≤ V_{IN} ≤ 28 V −40°C ≤ T_J ≤ 125°C	4.900	5.0	5.100	V
Output Voltage 3.3 V Version	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 4) 4.5 V ≤ V_{IN} ≤ 28 V	3.234	3.3	3.366	V
Line Regulation 5.0 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 6.0 V ≤ V_{IN} ≤ 28 V	−25	0.7	+25	mV
Line Regulation 3.3 V Version	ΔV_{OUT} vs. V_{IN}	I_{OUT} = 5.0 mA 4.5 V ≤ V_{IN} ≤ 28 V	−25	0.6	+25	mV
Load Regulation	ΔV_{OUT} vs. I_{OUT}	1.0 mA ≤ I_{OUT} ≤ 150 mA (Note 4)	−35	0.5	+35	mV
Dropout Voltage 5.0 V Version	V_{IN}−V_{OUT}	I_Q = 100 mA (Notes 4 & 5) I_Q = 150 mA (Notes 4 & 5)	− −	230 270	500 600	mV
Quiescent Current	I_q	I_{OUT} = 100 μA T_J = 25°C T_J = −40°C to +85°C	− −	21 22	29 30	μA
Active Ground Current	$I_{G(ON)}$	I_{OUT} = 50 mA (Note 4) I_{OUT} = 150 mA (Note 4)	− −	0.5 3.1	3 15	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 $V_{P−P}$, F = 100 Hz	−	67	−	dB
PROTECTION						
Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 4.5 V (5.0 V Version) (Note 4) V_{OUT} = 3.0 V (3.3 V Version) (Note 4)	150 150	− −	500 500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 4)	100	−	500	mA
Thermal Shutdown Threshold	T_{TSD}	(Note 6)	150	−	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Use pulse loading to limit power dissipation.
5. Dropout voltage = (V_{IN} − V_{OUT}), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.

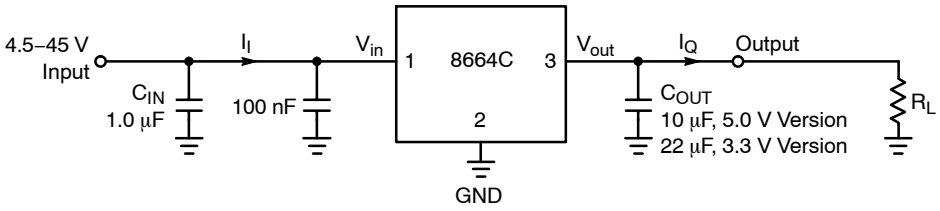


Figure 2. Measurement Circuit

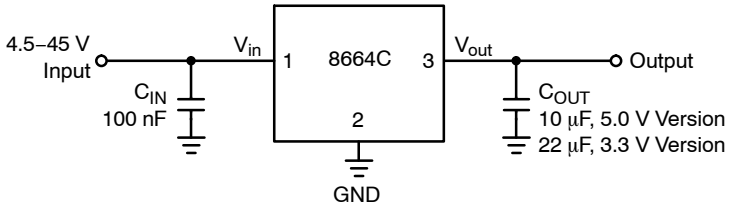


Figure 3. Applications Circuit

Typical Characteristic Curves – 5 V Version

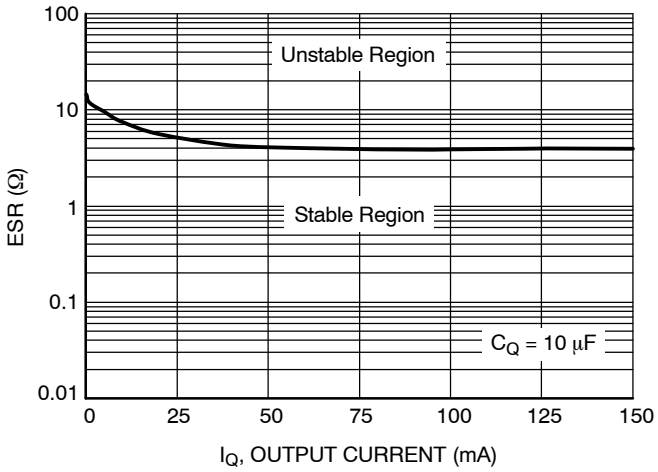


Figure 4. Output Stability with Output Capacitor ESR

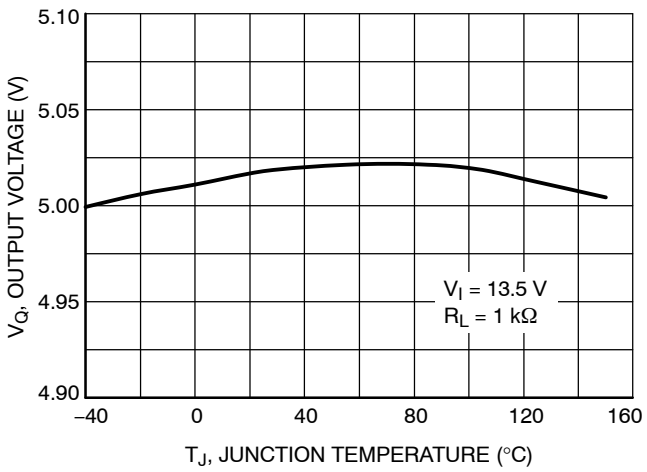


Figure 5. Output Voltage vs. Junction Temperature

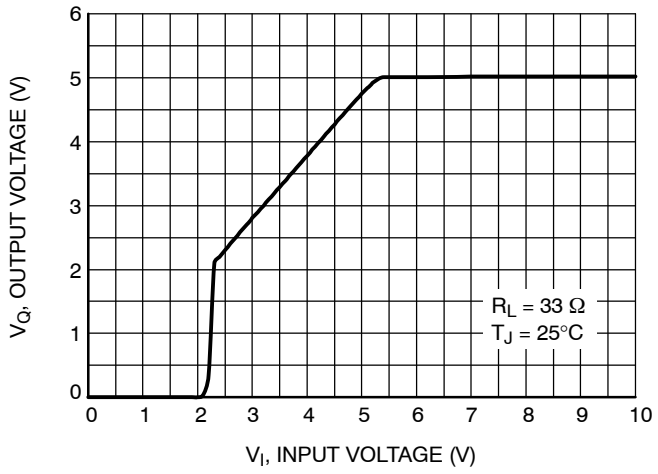


Figure 6. Output Voltage vs. Input Voltage

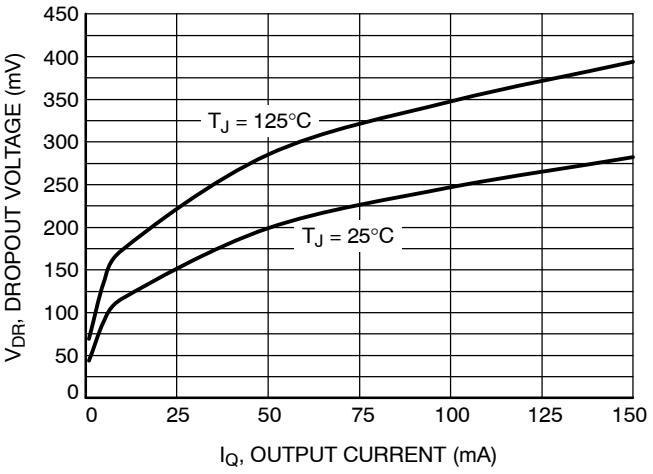


Figure 7. Dropout Voltage vs. Output Current

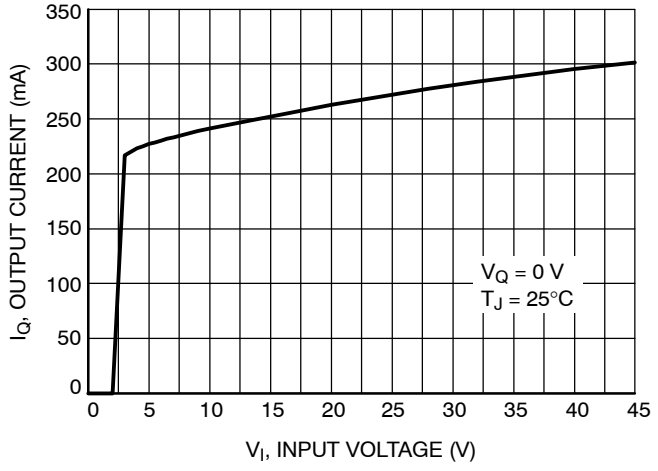


Figure 8. Maximum Output Current vs. Input Voltage

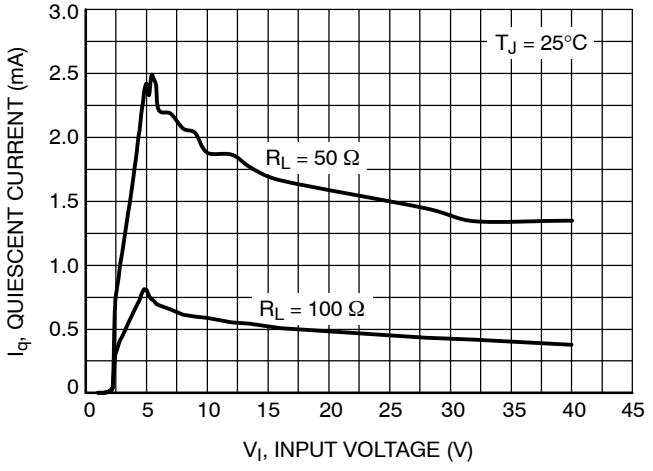


Figure 9. Quiescent Current vs. Input Voltage

Typical Characteristic Curves – 5 V Version

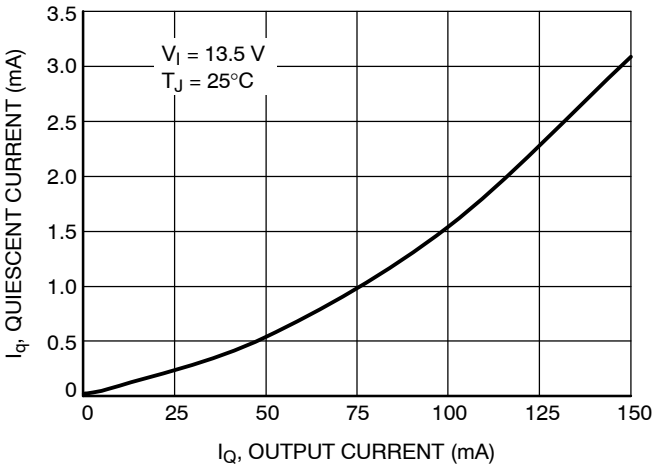


Figure 10. Quiescent Current vs. Output Current, (High Load)

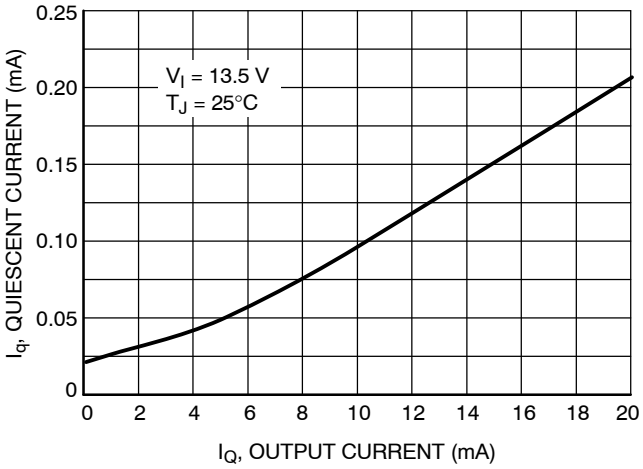


Figure 11. Quiescent Current vs. Output Current, (Low Load)

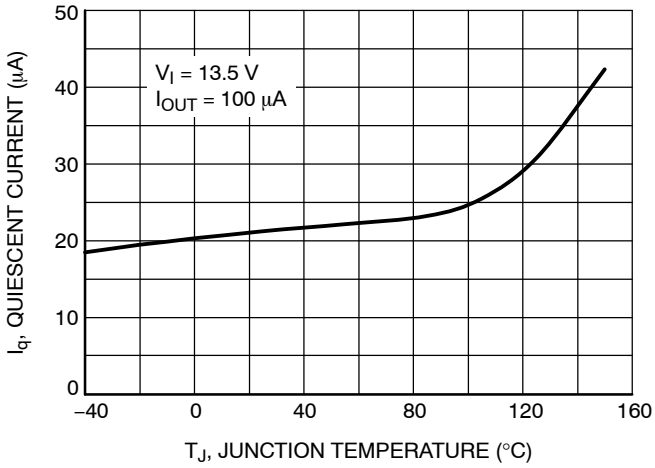


Figure 12. Quiescent Current vs. Temperature

Typical Characteristic Curves – 3.3 V Version

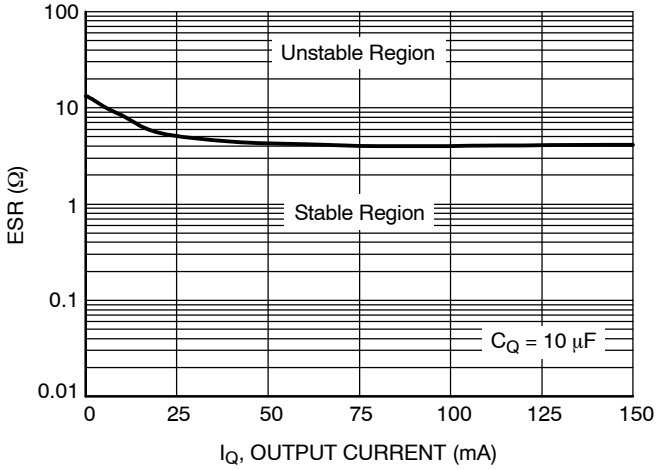


Figure 13. Output Stability with Output Capacitor ESR

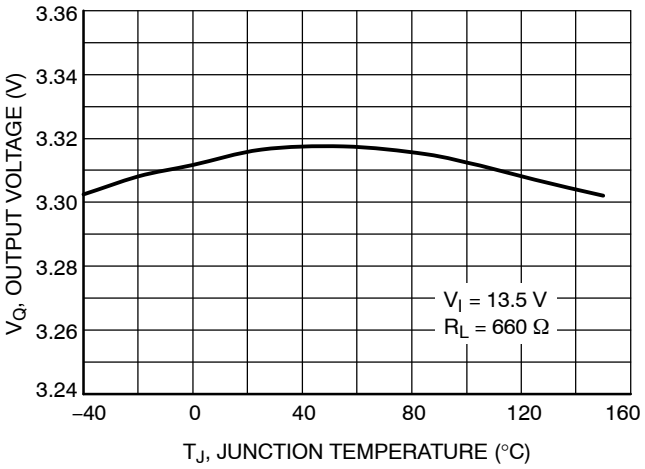


Figure 14. Output Voltage vs. Junction Temperature

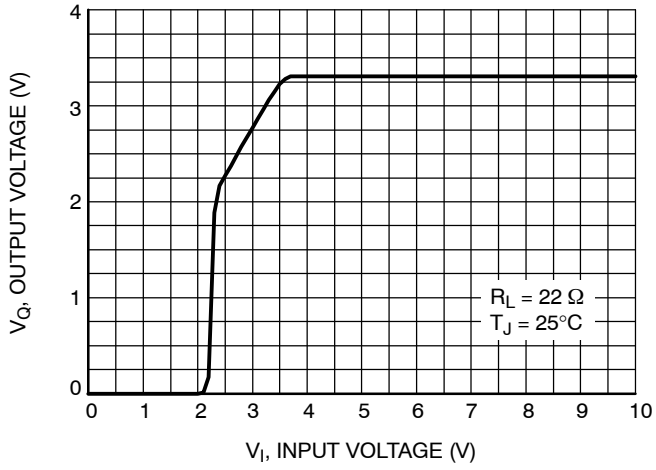


Figure 15. Output Voltage vs. Input Voltage

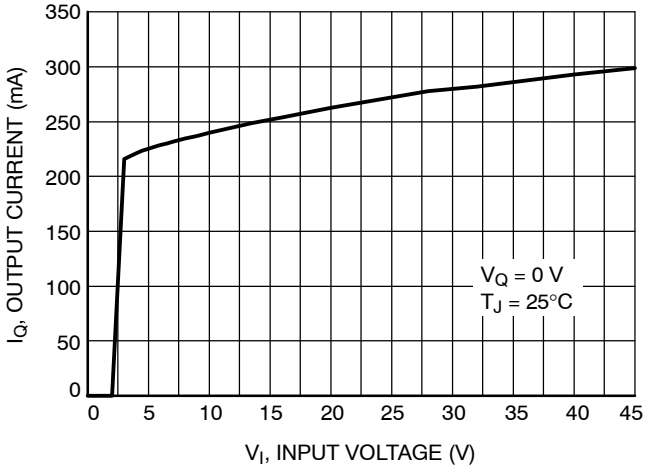


Figure 16. Maximum Output Current vs. Input Voltage

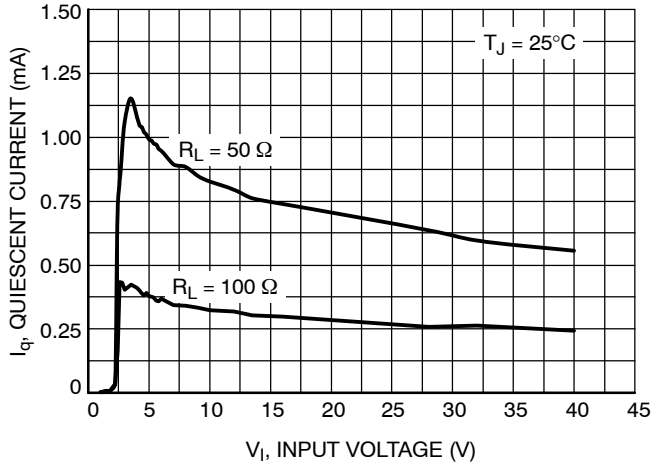


Figure 17. Quiescent Current vs. Input Voltage

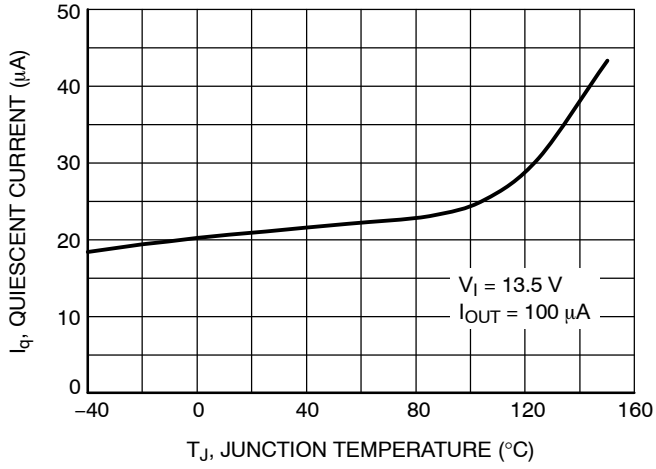


Figure 18. Quiescent Current vs. Temperature

Typical Characteristic Curves – 3.3 V Version

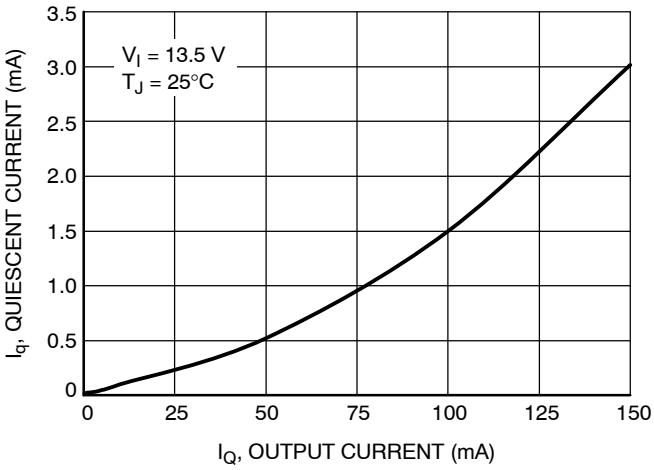


Figure 19. Quiescent Current vs. Output Current, (High Load)

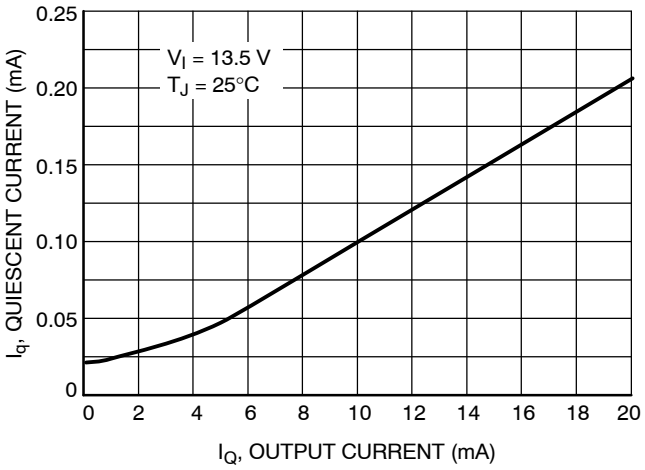


Figure 20. Quiescent Current vs. Output Current, (Low Load)

Circuit Description

The NCV8664C is a precision trimmed 3.3 V and 5.0 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 22 μA. The device has current capability of 150 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8664C is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

Regulator Stability Considerations

The input capacitor C_{IN} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with C_{IN}. The output or compensation capacitor, C_{OUT} helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Actual Stability Regions are shown in the graphs in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \quad \text{(eq. 1)}$$

Where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(Max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heat sinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor Website.

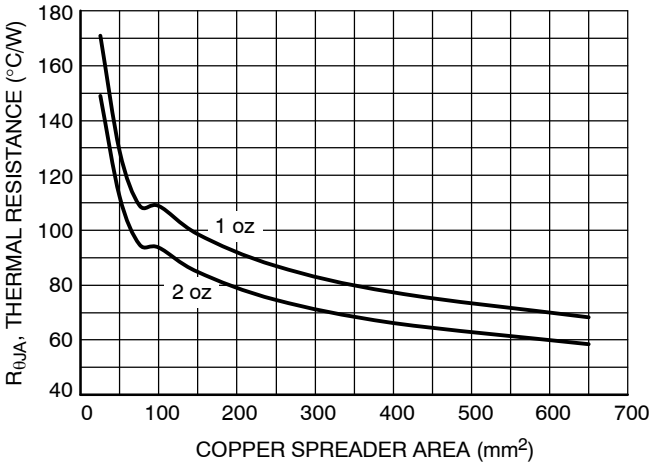


Figure 21. $R_{\theta JA}$ vs. Copper Spreader Area, SOT−223

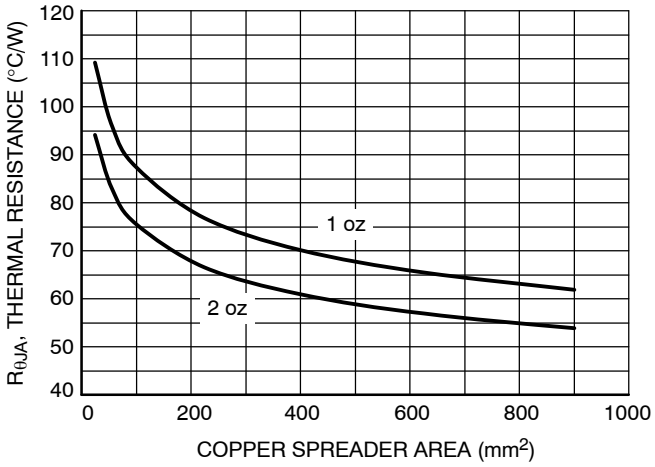


Figure 22. $R_{\theta JA}$ vs. Copper Spreader Area, DPAK

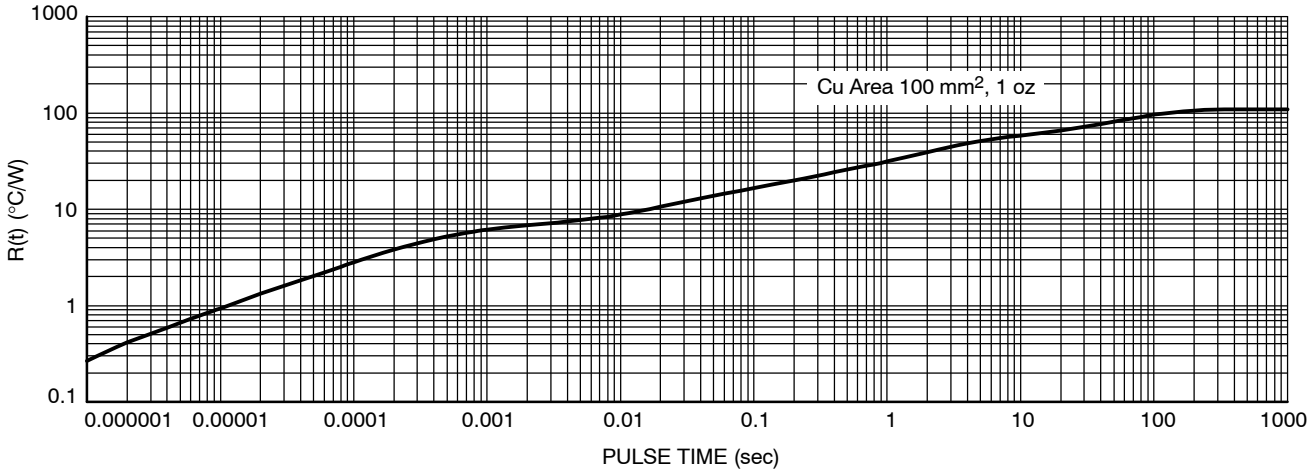


Figure 23. Single−Pulse Heating Curve, SOT−223

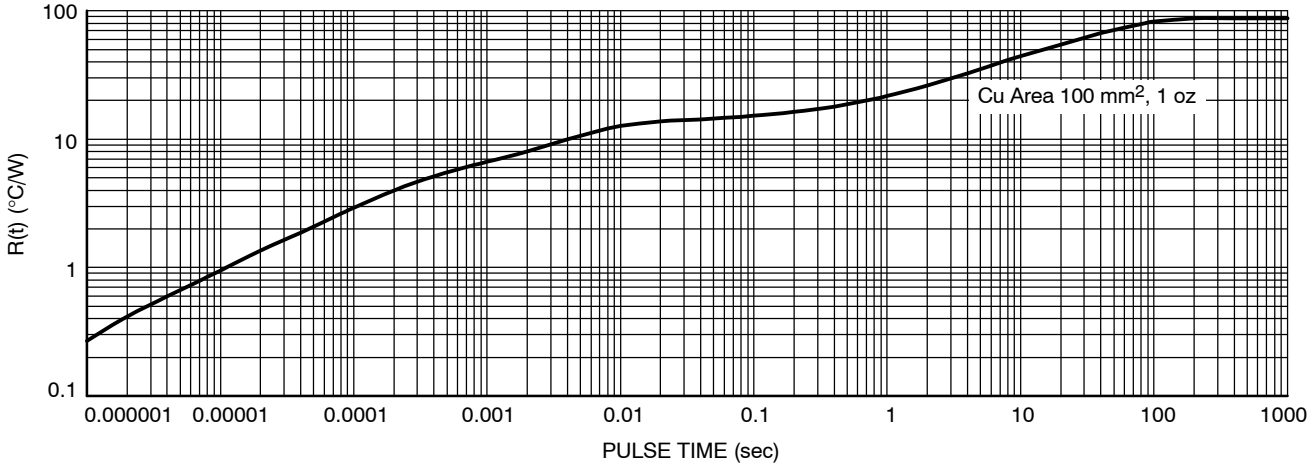


Figure 24. Single−Pulse Heating Curve, DPAK

ORDERING INFORMATION

Device*	Marking	Package	Shipping†
NCV8664CDT50RKG	664C50G	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8664CDT33RKG	664C33G	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8664CST50T3G	664C5	SOT−223 (Pb−Free)	4000 / Tape & Reel
NCV8664CST33T3G	664C3	SOT−223 (Pb−Free)	4000 / Tape & Reel

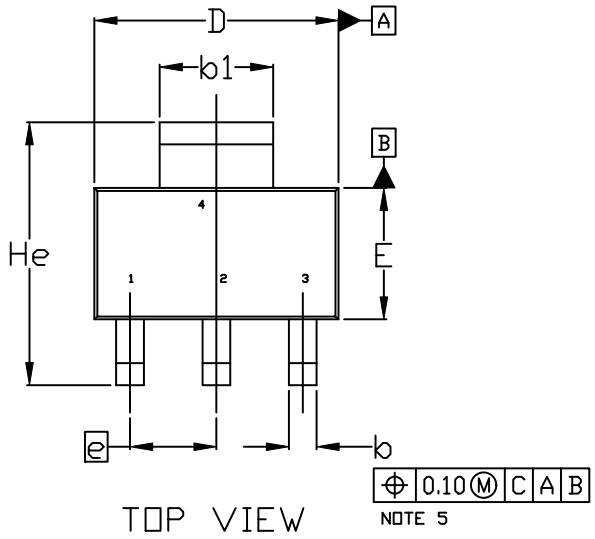
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

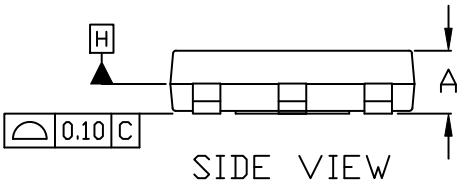
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

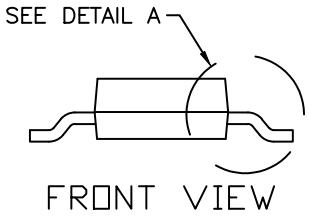
SCALE 1:1

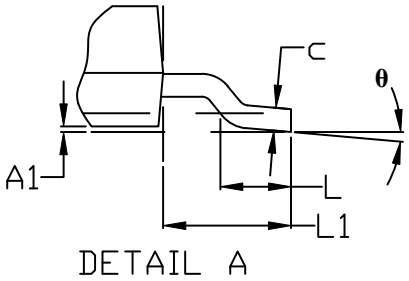
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



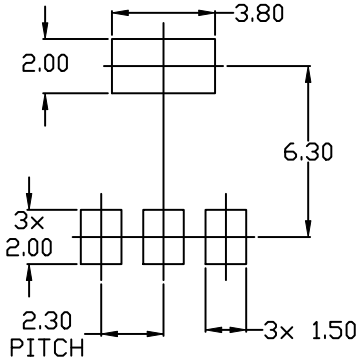






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

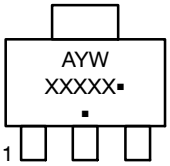
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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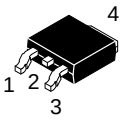
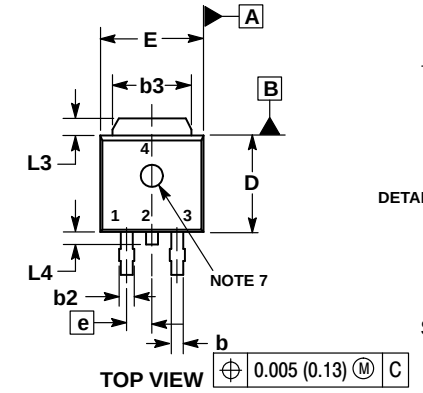
DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2



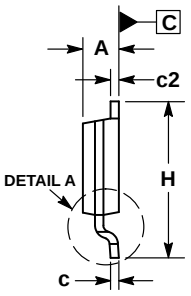
SCALE 1:1

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

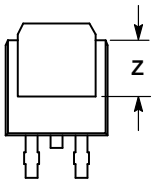
DATE 21 JUL 2015



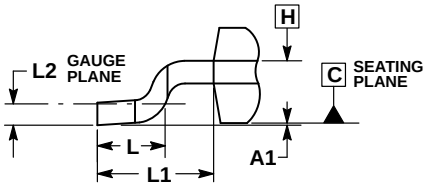
TOP VIEW



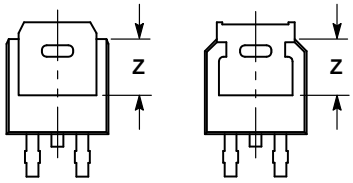
SIDE VIEW



BOTTOM VIEW



DETAIL A
ROTATED 90° CW



BOTTOM VIEW
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

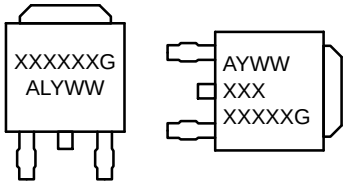
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

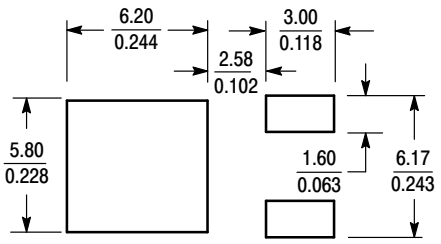


IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

PUBLICATION ORDERING INFORMATION

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