Power MOSFET

60 V, 28 m Ω , 26 A, Dual N-Channel

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R_{DS(on)} to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C680NLWF Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	٧
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain	Steady	T _C = 25°C	I _D	26	Α
Current R _{θJC} (Notes 1, 2, 3)		T _C = 100°C		13	
Power Dissipation	State	T _C = 25°C	P_{D}	19	W
R _{θJC} (Notes 1, 2)		T _C = 100°C		9.5	
Continuous Drain		T _A = 25°C	I _D	7.5	Α
Current R _{0JA} (Notes 1, 2, 3)	Steady	T _A = 100°C		5.3	
Power Dissipation	State	T _A = 25°C	P_{D}	3.0	W
R _{θJA} (Notes 1 & 2)		T _A = 100°C		1.5	
Pulsed Drain Current	$T_A = 25$	°C, t _p = 10 μs	I _{DM}	57	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to + 175	°C
Source Current (Body Diode)			Is	33	Α
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, I _{L(pk)} = 5 A)			E _{AS}	47	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	3.74	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	49	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

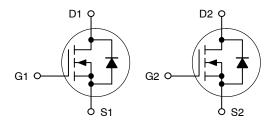


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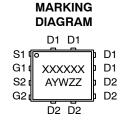
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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	28 mΩ @ 10 V	00.4
60 V	41 mΩ @ 4.5 V	26 A

Dual N-Channel







A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

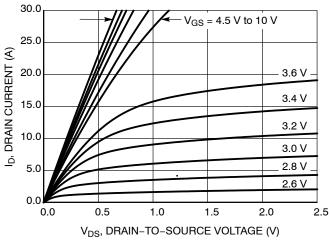
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit	
OFF CHARACTERISTICS							•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /				29		mV/°C	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, T _J = 25 °C				10		
		V _{DS} = 60 V	T _J = 125°C			100	μΑ	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V				100	nA	
ON CHARACTERISTICS (Note 4)					-			
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 13 \mu A$		1.2		2.2	V	
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-4.3		mV/°C	
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 5 A		23	28	28	
		V _{GS} = 4.5 V	I _D = 5 A		33	41	mΩ	
Forward Transconductance	9FS	V _{DS} = 15 V, I _D = 5 A			50		S	
CHARGES, CAPACITANCES & GATE RESISTANCE							•	
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V			350		pF	
Output Capacitance	C _{OSS}				150			
Reverse Transfer Capacitance	C _{RSS}				6			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 10 A			2.0			
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 10 A			5.0		1	
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 10 A			0.8		nC	
Gate-to-Source Charge	Q _{GS}				1.2			
Gate-to-Drain Charge	Q_{GD}				0.8			
Plateau Voltage	V _{GP}				3.0		V	
SWITCHING CHARACTERISTICS (Note 5)								
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 48 \text{ V},$ $I_{D} = 5 \text{ A}, R_{G} = 1.0 \Omega$			6.4			
Rise Time	t _r				25		- ns	
Turn-Off Delay Time	t _{d(OFF)}				13			
Fall Time	t _f				23			
DRAIN-SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.9	1.2	.,	
		I _S = 5 A	T _J = 125°C		0.8		_	
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dIS/dt = 10 A/μs, I _S = 5 A			17			
Charge Time	t _a				8		ns	
Discharge Time	t _b				9		1	
Reverse Recovery Charge	Q _{RR}				7		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300~\mu s$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

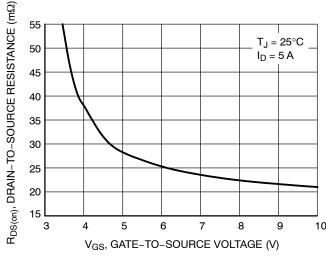
TYPICAL CHARACTERISTICS



V_{DS} = 10 V 45 40 _{ID}, DRAIN CURRENT (A) 35 $T_J = 25^{\circ}C$ 30 25 20 $T_J = -55^{\circ}C$ 15 10 5 $T_J = 125^{\circ}C$ 0 0 0.5 3 1.5 2.5 2 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



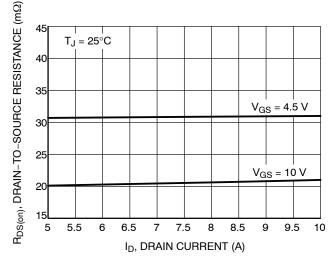
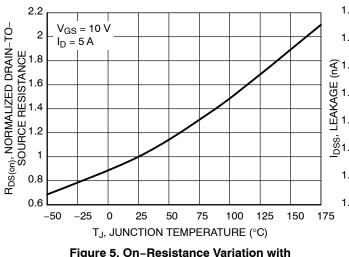


Figure 3. On-Resistance vs. Gate-to-Source Voltage

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



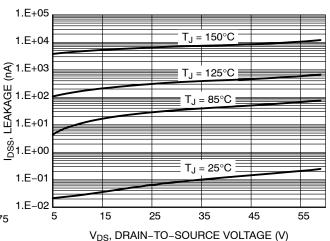


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

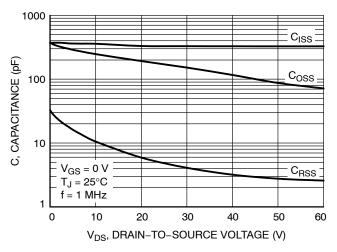


Figure 7. Capacitance Variation

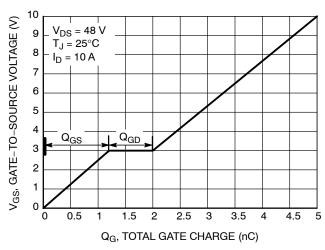


Figure 8. Gate-to-Source vs. Total Charge

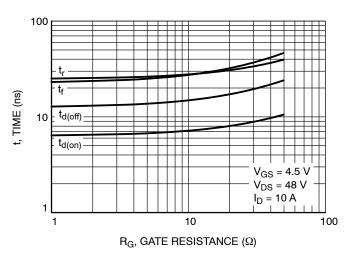


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

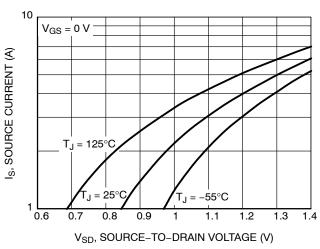


Figure 10. Diode Forward Voltage vs. Current

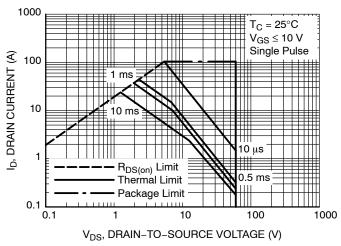


Figure 11. Maximum Rated Forward Biased Safe Operating Area

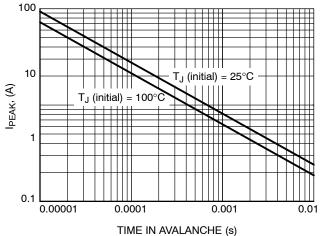


Figure 12. $I_{\mbox{\scriptsize PEAK}}$ vs. Time in Avalanche

TYPICAL CHARACTERISTICS

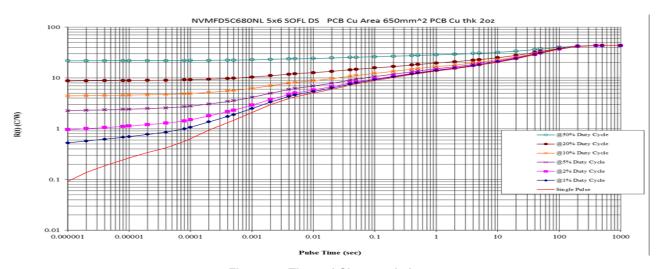


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

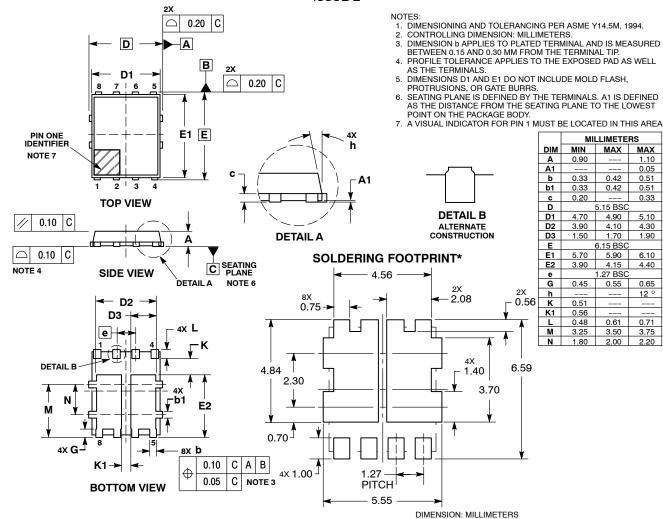
Device	Marking	Package	Shipping [†]
NVMFD5C680NLT1G	5C680L	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5C680NLWFT1G	680LWF	DFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT **ISSUE E**



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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