Power MOSFET

90 V, 17 m Ω , 50 A, Single N-Channel

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	90	V
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	٧
Continuous Drain Cur-		T _C = 25°C	I _D	50	Α
rent R _{θJC} (Notes 1 & 3)	Steady	$T_C = 100^{\circ}C$		35	
Power Dissipation R _{θJC}	State	T _C = 25°C	P_{D}	100	W
(Note 1)		$T_C = 100^{\circ}C$		50	
Continuous Drain		T _A = 25°C	I _D	10	Α
Current R _{θJA} (Notes 1, 2 & 3)	Steady	T _A = 100°C		7.0	
Power Dissipation R _{θJA}	State	T _A = 25°C	P_{D}	W	
(Notes 1 & 2)		T _A = 100°C		2.0	
Pulsed Drain Current	$T_A = 25^{\circ}$	C, t _p = 10 μs	I _{DM}	310	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 175	ç
Source Current (Body Diode)			I _S	50	Α
Single Pulse Drain-to-Source Avalanche Energy (T $_J$ = 25°C, V $_{GS}$ = 10 V, I $_{L(pk)}$ = 31 A, L = 0.3 mH, R $_{G}$ = 25 Ω)			E _{AS}	144	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Drain)	$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	38	

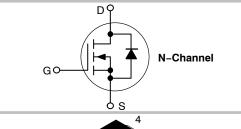
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- 2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
- Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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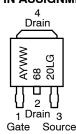
V _{(BR)DSS}	R _{DS(on)}	I _D	
90 V	16.7 mΩ @ 10 V	50 A	
	20.4 mΩ @ 4.5 V	30 A	





DPAK CASE 369C STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*

Y = Year WW = Work Week 6820L = Device Code G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter pin), the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping [†]
NVD6820NLT4G	DPAK (Pb-Free)	2500/Tape & Reel
NVD6820NLT4G- VF01	DPAK (Pb-Free)	2500/Tape & Reel

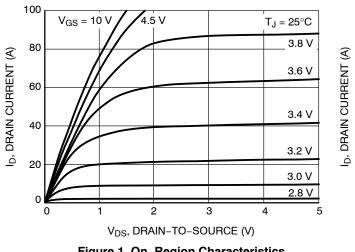
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Test Cond	ition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	<u>. </u>					•	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		90			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				87		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	Voc = 0 V	$T_J = 25^{\circ}C$			1.0	μΑ
		$V_{GS} = 0 V$, $V_{DS} = 90 V$	T _J = 125°C			100	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$				± 100	nA
ON CHARACTERISTICS (Note 4)						•	
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D$	= 250 μΑ	1.5		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J	do borb (-6.7		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _I	_O = 20 A		11.6	16.7	mΩ
	•	V _{GS} = 4.5 V, I	_D = 20 A		12.9	20.4	1
CHARGES, CAPACITANCES AND GA	TE RESISTANCE	S				•	
Input Capacitance	C _{iss}				4209		pF
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V, f} = V_{DS} = 29$	1.0 MHz,		253		1
Reverse Transfer Capacitance	C _{rss}	VDS - 23	, ,		187		1
Total Gate Charge	Q _{G(TOT)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 72 \text{ V},$ $I_{D} = 20 \text{ A}$ $V_{GS} = 10 \text{ V}, V_{DS} = 72 \text{ V},$ $I_{D} = 20 \text{ A}$			44		nC
	-				83		1
Threshold Gate Charge	Q _{G(TH)}				4.3		1
Gate-to-Source Charge	Q _{GS}	$V_{GS} = 10 \text{ V, } V_{D}$ $I_{D} = 20$	$_{0S} = 72 \text{ V},$		12.5		1
Gate-to-Drain Charge	Q_{GD}	ID - 20	A		22		1
SWITCHING CHARACTERISTICS (Not	e 5)				1		L
Turn-On Delay Time	t _{d(on)}				19		ns
Rise Time	t _r	Vcs = 10 V. Vr	nn = 72 V.		98		1
Turn-Off Delay Time	t _{d(off)}	V_{GS} = 10 V, V_{DD} = 72 V, I_{D} = 20 A, R_{G} = 2.5 Ω			36		1
Fall Time	t _f				59		1
DRAIN-SOURCE DIODE CHARACTER	RISTICS					•	
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	$T_J = 25^{\circ}C$		0.84	1.2	V
		I _S = 20 A	T _J = 125°C		0.72		7
Reverse Recovery Time	t _{RR}	V_{GS} = 0 V, dIs/dt = 100 A/ μ s, I _S = 20 A			39		ns
Charge Time	ta				27		1
Discharge Time	tb				12		1
Reverse Recovery Charge	Q_{RR}				55		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

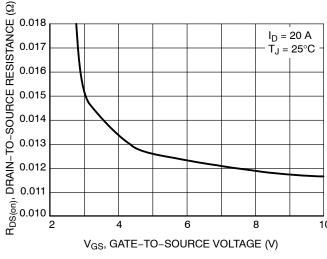
TYPICAL CHARACTERISTICS



100 $V_{DS} \ge 10 \text{ V}$ 80 60 40 T_J = 25°C 20 = 125 $T_J = -55^{\circ}C$ 0 2.0 3.0 3.5 4.0 V_{GS}, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



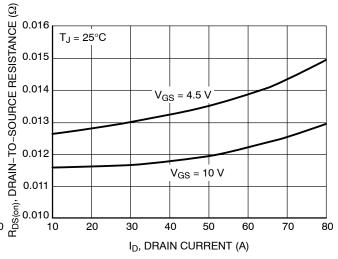
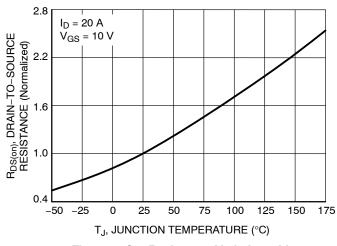


Figure 3. On-Resistance vs. Gate Voltage

Figure 4. On-Resistance vs. Drain Current and **Gate Voltage**



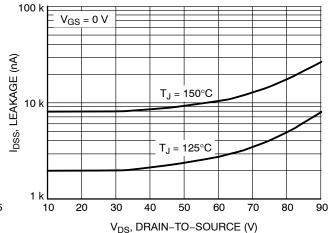


Figure 5. On-Resistance Variation with **Temperature**

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

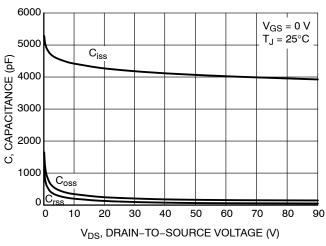


Figure 7. Capacitance Variation

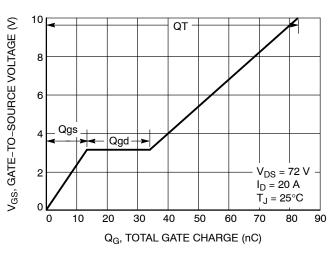


Figure 8. Gate-to-Source Voltage vs. Total Charge

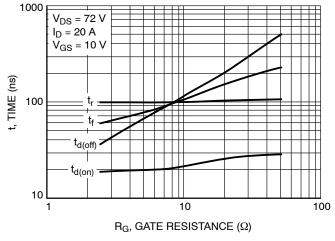


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

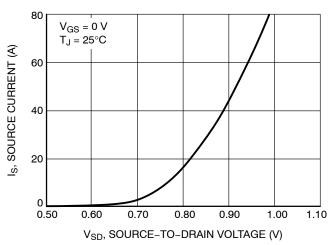


Figure 10. Diode Forward Voltage vs. Current

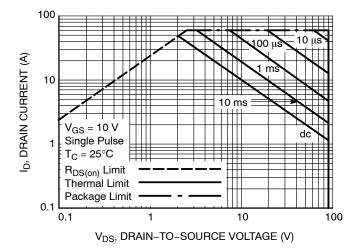


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

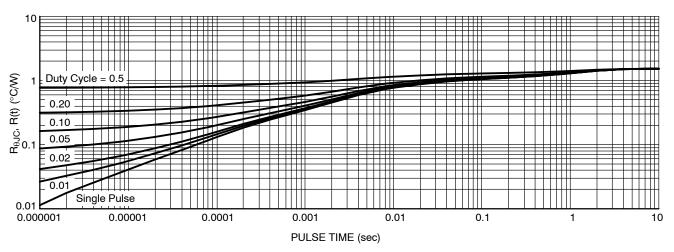
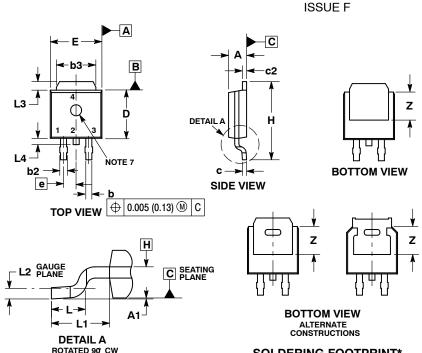


Figure 12. Thermal Response

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C



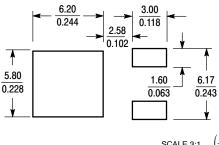
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME
- 714.5M, 1994.
 2. CONTROLLING DIMENSION: INCHES.
 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3. L3 and Z
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- 5. DIMENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.
 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIM	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX		
Α	0.086	0.094	2.18	2.38		
A1	0.000	0.005	0.00	0.13		
b	0.025	0.035	0.63	0.89		
b2	0.028	0.045	0.72	1.14		
b3	0.180	0.215	4.57	5.46		
С	0.018	0.024	0.46	0.61		
c2	0.018	0.024	0.46	0.61		
D	0.235	0.245	5.97	6.22		
E	0.250	0.265	6.35	6.73		
е	0.090	BSC	2.29	BSC		
Н	0.370	0.410	9.40	10.41		
L	0.055	0.070	1.40	1.78		
L1	0.114 REF		2.90	REF		
L2	0.020 BSC		0.51	BSC		
L3	0.035	0.050	0.89	1.27		
L4		0.040		1.01		
Z	0.155		3.93			

- STYLE 2: PIN 1. GATE

 - 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT*



mm SCALE 3:1

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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