

FDU5N60NZTU

N-Channel UniFET II MOSFET

600 V, 4 A, 2 Ω

UniFET II MOSFET is ON Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2 kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 1.65 \Omega$ (Typ.) @ $V_{GS} = 10 V, I_D = 2 A$
- Low Gate Charge (Typ. 10 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- These Devices are Pb-Free and are RoHS Compliant

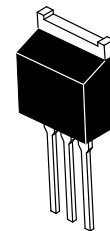
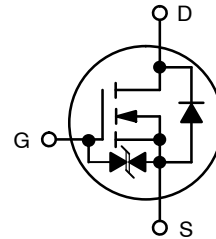
Applications

- LCD / LED TV
- Lighting
- Charger / Adapter



ON Semiconductor®

www.onsemi.com



IPAK3
CASE 369AR

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

FDU5N60NZTU

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-to-Source Voltage	600	V
V _{GSS}	Gate-to-Source Voltage	±25	V
I _D	Drain Current	Continuous (T _C = 25°C)	4
		Continuous (T _C = 100°C)	2.4
I _{DM}	Drain Current	Pulsed (Note 1)	16
E _{AS}	Single Pulse Avalanche Energy (Note 2)	216	mJ
I _{AR}	Avalanche Current (Note 1)	4	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	8.3	mJ
dv/dt	Peak Diode Recovery (Note 3)	10	V/ns
P _D	Power Dissipation	T _C = 25°C	83
		Derate Above 25°C	0.7
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purposes (1/8" from case for 5 seconds)	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 4 A, V_{DD} = 50 V, L = 27 mH, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 4 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case, Max.	1.5	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max.	90	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDU5N60NZTU	FDU5N60NZ	IPAK	Tube	N/A	N/A	75 units

FDU5N60NZTU

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_J = 25^\circ\text{C}$	600	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.6	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	50	μA
		$V_{DS} = 480 \text{ V}$, $T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate-to-Body Leakage Current	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-to-Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$	-	1.65	2.00	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 2 \text{ A}$	-	5	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	450	600	μF
C_{oss}	Output Capacitance		-	50	65	
C_{riss}	Reverse Transfer Capacitance		-	5	7.5	
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400 \text{ V}$, $I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ (Note 4)	-	10	13	nC
Q_{gs}	Gate-to-Source Gate Charge		-	2.5	-	
Q_{gd}	Gate-to-Drain "Miller" Charge		-	4	-	

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}$, $I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 25 \Omega$ (Note 4)	-	15	40	ns
t_r	Turn-On Rise Time		-	20	50	
$t_{d(off)}$	Turn-Off Delay Time		-	35	80	
t_f	Turn-Off Fall Time		-	20	50	

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	4	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	16		
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 4 \text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 4 \text{ A}$, $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	230	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.9	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of Operating Temperature Typical Characteristics.

FDU5N60NZTU

TYPICAL CHARACTERISTICS

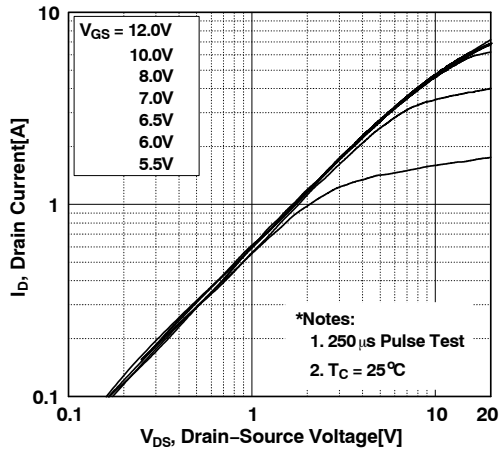


Figure 1. On-Region Characteristics

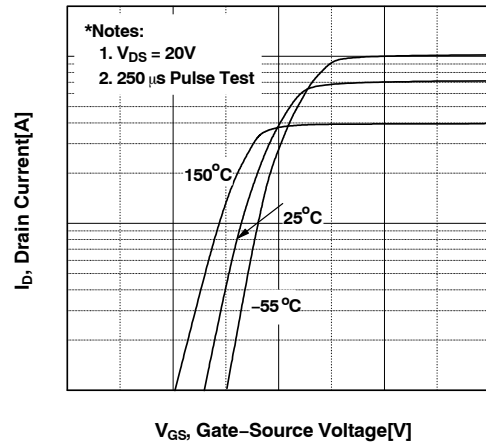


Figure 2. Transfer Characteristics

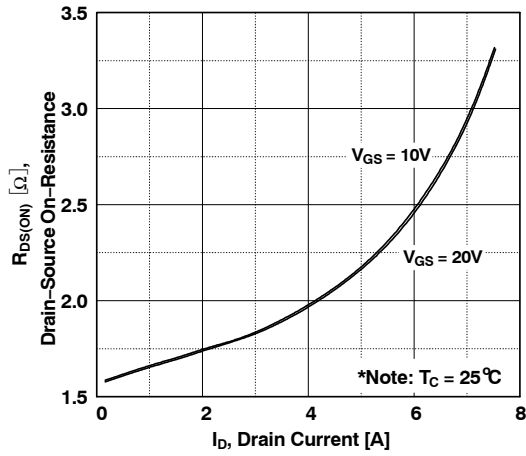


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

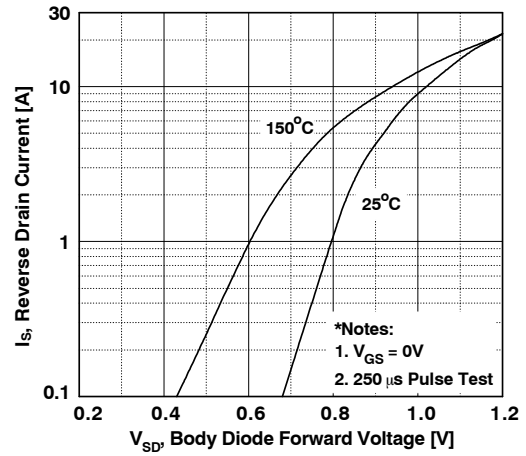


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

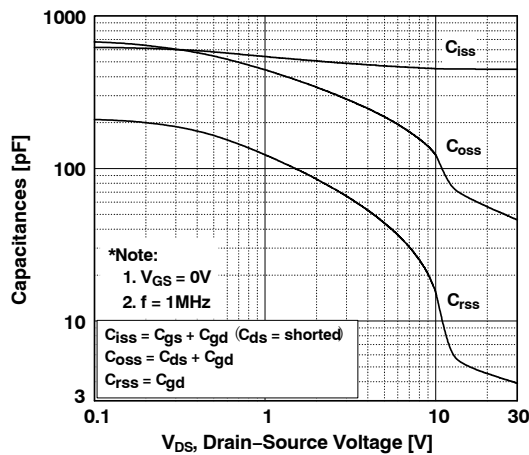


Figure 5. Capacitance Characteristics

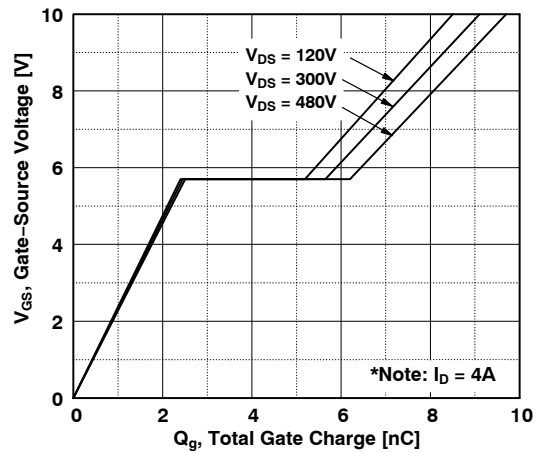


Figure 6. Gate Charge Characteristics

FDU5N60NZTU

TYPICAL CHARACTERISTICS

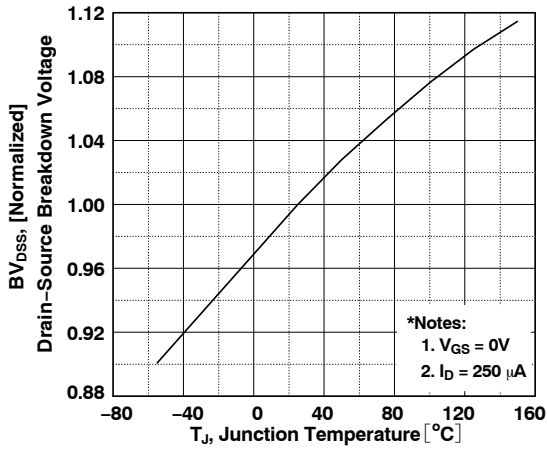


Figure 7. Breakdown Voltage Variation vs. Temperature

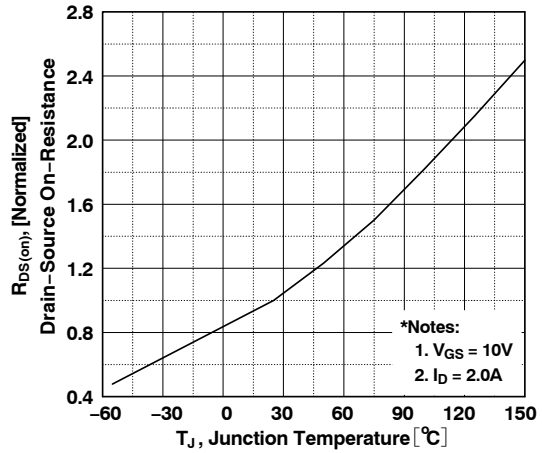


Figure 8. On-Resistance Variation vs. Temperature

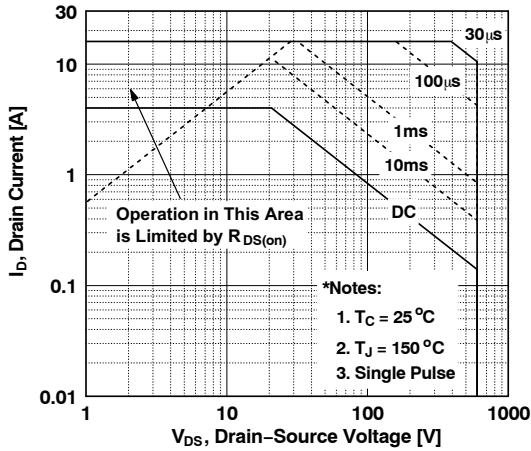


Figure 9. Maximum Safe Operating Area

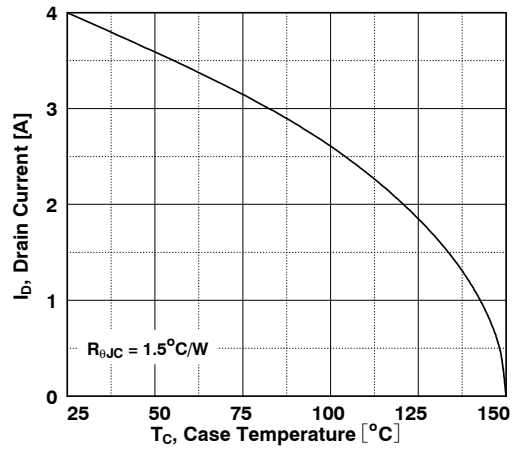


Figure 10. Maximum Drain Current vs. Case Temperature

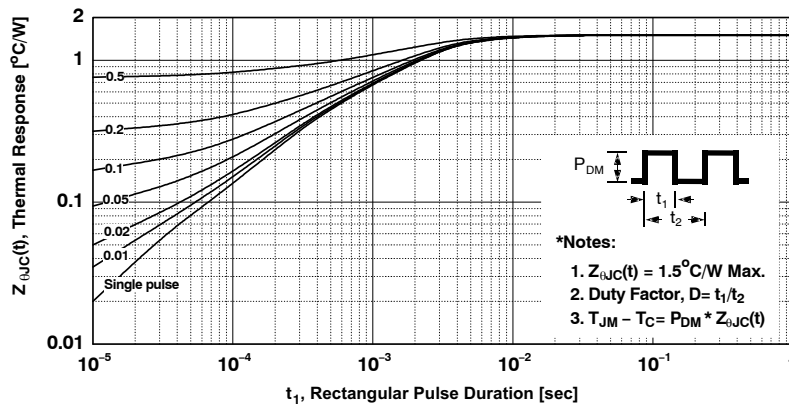


Figure 11. Transient Thermal Response Curve

FDU5N60NZTU

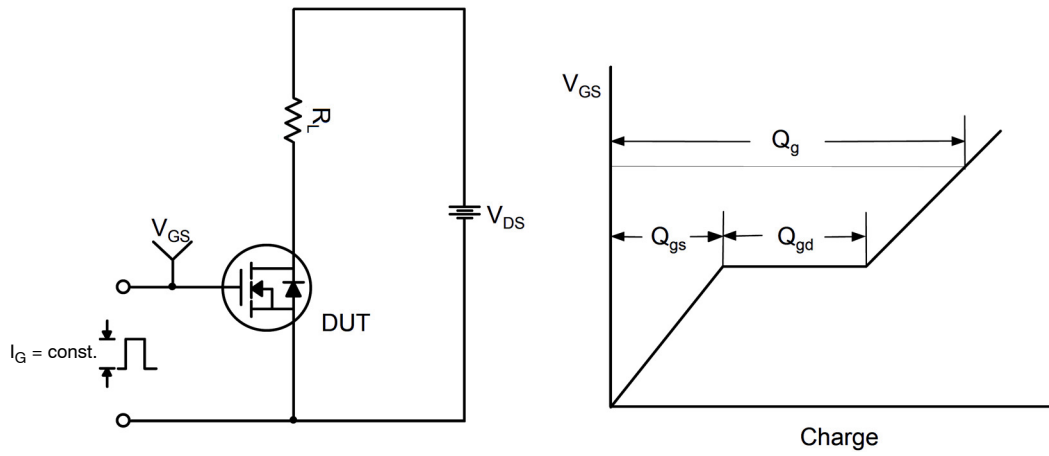


Figure 12. Gate Charge Test Circuit & Waveform

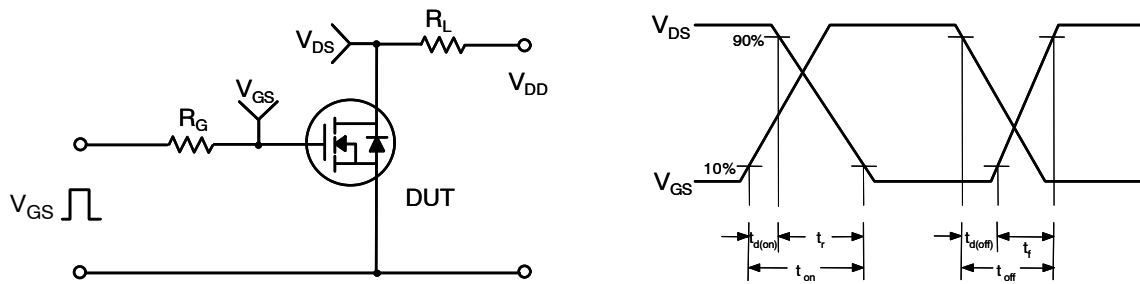


Figure 13. Resistive Switching Test Circuit & Waveforms

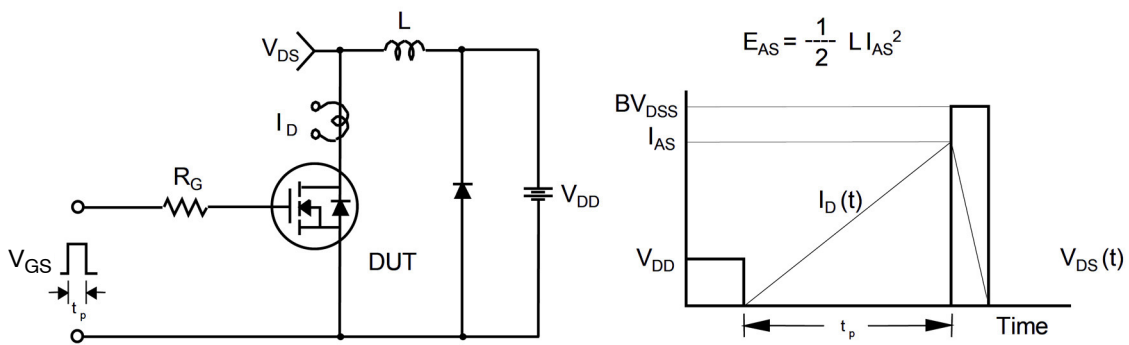


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FDU5N60N2TU

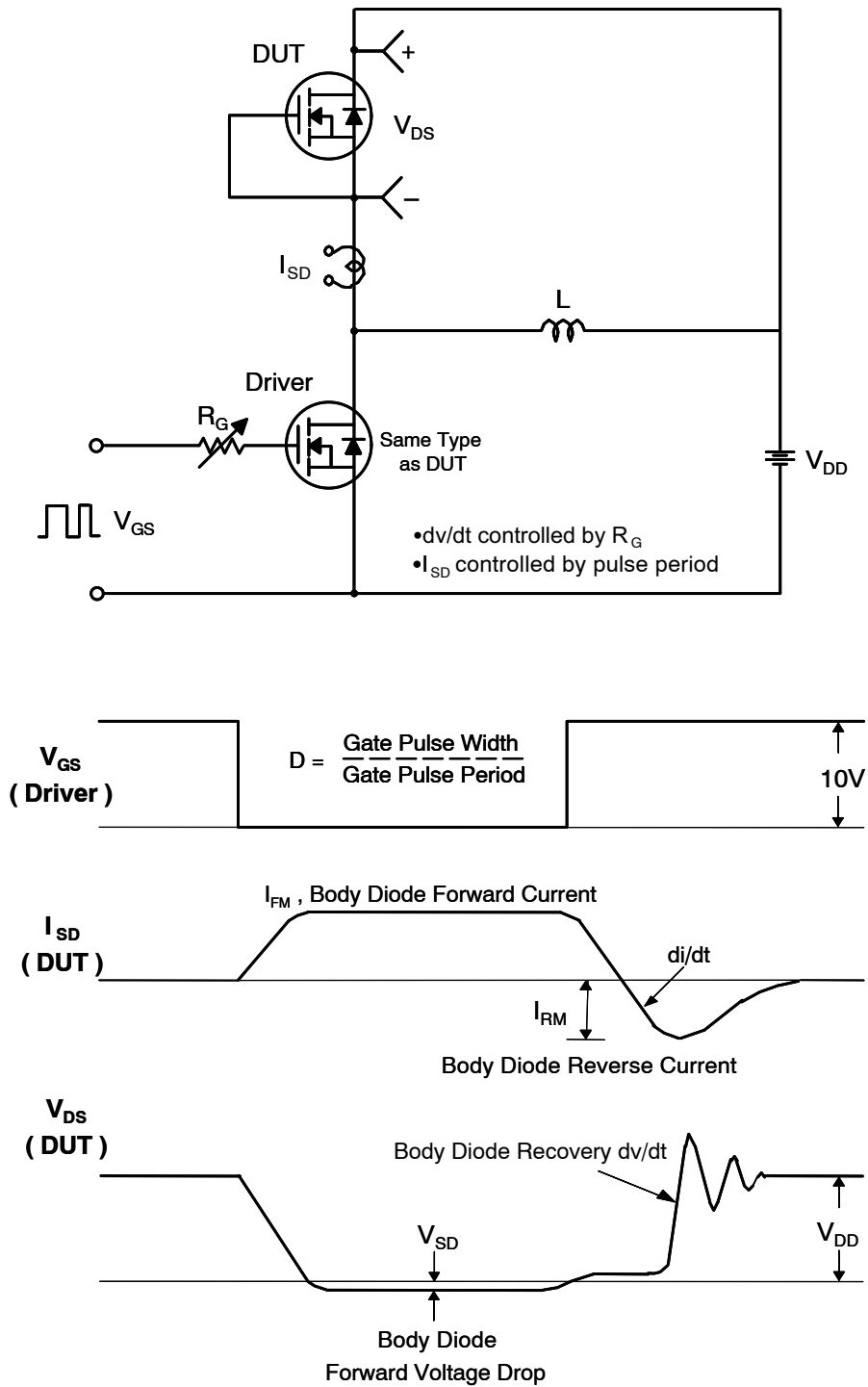
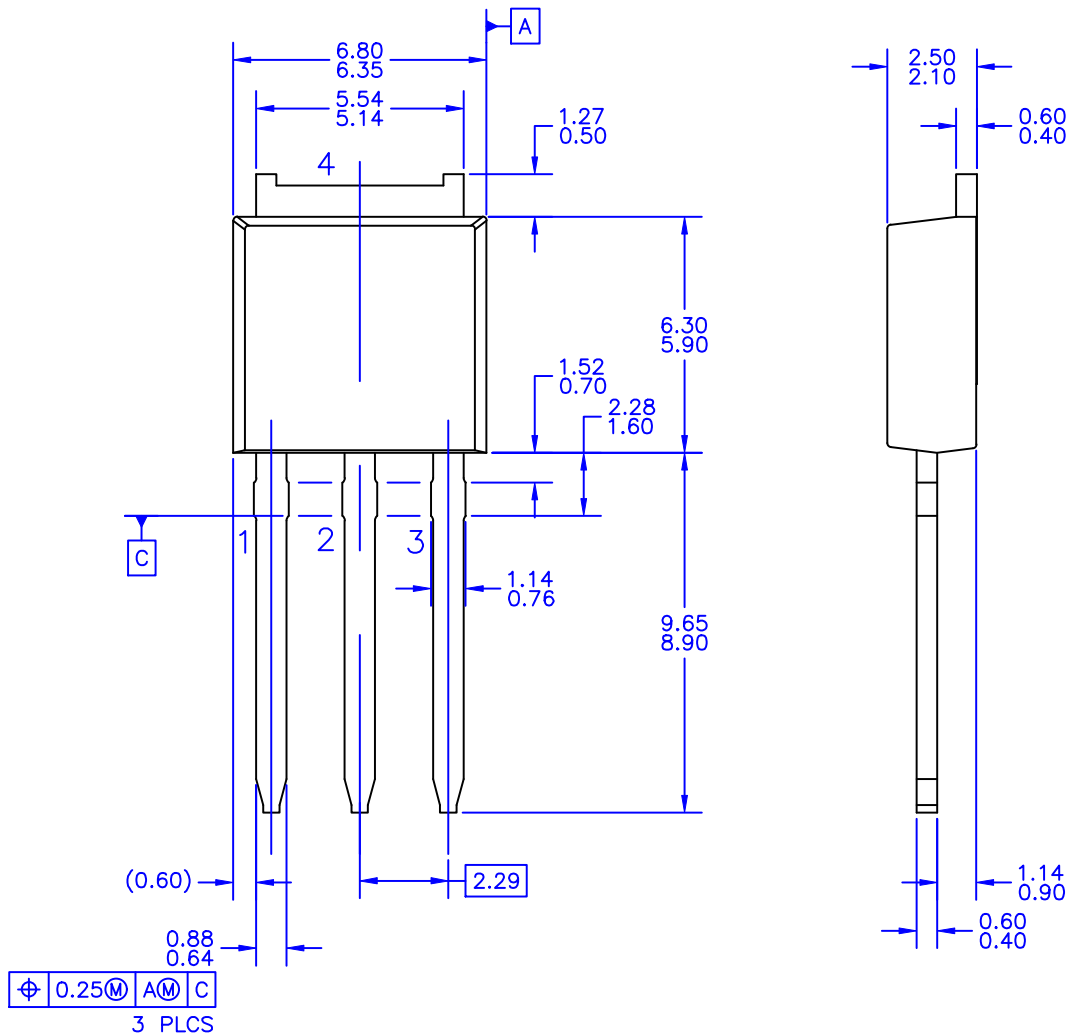


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FDU5N60NZTU

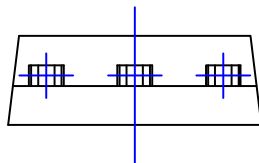
PACKAGE DIMENSIONS

DPAK3 (IPAK)
CASE 369AR
ISSUE O




NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-251, ISSUE C, VARIATION AA, DATED SEP 1988.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.



FDU5N60NZTU

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative