# 8-Bit Serial-Input/Parallel-Output Shift Register

# **High-Performance Silicon-Gate CMOS**

The MC74HC164B is identical in pinout to the LS164. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The MC74HC164B is an 8-bit, serial-input to parallel-output shift register. Two serial data inputs, A1 and A2, are provided so that one input may be used as a data enable. Data is entered on each rising edge of the clock. The active-low asynchronous Reset overrides the Clock and Serial Data inputs. Schmitt-trigger action at the Clock input enhances the device's tolerance to slower rise and fall times and immunity to noise of the input clock signal.

#### **Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 V to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 244 FETs or 61 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant



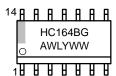
# ON Semiconductor®

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MARKING DIAGRAMS



SOIC-14 D SUFFIX CASE 751A





TSSOP-14 DT SUFFIX CASE 948G



A = Assembly Location

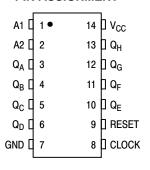
L, WL = Wafer Lot Y = Year W, WW = Work Week G or ■ = Pb-Free Package

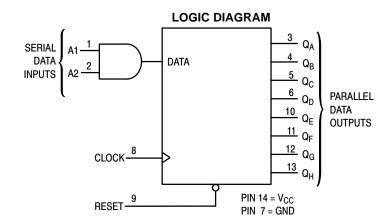
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# **PIN ASSIGNMENT**





# **FUNCTION TABLE**

| Inputs |       |    |    | Outp  | outs     |     |          |
|--------|-------|----|----|-------|----------|-----|----------|
| Reset  | Clock | A1 | A2 | $Q_A$ | $Q_{B}$  |     | $Q_{H}$  |
| L      | Х     | Х  | Х  | L     | L        |     | L        |
| Н      | ~     | Х  | Χ  | 1     | No Ch    | ang | е        |
| Н      |       | Н  | D  | D     | $Q_{An}$ |     | $Q_{Gn}$ |
| Н      |       | D  | Н  | D     | $Q_{An}$ |     | $Q_{Gn}$ |

D = data input

 $Q_{An} - Q_{Gn}$  = data shifted from the preceding stage on a rising edge at the clock input.

### **ORDERING INFORMATION**

| Device            | Package                  | Shipping <sup>†</sup> |
|-------------------|--------------------------|-----------------------|
| MC74HC164BDG      |                          | 55 Units / Rail       |
| MC74HC164BDR2G    | SOIC-14<br>(Pb-Free)     | 2500 / Tape & Reel    |
| NLV74HC164BDR2G*  | (1.2.1.00)               | 2500 / Tape & Reel    |
| MC74HC164BDTR2G   | 1C74HC164BDTR2G TSSOP-14 |                       |
| NLV74HC164BDTR2G* | (Pb-Free)                | 2500 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

#### **MAXIMUM RATINGS**

| Symbol           | Parameter   | Value                    | Unit |
|------------------|---|--------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)                                   | - 0.5 to + 7.0           | V    |
| V <sub>in</sub>  | DC Input Voltage (Referenced to GND)                                    | $-0.5$ to $V_{CC} + 0.5$ | V    |
| V <sub>out</sub> | DC Output Voltage (Referenced to GND)                                   | $-0.5$ to $V_{CC} + 0.5$ | V    |
| I <sub>in</sub>  | DC Input Current, per Pin   | ± 20                     | mA   |
| I <sub>out</sub> | DC Output Current, per Pin  | ± 25                     | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                         | ± 50                     | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air, SOIC Package† TSSOP Package†            | 500<br>450               | mW   |
| T <sub>stg</sub> | Storage Temperature   | - 65 to + 150            | °C   |
| TL               | Lead Temperature, 1 mm from Case for 10 Seconds (SOIC or TSSOP Package) | 260                      | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 mW/°C from 65° to 125°C

#### RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                   |  |             | Max                              | Unit |
|------------------------------------|---|--|-------------|----------------------------------|------|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)       |  |             | 6.0                              | V    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Refe GND) | erenced to   | 0           | V <sub>CC</sub>                  | V    |
| T <sub>A</sub>                     | Operating Temperature, All Package Ty       | - 55   | + 125       | °C                               |      |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time<br>(Figure 1)      | $V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 0<br>0<br>0 | No Limit<br>No Limit<br>No Limit | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

|                                |   |   |                          | Gu                           | aranteed Li                  | mit                          |      |
|--------------------------------|---|---|--------------------------|------------------------------|------------------------------|------------------------------|------|
| Symbol                         | Parameter   | Test Conditions   | V <sub>CC</sub><br>V     | –55°C to<br>25°C             | ≤ <b>85</b> °C               | ≤ 125°C                      | Unit |
| V <sub>T+</sub><br>max         | Maximum Positive–Going Input<br>Threshold Voltage<br>(Figure 3) | $V_{out} = 0.1V$ $ I_{out}  \le 20\mu A$  | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.15<br>3.15<br>4.20 | 1.50<br>2.15<br>3.15<br>4.20 | 1.50<br>2.15<br>3.15<br>4.20 | V    |
| V <sub>T+</sub> min            | Minimum Positive–Going Input<br>Threshold Voltage<br>(Figure 3) | $V_{out} = 0.1V$ $ I_{out}  \le 20\mu A$  | 2.0<br>3.0<br>4.5<br>6.0 | 1.0<br>1.5<br>2.3<br>3.0     | 0.95<br>1.45<br>2.25<br>2.95 | 0.95<br>1.45<br>2.25<br>2.95 | V    |
| V <sub>T-</sub><br>max         | Maximum Negative-Going Input<br>Threshold Voltage<br>(Figure 3) | $V_{out} = V_{CC} - 0.1V$ $ I_{out}  \le 20\mu A$   | 2.0<br>3.0<br>4.5<br>6.0 | 0.9<br>1.4<br>2.0<br>2.6     | 0.95<br>1.45<br>2.05<br>2.65 | 0.95<br>1.45<br>2.05<br>2.65 | V    |
| V <sub>T</sub> min             | Minimum Negative-Going Input<br>Threshold Voltage<br>(Figure 3) | $V_{out} = V_{CC} - 0.1V$ $ I_{out}  \le 20\mu A$   | 2.0<br>3.0<br>4.5<br>6.0 | 0.3<br>0.5<br>0.9<br>1.2     | 0.3<br>0.5<br>0.9<br>1.2     | 0.3<br>0.5<br>0.9<br>1.2     | V    |
| V <sub>H</sub> max<br>(Note 1) | Maximum Hysteresis Voltage<br>(Figure 3)                        | $V_{out} = 0.1V$ or $V_{CC} - 0.1V$<br>$ I_{out}  \le 20\mu A$  | 2.0<br>3.0<br>4.5<br>6.0 | 1.20<br>1.65<br>2.25<br>3.00 | 1.20<br>1.65<br>2.25<br>3.00 | 1.20<br>1.65<br>2.25<br>3.00 | V    |
| V <sub>H</sub> min<br>(Note 1) | Minimum Hysteresis Voltage<br>(Figure 3)                        | $V_{out} = 0.1V \text{ or } V_{CC} - 0.1V$<br>$ I_{out}  \le 20\mu\text{A}$   | 2.0<br>3.0<br>4.5<br>6.0 | 0.20<br>0.25<br>0.40<br>0.50 | 0.20<br>0.25<br>0.40<br>0.50 | 0.20<br>0.25<br>0.40<br>0.50 | V    |
| V <sub>OH</sub>                | Minimum High-Level Output<br>Voltage                            | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20 \ \mu\text{A}$  | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | 1.9<br>4.4<br>5.9            | V    |
|                                |   | $\begin{split} V_{\text{in}} = V_{\text{IH}} \text{ or } V_{\text{IL}} &   I_{\text{out}}  \leq 2.4 \text{ mA} \\  I_{\text{out}}  \leq 4.0 \text{ mA} \\  I_{\text{out}}  \leq 5.2 \text{ mA} \end{split}$ | 3.0<br>4.5<br>6.0        | 2.48<br>3.98<br>5.48         | 2.34<br>3.84<br>5.34         | 2.20<br>3.70<br>5.20         |      |
| V <sub>OL</sub>                | Maximum Low–Level Output<br>Voltage                             | $V_{in} = V_{IH} \text{ or } V_{IL}$<br>$ I_{out}  \le 20  \mu\text{A}$   | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | 0.1<br>0.1<br>0.1            | V    |
|                                |   | $\begin{aligned} V_{in} = V_{IH} \text{ or } V_{IL} & &  I_{out}  \leq 2.4 \text{ mA} \\ &  I_{out}  \leq 4.0 \text{ mA} \\ &  I_{out}  \leq 5.2 \text{ mA} \end{aligned}$                                  | 3.0<br>4.5<br>6.0        | 0.26<br>0.26<br>0.26         | 0.33<br>0.33<br>0.33         | 0.40<br>0.40<br>0.40         |      |
| l <sub>in</sub>                | Maximum Input Leakage Current                                   | $V_{in} = V_{CC}$ or GND  | 6.0                      | ± 0.1                        | ± 1.0                        | ± 1.0                        | μΑ   |
| Icc                            | Maximum Quiescent Supply Current (per Package)                  | $V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$  | 6.0                      | 4                            | 40                           | 160                          | μΑ   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 1.  $V_H min > (V_{T+} min) - (V_{T-} max); V_H max = (V_{T+} max) - (V_{T-} min).$ 

# AC ELECTRICAL CHARACTERISTICS ( $C_L$ = 50 pF, Input $t_{\rm f}$ = $t_{\rm f}$ = 6 ns)

|  |  |                          | Gu                     | aranteed Li            | mit                    |      |
|--|--|--------------------------|------------------------|------------------------|------------------------|------|
| Symbol                                 | Parameter  | V <sub>CC</sub>          | –55°C to<br>25°C       | ≤ 85°C                 | ≤ 125°C                | Unit |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)   | 2.0<br>3.0<br>4.5<br>6.0 | 10<br>20<br>40<br>50   | 10<br>20<br>35<br>45   | 10<br>20<br>30<br>40   | MHz  |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q (Figures 1 and 4)      | 2.0<br>3.0<br>4.5<br>6.0 | 160<br>100<br>32<br>27 | 200<br>150<br>40<br>34 | 250<br>200<br>48<br>42 | ns   |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to Q (Figures 2 and 4)      | 2.0<br>3.0<br>4.5<br>6.0 | 175<br>100<br>35<br>30 | 220<br>150<br>44<br>37 | 260<br>200<br>53<br>45 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13   | 95<br>32<br>19<br>16   | 110<br>36<br>22<br>19  | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                    | _                        | 10                     | 10                     | 10                     | pF   |

|          |  | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |    |
|----------|--|---|----|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)* | 180                                     | pF |

# **TIMING REQUIREMENTS** (Input $t_r = t_f = 6 \text{ ns}$ )

|                  |   |                          | Gu                   | aranteed Li          | mit                  |      |
|------------------|---|--------------------------|----------------------|----------------------|----------------------|------|
| Symbol           | Parameter   | v <sub>cc</sub>          | –55°C to<br>25°C     | ≤ 85°C               | ≤ 125°C              | Unit |
| t <sub>su</sub>  | Minimum Setup Time, A1 or A2 to Clock<br>(Figure 3)       | 2.0<br>3.0<br>4.5<br>6.0 | 25<br>15<br>7<br>5   | 35<br>20<br>8<br>6   | 40<br>25<br>9<br>6   | ns   |
| t <sub>h</sub>   | Minimum Hold Time, Clock to A1 or A2 (Figure 3)           | 2.0<br>3.0<br>4.5<br>6.0 | 3<br>3<br>3          | 3<br>3<br>3<br>3     | 3<br>3<br>3<br>3     | ns   |
| t <sub>rec</sub> | Minimum Recovery Time, Reset Inactive to Clock (Figure 2) | 2.0<br>3.0<br>4.5<br>6.0 | 3<br>3<br>3<br>3     | 3<br>3<br>3<br>3     | 3<br>3<br>3<br>3     | ns   |
| t <sub>W</sub>   | Minimum Pulse Width, Clock<br>(Figure 1)                  | 2.0<br>3.0<br>4.5<br>6.0 | 50<br>26<br>12<br>10 | 60<br>35<br>15<br>12 | 75<br>45<br>20<br>15 | ns   |
| t <sub>w</sub>   | Minimum Pulse Width, Reset<br>(Figure 2)                  | 2.0<br>3.0<br>4.5<br>6.0 | 50<br>26<br>12<br>10 | 60<br>35<br>15<br>12 | 75<br>45<br>20<br>15 | ns   |

#### PIN DESCRIPTIONS

#### **INPUTS**

# A1, A2 (Pins 1, 2)

Serial Data Inputs. Data at these inputs determine the data to be entered into the first stage of the shift register. For a high level to be entered into the shift register, both A1 and A2 inputs must be high, thereby allowing one input to be used as a data—enable input. When only one serial input is used, the other must be connected to  $V_{CC}$ .

### Clock (Pin 8)

Shift Register Clock. A positive—going transition on this pin shifts the data at each stage to the next stage. The shift

register is completely static, allowing clock rates down to DC in a continuous or intermittent mode.

#### **OUTPUTS**

# Q<sub>A</sub> - Q<sub>H</sub> (Pins 3, 4, 5, 6, 10, 11, 12, 13)

Parallel Shift Register Outputs. The shifted data is presented at these outputs in true, or noninverted, form.

#### **CONTROL INPUT**

### Reset (Pin 9)

Active–Low, Asynchronous Reset Input. A low voltage applied to this input resets all internal flip–flops and sets Outputs  $Q_A - Q_H$  to the low level state.

#### SWITCHING WAVEFORMS

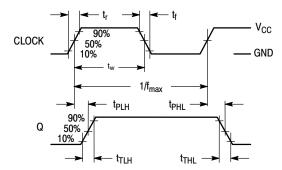


Figure 1.

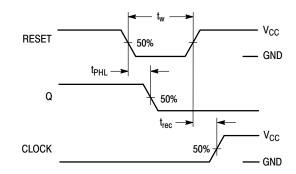


Figure 2.

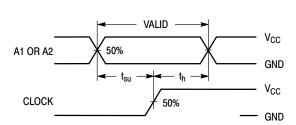
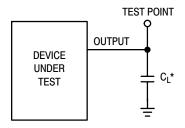


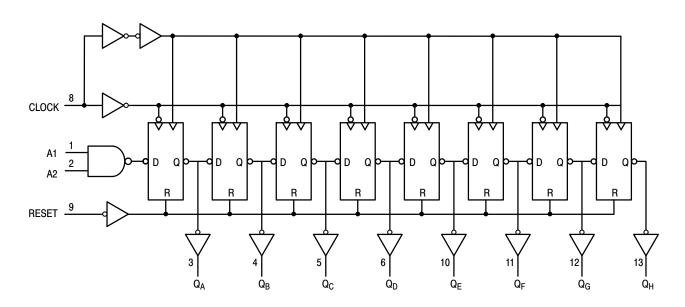
Figure 3.



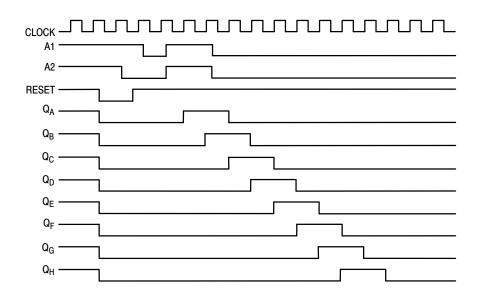
\*Includes all probe and jig capacitance

Figure 4. Test Circuit

# **EXPANDED LOGIC DIAGRAM**

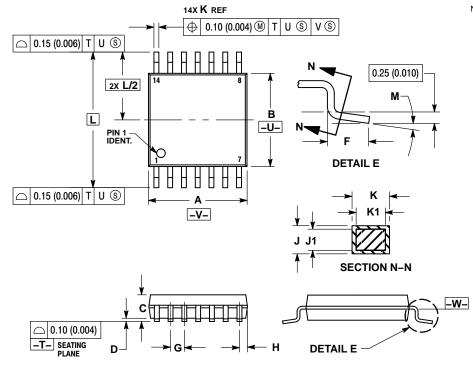


# **TIMING DIAGRAM**



#### **PACKAGE DIMENSIONS**

## TSSOP-14 **DT SUFFIX** CASE 948G **ISSUE B**



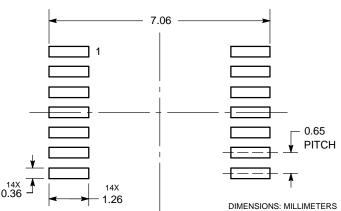
- JIES:

  1. DIMENSIONING AND TOLERANCING PER
  ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD
  FLASH, PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
  INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE
- DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08
  (0.003) TOTAL IN EXCESS OF THE K
  DIMENSION AT MAXIMUM MATERIAL
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

|     | MILLIN | IETERS | INC       | HES   |
|-----|--------|--------|-----------|-------|
| DIM | MIN    | MAX    | MIN       | MAX   |
| Α   | 4.90   | 5.10   | 0.193     | 0.200 |
| В   | 4.30   | 4.50   | 0.169     | 0.177 |
| С   |        | 1.20   |           | 0.047 |
| D   | 0.05   | 0.15   | 0.002     | 0.006 |
| F   | 0.50   | 0.75   | 0.020     | 0.030 |
| G   | 0.65   | BSC    | 0.026 BSC |       |
| Н   | 0.50   | 0.60   | 0.020     | 0.024 |
| J   | 0.09   | 0.20   | 0.004     | 0.008 |
| J1  | 0.09   | 0.16   | 0.004     | 0.006 |
| K   | 0.19   | 0.30   | 0.007     | 0.012 |
| K1  | 0.19   | 0.25   | 0.007     | 0.010 |
| L   | 6.40   |        | 0.252 BSC |       |
| М   | 0°     | 8 °    | 0°        | 8 °   |

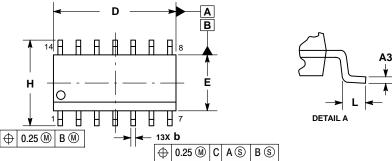
#### **SOLDERING FOOTPRINT\***



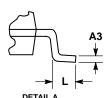
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

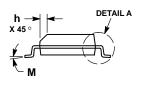
### PACKAGE DIMENSIONS

### SOIC-14 NB CASE 751A-03 ISSUE K



14X 0.58 C SEATING PLANE





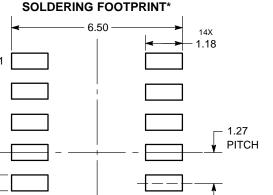
#### NOTES:

- AOTES.

  1. DIMENSIONING AND TOLERANCING PER
  ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR
- PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

  5. MAXIMUM MOLD PROTRUSION 0.15 PER

|     | MILLIN | IETERS   | INC   | HES   |
|-----|--------|----------|-------|-------|
| DIM | MIN    | MAX      | MIN   | MAX   |
| Α   | 1.35   | 1.75     | 0.054 | 0.068 |
| A1  | 0.10   | 0.25     | 0.004 | 0.010 |
| A3  | 0.19   | 0.25     | 0.008 | 0.010 |
| b   | 0.35   | 0.49     | 0.014 | 0.019 |
| D   | 8.55   | 8.75     | 0.337 | 0.344 |
| Е   | 3.80   | 4.00     | 0.150 | 0.157 |
| е   | 1.27   | 1.27 BSC |       | BSC   |
| Н   | 5.80   | 6.20     | 0.228 | 0.244 |
| h   | 0.25   | 0.50     | 0.010 | 0.019 |
| L   | 0.40   | 1.25     | 0.016 | 0.049 |
| М   | 0 °    | 7°       | 0 °   | 7°    |



**DIMENSIONS: MILLIMETERS** 

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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