



# NVMFS5C410N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V	T <sub>J</sub> = 25 °C		10	μA
			T <sub>J</sub> = 125°C		100	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.5		3.5	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-8.6		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		0.76	0.92	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A		190		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V		6100		pF
Output Capacitance	C <sub>OSS</sub>			3400		
Reverse Transfer Capacitance	C <sub>RSS</sub>			70		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V; I <sub>D</sub> = 50 A		86		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V; I <sub>D</sub> = 50 A		18		
Gate-to-Source Charge	Q <sub>GS</sub>			28		
Gate-to-Drain Charge	Q <sub>GD</sub>			14		
Plateau Voltage	V <sub>GP</sub>			4.9		

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 50 A, R <sub>G</sub> = 2.5 Ω		54		ns
Rise Time	t <sub>r</sub>			162		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			227		
Fall Time	t <sub>f</sub>			173		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 50 A	T <sub>J</sub> = 25°C		0.8	1.2	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 50 A		91		ns	
Charge Time	t <sub>a</sub>			42			
Discharge Time	t <sub>b</sub>			49			
Reverse Recovery Charge	Q <sub>RR</sub>			159			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

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## TYPICAL CHARACTERISTICS

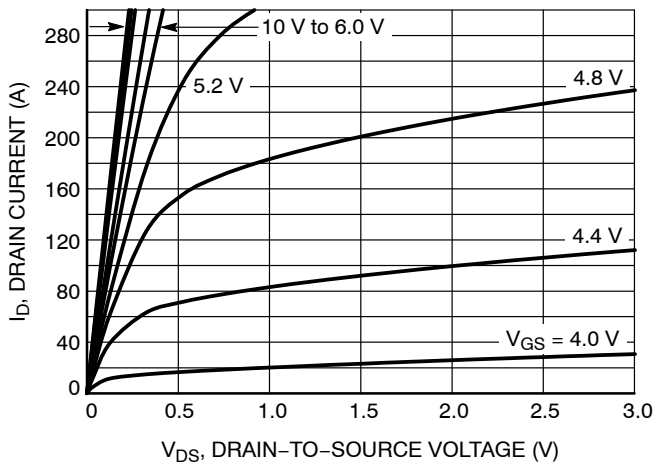


Figure 1. On-Region Characteristics



Figure 2. Transfer Characteristics

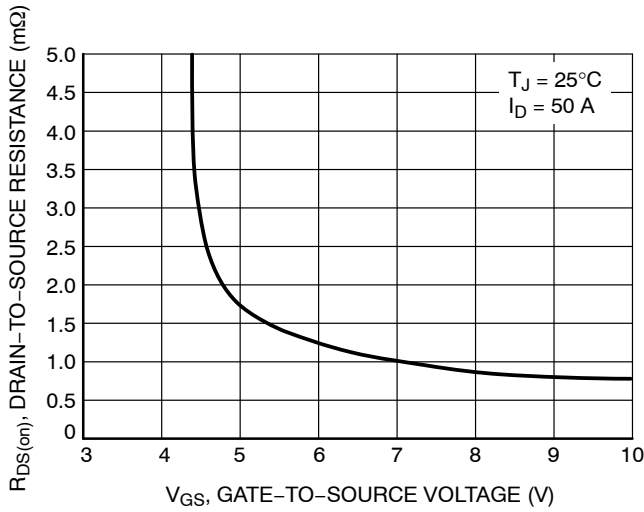


Figure 3. On-Resistance vs. Gate-to-Source Voltage

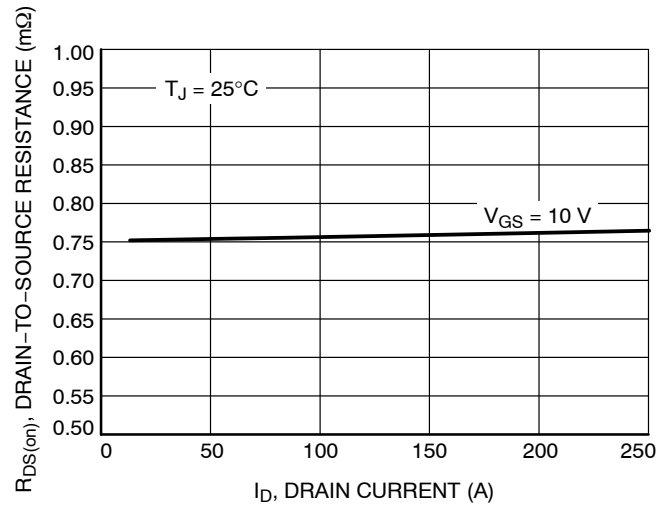


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

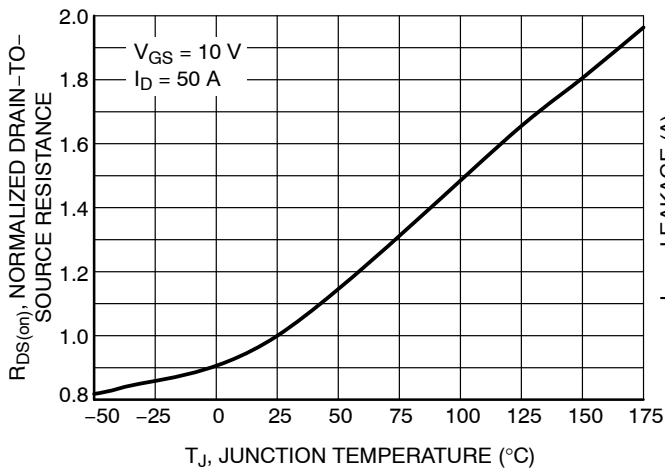


Figure 5. On-Resistance Variation with Temperature

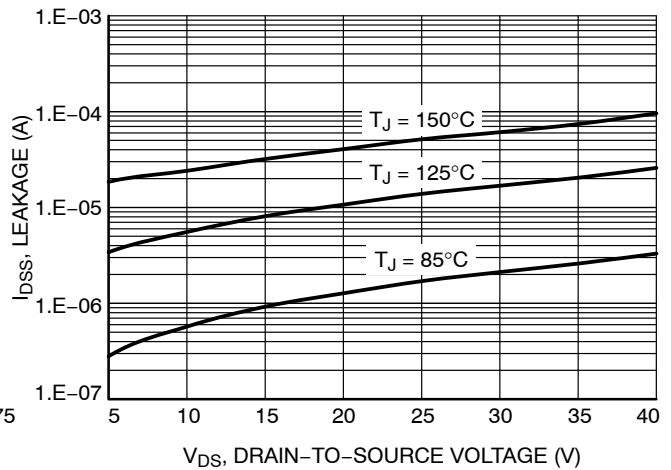
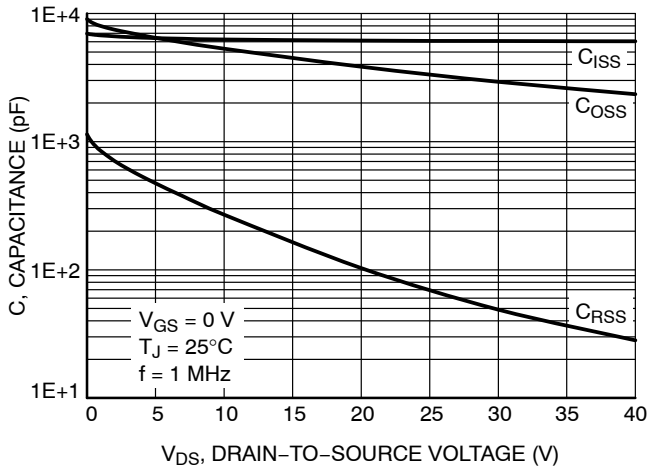


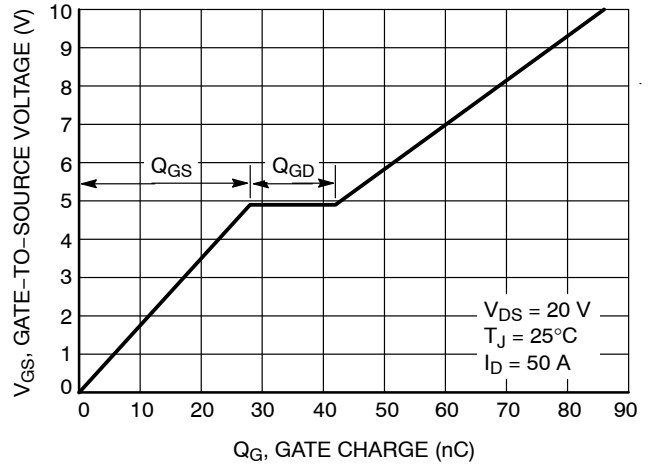
Figure 6. Drain-to-Source Leakage Current vs. Voltage

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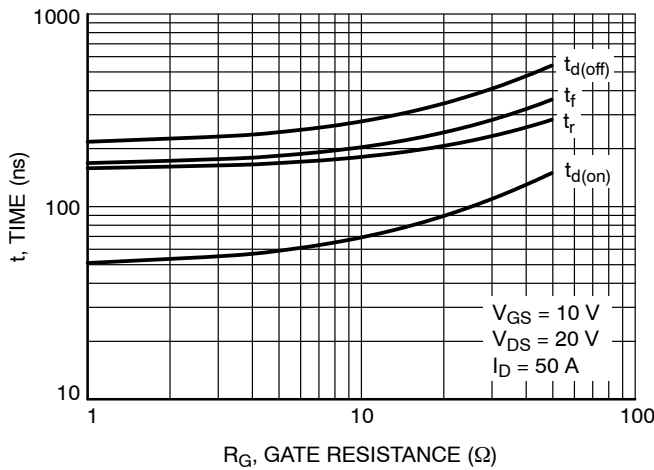
## TYPICAL CHARACTERISTICS



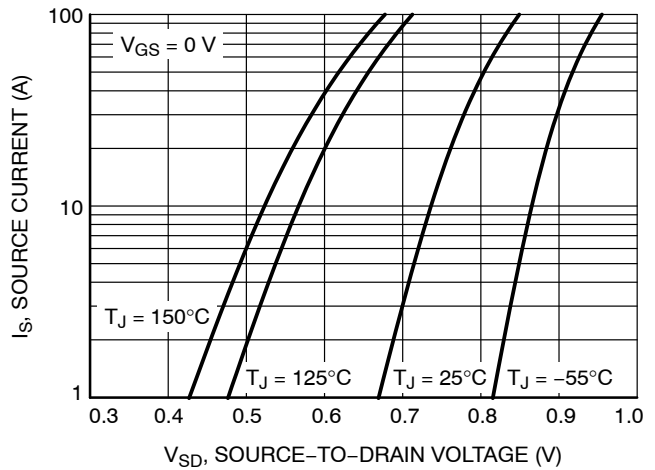
**Figure 7. Capacitance Variation**



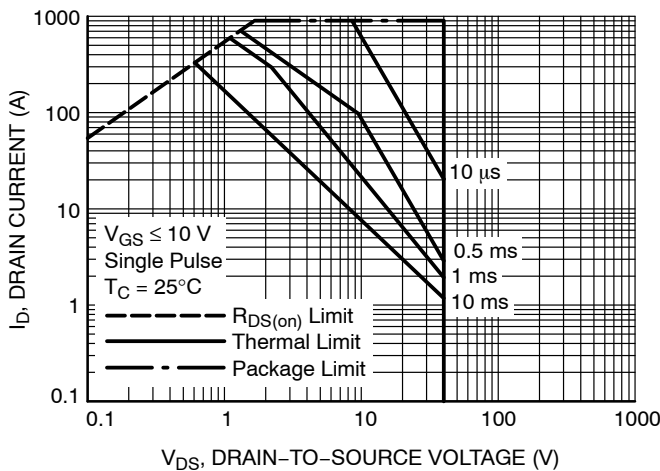
**Figure 8. Gate-to-Source Voltage vs. Charge**



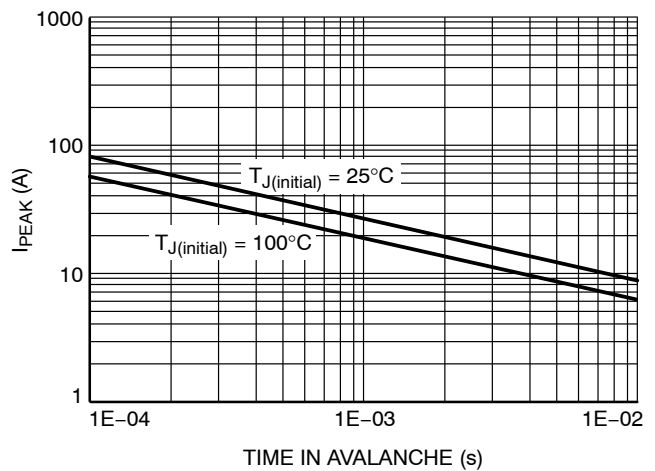
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Diode Forward Voltage vs. Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. IPEAK vs. Time in Avalanche**

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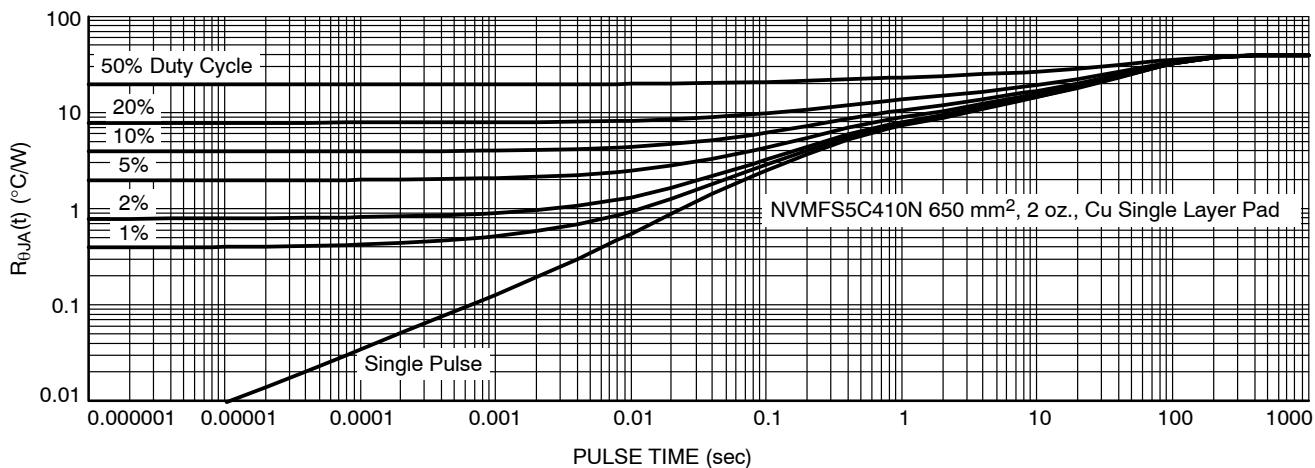


Figure 13. Thermal Characteristics

## DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5C410NT1G	5C410N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C410NWFT1G	410NWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C410NT3G	5C410N	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C410NWFT3G	410NWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C410NAFT1G	5C410N	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C410NWFAFT1G	410NWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



1  
SCALE 2:1

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

### GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN
- STYLE 2:  
PIN 1. ANODE  
2. ANODE  
3. ANODE  
4. NO CONNECT  
5. CATHODE

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5 5x6, 1.27P (SO-8FL)	PAGE 1 OF 1

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