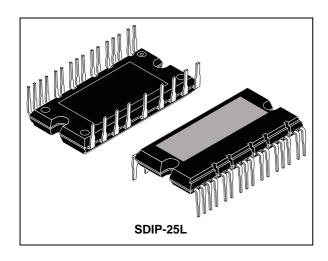
STGIPS20K60



SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter - 18 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Features

- IPM 18 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Short-circuit rugged IGBTs
- V_{CE(sat)} negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against over temperature and overcurrent
- · DBC leading to low thermal resistance
- Isolation rating of 2500 V_{rms}/min
- UL Recognized: UL1557 file E81734

Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machine

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuitrugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPS20K60	GIPS20K60	SDIP-25L	Tube

Contents STGIPS20K60

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1 Internal block diagram and pin configuration

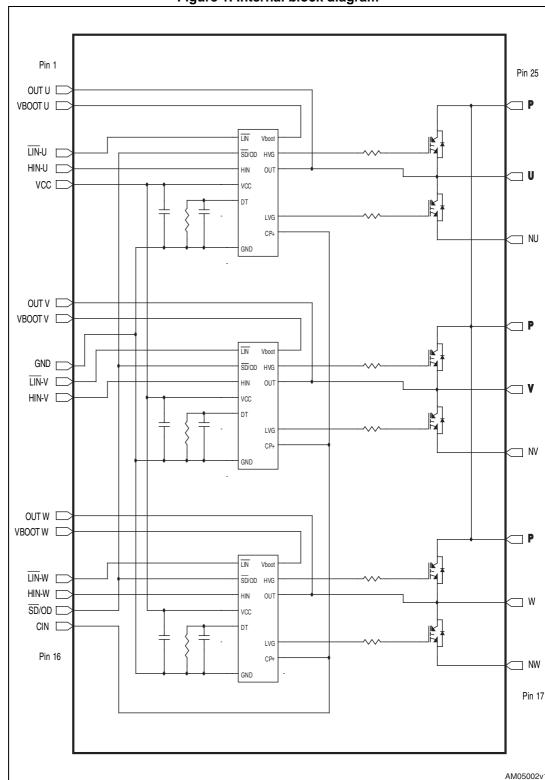
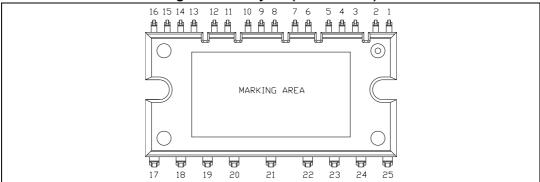


Figure 1. Internal block diagram

Table 2. Pin description

Pin n°	Symbol	Description
1	OUT _U	High-side reference output for U phase
2	V _{bootU}	Bootstrap voltage for U phase
3	LIN _U	Low-side logic input for U phase
4	HIN _U	High-side logic input for U phase
5	V _{CC}	Low voltage power supply
6	OUT _V	High-side reference output for V phase
7	V _{boot V}	Bootstrap voltage for V phase
8	GND	Ground
9	LIN _V	Low-side logic input for V phase
10	HIN_V	High-side logic input for V phase
11	OUT _W	High-side reference output for W phase
12	V _{boot W}	Bootstrap voltage for W phase
13	LIN _W	Low-side logic input for W phase
14	HIN _W	High-side logic input for W phase
15	SD/OD	Shutdown logic input (active low) / open-drain (comparator output)
16	CIN	Comparator input
17	N _W	Negative DC input for W phase
18	W	W phase output
19	Р	Positive DC input
20	N _V	Negative DC input for V phase
21	V	V phase output
22	Р	Positive DC input
23	N _U	Negative DC input for U phase
24	U	U phase output
25	Р	Positive DC input

Figure 2. Pin layout (bottom view)



STGIPS20K60 Electrical ratings

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U , N_V , N_W	450	V
V _{PN(surge)}	Supply voltage (surge) applied between P - N _U , N _V , N _W 500		V
V _{CES}	Each IGBT collector emitter voltage (V _{IN} ⁽¹⁾ = 0)	600	V
± I _C ⁽²⁾	Each IGBT continuous collector current at T _C = 25°C	18	Α
± I _{CP} ⁽³⁾	Each IGBT pulsed collector current	40	Α
P _{TOT}	Each IGBT total dissipation at T _C = 25°C	52	W
t _{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125 ^{\circ}\text{C}, V_{CC} = V_{boot} = 15 \text{V}, V_{IN~(1)} = 0 \div 5 \text{V}$	5	μs

- 1. Applied between HIN_i, $\overline{\text{LIN}}_{i \text{ and }} G_{ND}$ for i = U, V, W
- 2. Calculated according to the iterative formula:

$$I_{C}(T_{C}) = \frac{T_{j(max)} - T_{C}}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_{C}(T_{C}))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V _{OUT}	Output voltage applied between OUT _U , OUT _V , OUT _W - GND	V _{boot} - 21	V _{boot} + 0.3	V
V _{CC}	Low voltage power supply	- 0.3	21	V
V _{CIN}	Comparator input voltage	- 0.3	V _{CC} + 0.3	V
V _{boot}	Bootstrap voltage	- 0.3	620	V
V _{IN}	Logic input voltage applied between HIN, $\overline{\text{LIN}}$ and GND	- 0.3	15	V
V _{SD/OD}	Open drain voltage	- 0.3	15	V
dV _{OUT} /dt	Allowed output slew rate		50	V/ns

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Table 5. Total system

Symbol	Parameter	Value	Unit
V _{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	2500	V
T _j	Power chips operating junction temperature	- 40 to 150	°C
T _C	Module case operation temperature	- 40 to 125	°C

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
D	Thermal resistance junction-case single IGBT	2.4	°C/W
R _{thJC}	Thermal resistance junction-case single diode	5	°C/W

3 Electrical characteristics

 $T_J = 25$ °C unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
Symbol	Farameter	rest conditions	Min.	Тур.	Max.	Onit
V	V _{CE(sat)} Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15 \text{ V}, V_{IN}^{(1)} = 0 \div 5 \text{ V},$ $I_{C} = 12 \text{ A}$	-	2.2	2.75	V
VCE(sat)		$V_{CC} = V_{boot} = 15 \text{ V}, V_{IN}^{(1)} = 0 \div 5 \text{ V},$ $I_{C} = 12 \text{ A}, T_{J} = 125 \text{ °C}$	-	1.8		V
I _{CES}	Collector-cut off current (V _{IN} ⁽¹⁾ = 0 "logic state")	V _{CE} = 550 V, V _{CC} = V _{Boot} = 15 V	-		150	μΑ
V _F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 12 \text{ A}$	-		3.8	V
Inductive	load switching time and	energy				
t _{on}	Turn-on time		-	300	-	
t _{c(on)}	Crossover time (on)	V _{PN} = 300 V,	-	150	-	
t _{off}	Turn-off time	$V_{CC} = V_{boot} = 15 \text{ V},$	-	730	-	ns
t _{c(off)}	Crossover time (off)	$V_{IN}^{(1)} = 0 \div 5 \text{ V},$ $I_C = 12 \text{ A}$ (see <i>Figure 3</i>)	-	170	-	
t _{rr}	Reverse recovery time		-	60	-	
E _{on}	Turn-on switching losses		-	290	-	1
E _{off}	Turn-off switching losses		-	250	-	μJ

^{1.} Applied between HIN_i, $\overline{\text{LIN}}_{i \text{ and }} G_{ND}$ for i = U, V, W. ($\overline{\text{LIN}}$ inputs are active-low).

Note:

 t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Electrical characteristics STGIPS20K60

INPUT BUS BOOT VBOOT>VCC /SD HVG RSD Hin VCC OUT Vcc LVG DT GND CP+ ±_0 AM17166v1

Figure 3. Switching time test circuit



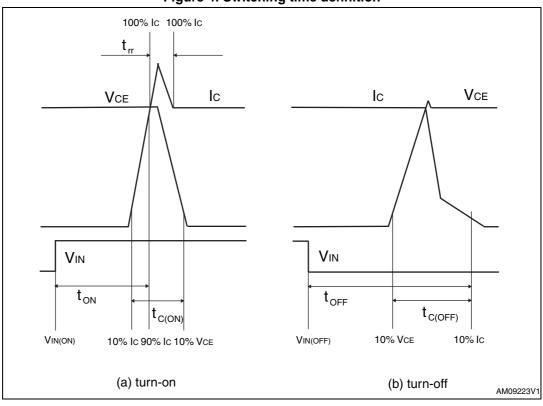


Figure 4 "Switching time definition" refers to HIN inputs (active high). For $\overline{\text{LIN}}$ inputs (active low), V_{IN} polarity must be inverted for turn-on and turn-off.

3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15 \text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{CC_hys}	V _{CC} UV hysteresis		1.2	1.5	1.8	V
V _{CC_thON}	V _{CC} UV turn ON threshold		11.5	12	12.5	V
V _{CC_thOFF}	V _{CC} UV turn OFF threshold		10	10.5	11	V
I _{qccu}	Undervoltage quiescent supply current	$V_{CC} = 10 \text{ V}$ $\overline{SD}/OD = 5 \text{ V}; \overline{LIN} = 5 \text{ V};$ $H_{IN} = 0, C_{IN} = 0$			450	μΑ
I _{qcc}	Quiescent current	$V_{CC} = 15 \text{ V}$ $\overline{SD}/OD = 5 \text{ V}; \overline{LIN} = 5 \text{ V}$ $H_{IN} = 0, C_{IN} = 0$			3.5	mA
V _{ref}	Internal comparator (CIN) reference voltage		0.5	0.54	0.58	V

Table 9. Bootstrapped voltage ($V_{CC} = 15 \text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V_{BS_hys}	V _{BS} UV hysteresis		1.2	1.5	1.8	V
V _{BS_thON}	V _{BS} UV turn ON threshold		11.1	11.5	12.1	V
V _{BS_thOFF}	V _{BS} UV turn OFF threshold		9.8	10	10.6	V
I_{QBSU}	Undervoltage V _{BS} quiescent current	V_{BS} < 9 V \overline{SD} /OD = 5 V; \overline{LIN} and \overline{HIN} = 5 V; $\overline{C_{IN}}$ = 0		70	110	μA
I _{QBS}	V _{BS} quiescent current	$V_{BS} = 15 \text{ V}$ $\overline{SD}/OD = 5 \text{ V}; \overline{LIN} \text{ and}$ $HIN = 5 \text{ V}; C_{IN} = 0$		210	300	μA
R _{DS(on)}	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10. Logic inputs (V_{CC} = 15 V unless otherwise specified)

Symbol Parameter Test conditions Min. Typ. V_{il} Low logic level voltage 0.8 V_{ih} High logic level voltage 1.9 I_{HINh} HIN logic "1" input bias current HIN = 15 V 110 175 I_{HINI} HIN logic "0" input bias current HIN = 0 V 3 6 I_{LINI} \overline{LIN} logic "1" input bias current \overline{LIN} = 15 V 30 120 I_{SDh} \overline{SD} logic "0" input bias current \overline{SD} = 0 V	rame to a give in pane (100 to 1 among a mor mor abounds)							
V _{ih} High logic level voltage 1.9 I _{HINh} HIN logic "1" input bias current HIN = 15 V 110 175 I _{HINI} HIN logic "0" input bias current HIN = 0 V 3 6 I _{LINI} LIN logic "1" input bias current LIN = 15 V 3 6 I _{SDh} SD logic "0" input bias current SD = 15 V 30 120	Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
I_{HINh} HIN logic "1" input bias current HIN = 15 V 110 175 I_{HINI} HIN logic "0" input bias current HIN = 0 V 3 6 I_{LINI} LIN logic "1" input bias current LIN = 15 V 3 6 I_{LINh} LIN logic "0" input bias current LIN = 15 V 30 120	V_{il}	Low logic level voltage		8.0		1.1	V	
I_{HINI} HIN logic "0" input bias current HIN = 0 V I_{LINI} \overline{LIN} logic "1" input bias current \overline{LIN} = 0 V 3 6 I_{LINh} \overline{LIN} logic "0" input bias current \overline{LIN} = 15 V 3 120 I_{SDh} \overline{SD} logic "0" input bias current \overline{SD} = 15 V 30 120	V _{ih}	High logic level voltage		1.9		2.25	V	
I_{LINI} \overline{LIN} logic "1" input bias current \overline{LIN} = 0 V 3 6 I_{LINh} \overline{LIN} logic "0" input bias current \overline{LIN} = 15 V 30 120 I_{SDh} \overline{SD} logic "0" input bias current \overline{SD} = 15 V 30 120	I _{HINh}	HIN logic "1" input bias current	HIN = 15 V	110	175	260	μA	
I _{LINh} LIN logic "0" input bias current LIN = 15 V I _{SDh} SD logic "0" input bias current SD = 15 V 30 120	I _{HINI}	HIN logic "0" input bias current	HIN = 0 V			1	μΑ	
I_{SDh} \overline{SD} logic "0" input bias current $\overline{SD} = 15 \text{ V}$ 30 120	I _{LINI}	LIN logic "1" input bias current	LIN = 0 V	3	6	20	μA	
	I _{LINh}	LIN logic "0" input bias current	<u>LIN</u> = 15 V			1	μA	
I _{SDI} SD logic "1" input bias current SD = 0 V	I _{SDh}	SD logic "0" input bias current	SD = 15 V	30	120	300	μA	
	I _{SDI}	SD logic "1" input bias current	SD = 0 V			3	μA	
Dt Dead time see Figure 7 600	Dt	Dead time	see Figure 7		600		ns	

Electrical characteristics STGIPS20K60

Table 11. Sense comparator characteristics ($V_{CC} = 15 \text{ V}$ unless otherwise specified)

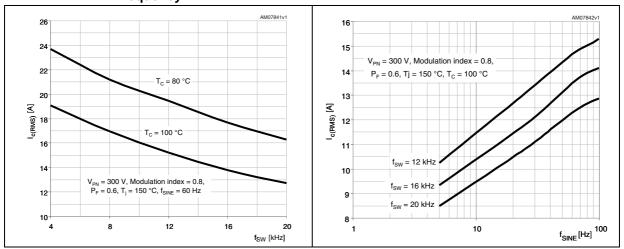
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{ib}	Input bias current	V _{CIN} = 1 V	-		3	μA
V _{ol}	Open-drain low-level output voltage	I _{od} = 3 mA	-		0.5	V
t _{d_comp}	Comparator delay	SD/OD pulled to 5 V through 100 kΩ resistor	-	90	130	ns
SR	Slew rate	$C_L = 180 \text{ pF}; R_{pu} = 5 \text{ k}\Omega$	-	60		V/µsec
t _{sd}	Shut down to high / low side driver propagation delay	$V_{OUT} = 0, V_{boot} = V_{CC},$ $V_{IN} = 0 \text{ to } 3.3 \text{ V}$	50	125	200	
t _{isd}	Comparator triggering to high / low side driver turn-off propagation delay	Measured applying a voltage step from 0 V to 3.3 V to pin CIN	50	200	250	ns

Table 12. Truth table

Condition	Logic input (V _I)			Output		
	SD/OD	LIN	HIN	LVG	HVG	
Shutdown enable half-bridge tri-state	L	Х	Х	L	L	
Interlocking half-bridge tri-state	Н	L	Н	L	L	
0 "logic state" half-bridge tri-state	Н	Н	L	L	L	
1 "logic state" low side direct driving	Н	L	L	Н	L	
1 "logic state" high side direct driving	Н	Н	Н	L	Н	

Note: X: don't care

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{SINE} (1) frequency (1)



1. Simulated curves refer to typical IGBT parameters and maximum $\rm \textit{R}_{thj\text{-}c.}$



Electrical characteristics STGIPS20K60

3.2 **Waveforms definitions**

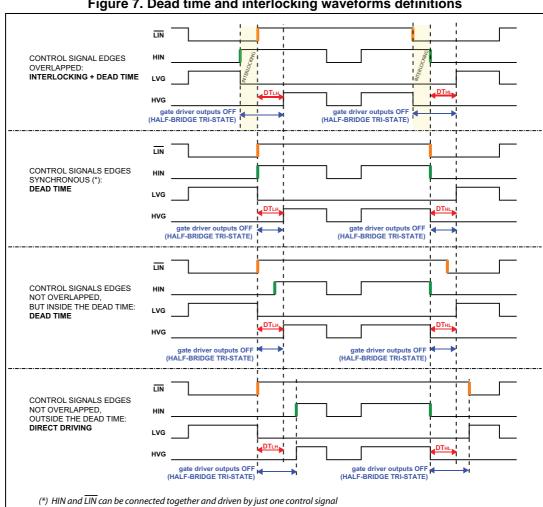


Figure 7. Dead time and interlocking waveforms definitions

4 Smart shutdown function

The STGIPS20K60 integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference Vref connected to the inverting input, while the non-inverting input, available on pin (CIN), can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the halfbridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open-drain output (pin SD/OD) is turned on by the internal logic which holds it on until the shutdown voltage is lower than the logic input lower threshold (Vil). Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.



Smart shutdown function STGIPS20K60

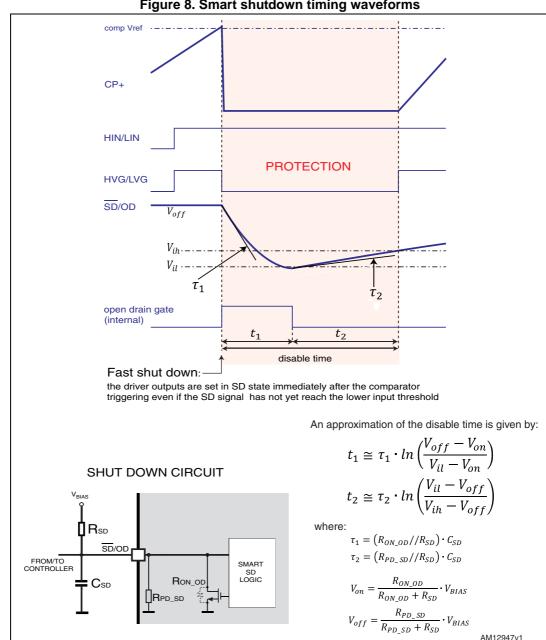
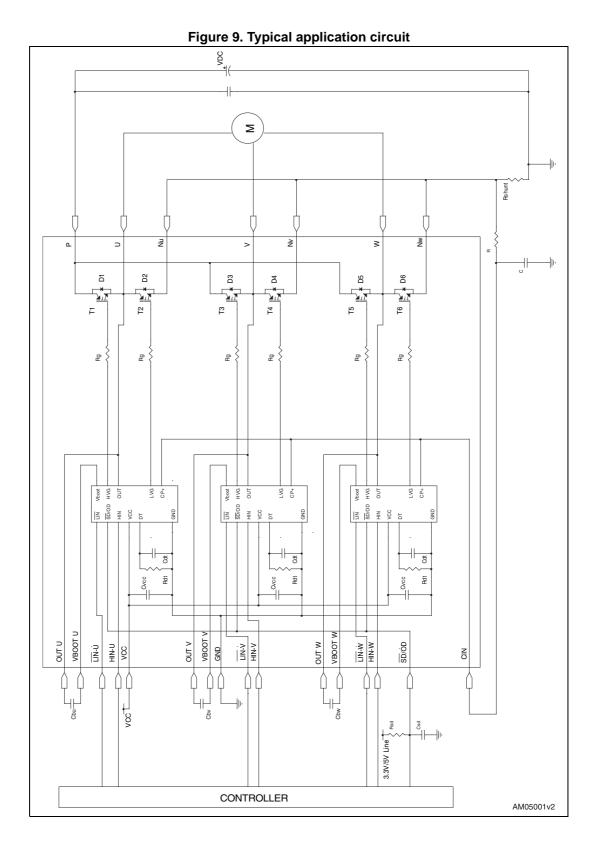


Figure 8. Smart shutdown timing waveforms

Please refer to Table 11 for internal propagation delay time details.

5 Application information



5.1 Recommendations

- Input signal HIN is active high logic. A 85 k Ω (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- Input signal LIN is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5 V regulator through a diode, is built-in for each low side input.
- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The SD/OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see Section 4: Smart shutdown function for detailed info).

Table 13. Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
	Farameter	Conditions	Min.	Тур.	Max.	Onit
V_{PN}	Supply Voltage	Applied between P-Nu,Nv,Nw		300	400	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	13.5	15	18	V
V _{BS}	High side bias voltage	Applied between V_{BOOTi} -OUT _i for $i = U,V,W$	13		18	V
t _{dead}	Blanking time to prevent Arm-short	For each input signal	1			μs
f _{PWM}	PWM input signal	-40°C < T _c < 100°C -40°C < T _j < 125°C			20	kHz
T _C	Case operation temperature				100	°C

For further details refer to AN3338.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 14. SDIP-25L mechanical data

Dim.	(mm.)					
Dim.	Min.	Тур.	Max.			
А	43.90	44.40	44.90			
A1	1.15	1.35	1.55			
A2	1.40	1.60	1.80			
A3	38.90	39.40	39.90			
В	21.50	22.00	22.50			
B1	11.25	11.85	12.45			
B2	24.83	25.23	25.63			
С	5.00	5.40	6.00			
C1	6.50	7.00	7.50			
C2	11.20	11.70	12.20			
е	2.15	2.35	2.55			
e1	3.40	3.60	3.80			
e2	4.50	4.70	4.90			
e3	6.30	6.50	6.70			
D		33.30				
D1		5.55				
E		11.20				
E1		1.40				
F	0.85	1.00	1.15			
F1	0.35	0.50	0.65			
R	1.55	1.75	1.95			
Т	0.45	0.55	0.65			
V	0°		6°			

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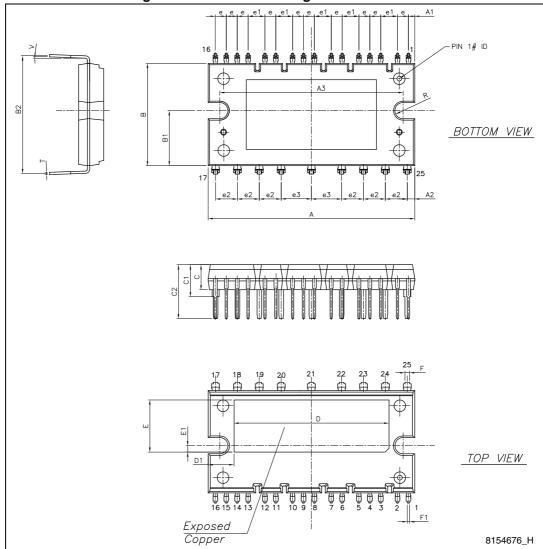


Figure 10. SDIP-25L drawing dimensions data

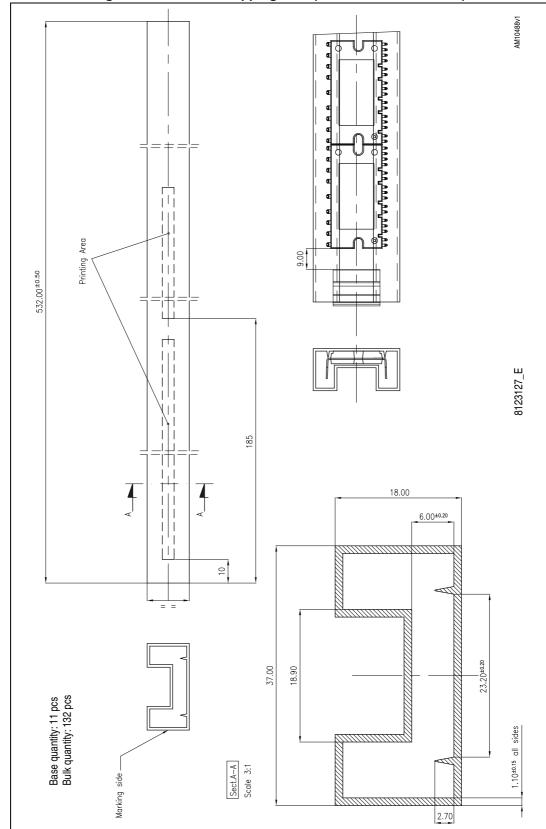


Figure 11. SDIP-25L shipping tube (dimensions are in mm.)

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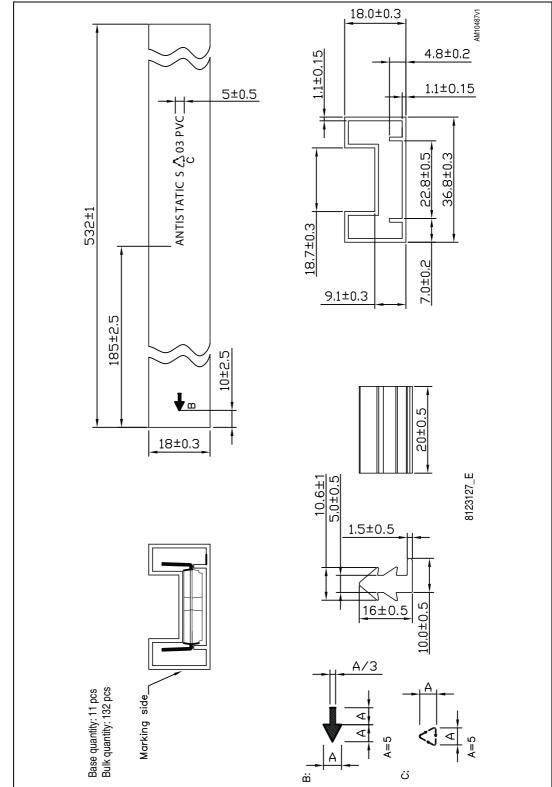


Figure 12. SDIP-25L shipping tube type B (dimensions are in mm.)

STGIPS20K60 Revision history

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
10-Aug-2009	1	Initial release
01-Jul-2010	2	Document status promoted from preliminary to datasheet. Updated package mechanical data (Section 6: Package mechanical data). Minor text changes to improve readability.
23-Sep-2010	3	Updated: <i>Table 3</i> , 5, 10 and <i>Table 11</i> . Modified: <i>Figure 5</i> and <i>Figure 6</i> .
03-May-2011	4	Updated title with SLLIMM™ in cover page, added SDIP-25L tube dimensions <i>Figure 10 on page 18</i> .
04-Nov-2011	5	Updated title with SLLIMM™ (small low-loss intelligent molded module) IPM, 3-phase inverter - 18 A, 600 V short-circuit rugged IGBT in cover page and SDIP-25L mechanical data <i>Table 14 on page 17, Figure 10 on page 18.</i>
28-Aug-2012	6	Modified: Min. and Max. value <i>Table 4 on page 5</i> . Updated: <i>Figure 11 on page 19</i> . Added: <i>Figure 12 on page 20</i> .
02-May-2013	7	Modified: Figure 3 on page 8 and Figure 8 on page 14.

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