

SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

- Operating Range 2-V to 5.5-V V_{CC}
- EPIC™ (Enhanced-Performance Implanted CMOS) Process
- High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

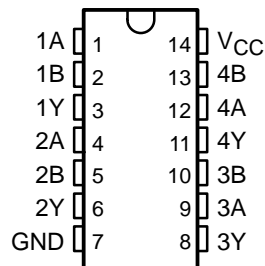
description

The 'AHC86 are quadruple 2-input exclusive-OR gates. These devices perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

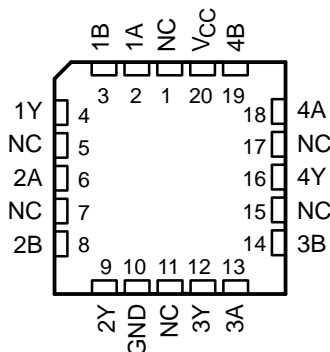
A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

The SN54AHC86 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC86 is characterized for operation from -40°C to 85°C .

SN54AHC86 . . . J OR W PACKAGE
SN74AHC86 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



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 **TEXAS
INSTRUMENTS**

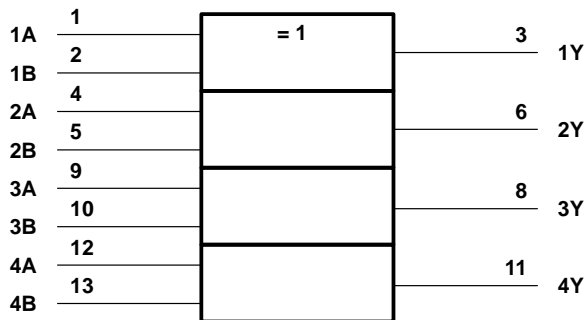
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SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

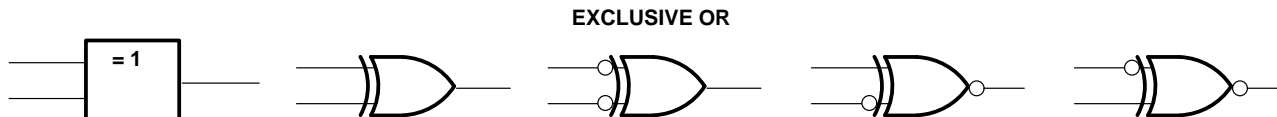
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, PW, and W packages.

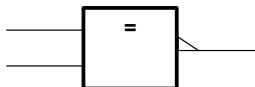
exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an SN74AHC86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



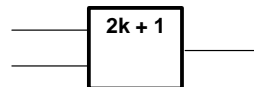
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

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SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): D package	1.25 W
DB or PW package	0.5 W
N package	1.1 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

		SN54AHC86		SN74AHC86		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5		V
		$V_{CC} = 3$ V		2.1		
		$V_{CC} = 5.5$ V		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		V
		$V_{CC} = 3$ V		0.9		
		$V_{CC} = 5.5$ V		1.65		
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		μA
		$V_{CC} = 3.3$ V ± 0.3 V		–4		mA
		$V_{CC} = 5$ V ± 0.5 V		–8		
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		μA
		$V_{CC} = 3.3$ V ± 0.3 V		4		mA
		$V_{CC} = 5$ V ± 0.5 V		8		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.



SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC86		SN74AHC86		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	A or B inputs	V _I = V _{CC} or GND	5.5 V			± 0.1		± 1	± 1	μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	20	μA
C _i		V _I = V _{CC} or GND	5 V		4	10			10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC86				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH} *	A or B	Y	C _L = 15 pF	7	11	1	13	ns	
t _{PHL} *				7	11	1	13		
t _{PLH}	A or B	Y	C _L = 50 pF	9.5	14.5	1	16.5	ns	
t _{PHL}				9.5	14.5	1	16.5		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC86				UNIT	
				T _A = 25°C			MIN		MAX
				MIN	TYP	MAX			
t _{PLH}	A or B	Y	C _L = 15 pF	7	11	1	13	ns	
t _{PHL}				7	11	1	13		
t _{PLH}	A or B	Y	C _L = 50 pF	9.5	14.5	1	16.5	ns	
t _{PHL}				9.5	14.5	1	16.5		



SN54AHC86, SN74AHC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN54AHC86				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{PLH}^*	A or B	Y	$C_L = 15\text{ pF}$	4.8	6.8	1	8	ns	
t_{PHL}^*				4.8	6.8	1	8		
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	6.3	8.8	1	10	ns	
t_{PHL}				6.3	8.8	1	10		

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

**switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	SN74AHC86				UNIT	
				$T_A = 25^\circ\text{C}$			MIN		MAX
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	$C_L = 15\text{ pF}$	4.8	6.8	1	8	ns	
t_{PHL}				4.8	6.8	1	8		
t_{PLH}	A or B	Y	$C_L = 50\text{ pF}$	6.3	8.8	1	10	ns	
t_{PHL}				6.3	8.8	1	10		

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC86			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.3	0.8		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.3	-0.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5		V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

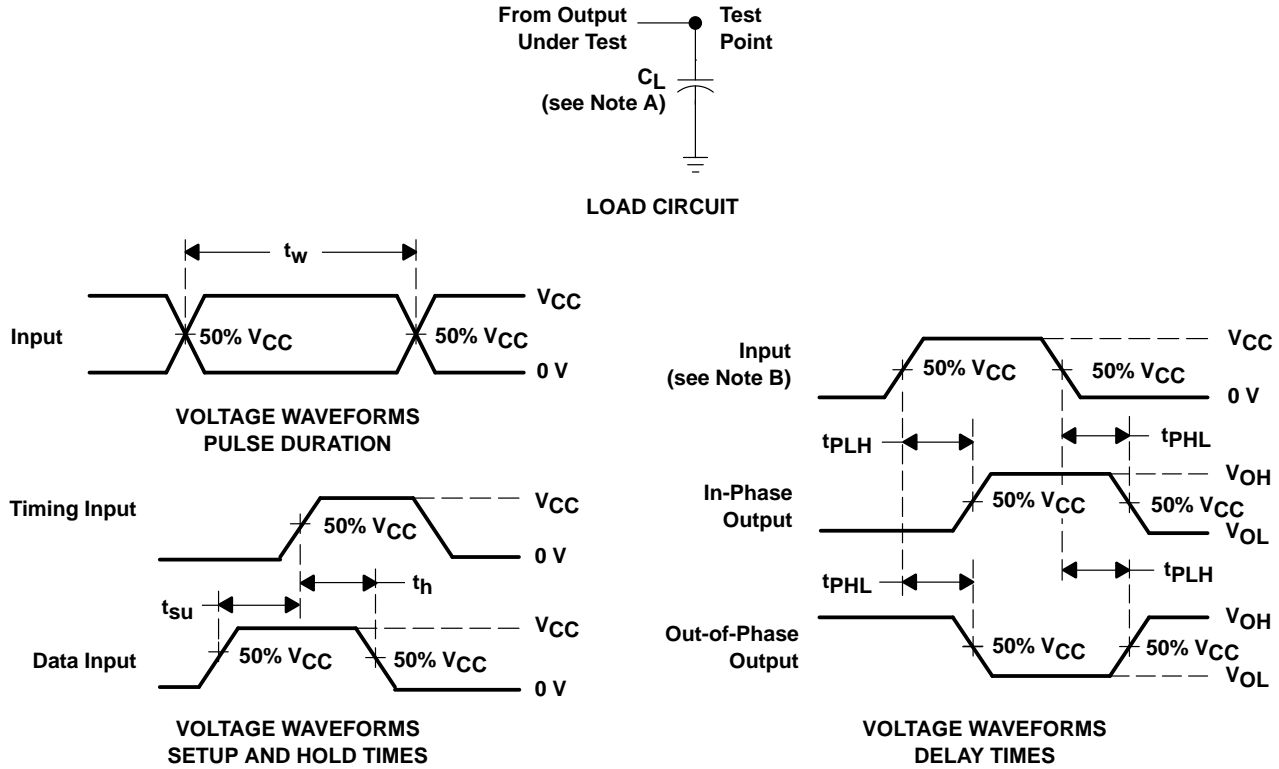
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF

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SCLS249A – OCTOBER 1995 – REVISED MARCH 1996

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 3\text{ ns}$, $t_f = 3\text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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