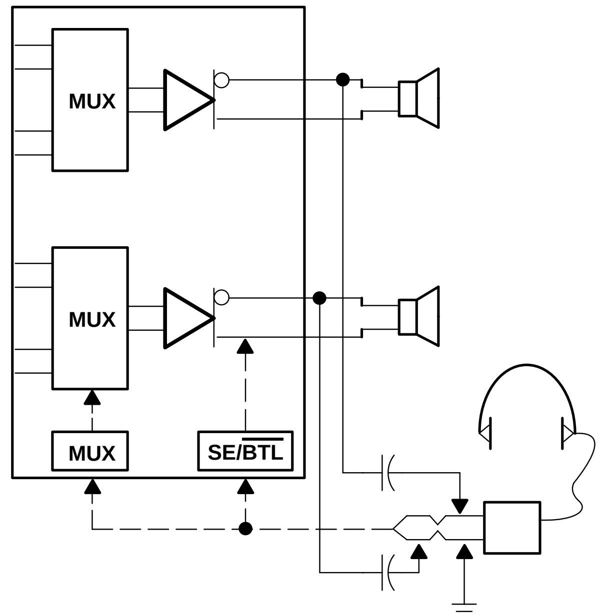
- **High Power with PC Power Supply**
  - **– 1.5 W/Ch at 5 V**
  - **– 600 mW/Ch at 3 V**
- **Ultra-Low Distortion**
  < 0.05% THD+N at 1.5 W and 4-Ω Load
- **Bridge-Tied Load (BTL) or Single Ended (SE) Modes**
- **Stereo Input MUX**
- **Surface Mount Power Package**
  24-Pin TSSOP PowerPAD™
- **Shutdown Control . . . I_{DD} < 10 μA**



description

The TPA0102 is a stereo audio power amplifier in a 24-pin TSSOP thermal package capable of delivering greater than 1.5 W of continuous RMS power per channel into 4-Ω loads. This device functionality provides a very efficient upgrade path from the TPA4860 and TPA4861 mono amplifiers where three separate devices are required for stereo applications: two for speaker drive, plus a third for headphone drive. The TPA0102 simplifies design and frees up board space for other features. Full power distortion levels of less than 0.1% THD+N from a 5-V supply are typical. This provides significant improvement in fidelity for speech and music over the popular TPA4860/61 series. Low-voltage applications are also well served by the TPA0102 providing 600-mW per channel into 4-Ω loads with a 3.3-V supply voltage.

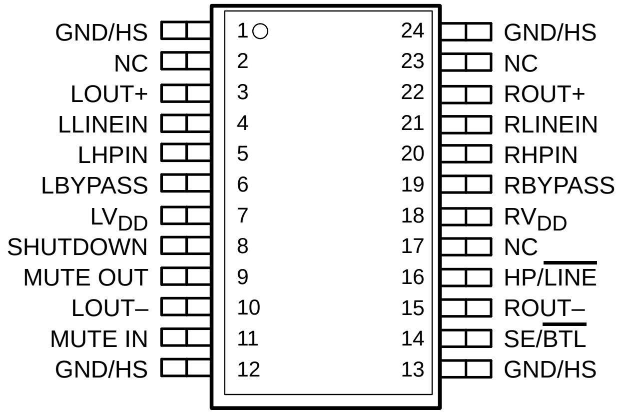
Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 2 to 20 in BTL mode (1 to 10 in SE mode). An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line (often headphone drive) outputs are required to be SE, the TPA0102 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated. Using the TPA0102 to drive line outputs up to 500 mW/channel into external 4 Ω loads is ideal for small non-powered external speakers in portable multimedia systems. The TPA0102 also features a shutdown function for power sensitive applications, holding the supply current below 5 μA. In speakerphone or other monaural applications, the TPA0102 is configured through the power supply terminals to activate only half of the amplifier which reduces supply current by approximately one-half over stereo applications.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0102 to operate at full power into 4-Ω loads at ambient temperature of up to 55°C. Into 8-Ω loads, the operating ambient temperature increases to 100°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP (PWP)
–20°C to 85°C	TPA0102PWP

**PWP PACKAGE
(TOP VIEW)**



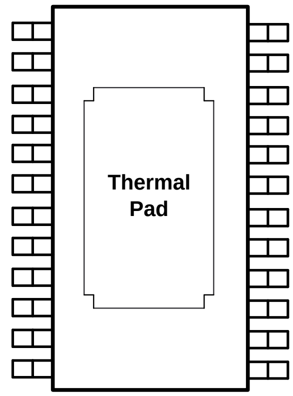


Figure 1. Bottom View of PWP Package, Showing the Thermal Pad

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND/HS	1, 12, 13, 24		Ground connection for circuitry, directly connected to thermal pad.
HP/$\overline{\text{LINE}}$	16	I	Input MUX control input, hold high to select L/RHPIN (5, 20), hold low to select L/RLINEIN (4, 21).
LBYPASS	6		Tap to voltage divider for left channel internal mid-supply bias.
LHP IN	5	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high.
LLINE IN	4	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low.
LOUT+	3	O	Left channel + output in BTL mode, + output in SE mode.
LOUT–	10	O	Left channel – output in BTL mode, high-impedance state in SE mode.
LV_{DD}	7	I	Supply voltage input for left channel and for primary bias circuits.
MUTE IN	11	I	Mute all amplifiers, hold low for normal operation, hold high to mute.
MUTE OUT	9	O	Follows MUTE IN terminal (11), provides buffered output.
NC	2, 17, 23		No internal connection.
RBYPASS	19		Tap to voltage divider for right channel internal mid–supply bias.
RHP IN	20	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held high.
RLINE IN	21	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ terminal (16) is held low.
ROUT+	22	O	Right channel + output in BTL mode, + output in SE mode.
ROUT–	15	O	Right channel – output in BTL mode, high impedance state in SE mode.
RV_{DD}	18	I	Supply voltage input for right channel.
SE/$\overline{\text{BTL}}$	14	I	Hold low for BTL mode, hold high for SE mode.
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, I_{DD} < I μA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 6 V
Continuous total power dissipation . . . . internally limited

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	0	2.7 W	21.8 mW/°C	1.7 W	1.4 W
	300	4.0 W	32.1 mW/°C	2.6 W	2.1 W
PWP‡	0	2.8 W	22.1 mW/°C	1.8 W	1.4 W
	300	6.7 W	53.7 mW/°C	4.3 W	3.5 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.
‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}			3	5	5.5	V
Operating free-air temperature, T_A	V_{DD} = 5 V, 250 mW/ch average power,	4-Ω stereo BTL drive, With proper PCB design	–20		85	°C
	V_{DD} = 5 V, 1.5 W/ch average power,	4-Ω stereo BTL drive, With proper PCB design	–20		55	
Common mode input voltage, V_{ICM}	V_{DD} = 5 V		1.25		4.5	V
	V_{DD} = 3.3 V		1.25		2.7	

dc electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TYP†	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 5 V	Stereo BTL	19	25	mA
			Stereo SE	9	15	mA
			Mono BTL	9	15	mA
			Mono SE	3	10	mA
		V_{DD} = 3.3 V	Stereo BTL	13	20	mA
			Stereo SE	3	10	mA
			Mono BTL	3	10	mA
			Mono SE	3	10	mA
$V_{O(diff)}$	DC differential output voltage	V_{DD} = 5 V	Gain = 2, See Note 1	5	25	mV
$I_{DD(MUTE)}$	Supply current in mute mode	V_{DD} = 5 V		800		µA
I_{SD}	I_{DD} in shutdown	V_{DD} = 5 V		5	15	µA

NOTE 1: At 3 V < V_{DD} < 5 V the dc output voltage is approximately $V_{DD}/2$.

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$P_{(OUT)}$	Output power (each channel) see Note 2	THD = 0.2%,	BTL		1.25		W
		THD = 1%,	BTL		1.5		W
		THD = 0.2%,	SE		500		mW
		THD = 1%,	SE		600		mW
THD+N	Total harmonic distortion plus noise	P_O = 1 W,	f = 20 to 20 kHz		200		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL			72°		
		Open Load			71°		
		SE			52°		
PSRR	Power supply ripple rejection	f = 1 kHz			75		dB
		f = 20 – 20 kHz,			60		dB
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage				25		µV(rms)

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$P_{(OUT)}$	Output power (each channel) see Note 2	THD = 0.2%	BTL		600		mW
		THD = 1%	BTL		750		mW
		THD = 0.2%,	SE		200		mW
		THD = 1%,	SE		250		mW
THD+N	Total harmonic distortion plus noise	P_O = 600 mW,	f = 20 to 20 kHz		250		m%
B_{OM}	Maximum output power bandwidth	G = 10,	THD < 5 %		>20		kHz
	Phase margin	BTL			92°		
		Open Load			70°		
		SE			57°		
PSRR	Power supply ripple rejection	f = 1 kHz			70		dB
		f = 20 – 20 kHz			55		dB
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			65		dB
	Line/HP input separation				100		dB
	BTL attenuation in SE mode				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	P_O = 500 mW,	BTL		95		dB
V_n	Output noise voltage				25		µV(rms)

NOTE 2 Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

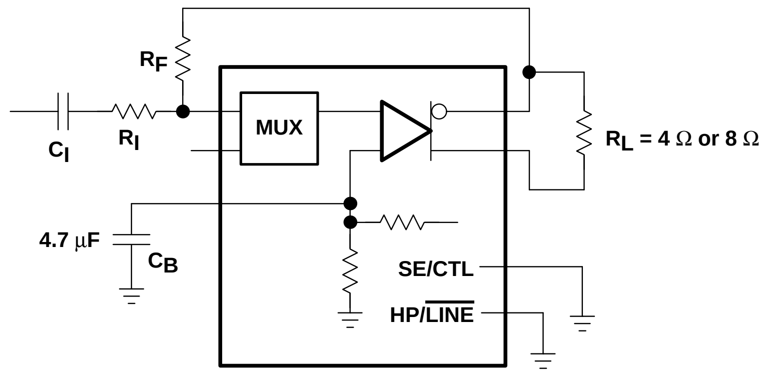


Figure 2. BTL Test Circuit

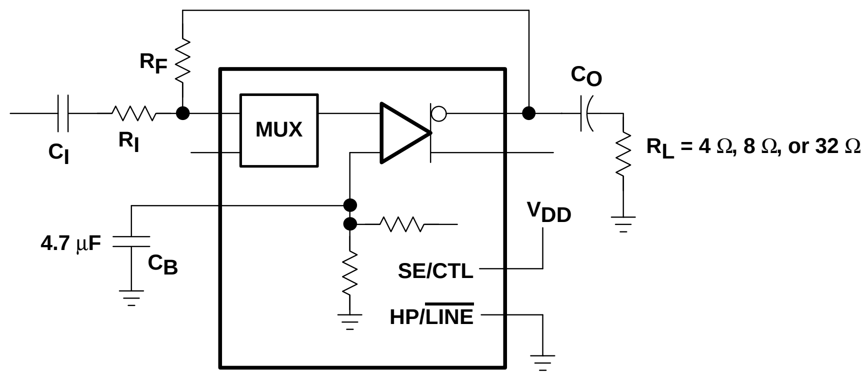


Figure 3. SE Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Frequency	5,6,8,9,12,13,15,16,18,19,21,22, 24,25,27,28,30,31,33,34
		vs Power output	4,7,10,11,14,17,20,23,26,29,32,35
V_n	Noise voltage	vs Frequency	36,37
PSRR	Power supply rejection ratio	vs Frequency	38,39
	Crosstalk	vs Frequency	40 – 43
	Open loop response	vs Frequency	44,45
	Closed loop response	vs Frequency	46 – 49
I_{DD}	Supply current	vs Supply voltage	50
P_O	Output power	vs Supply voltage vs Load resistance	51,52 53,54
P_D	Power dissipation	vs Output power	55 – 58

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

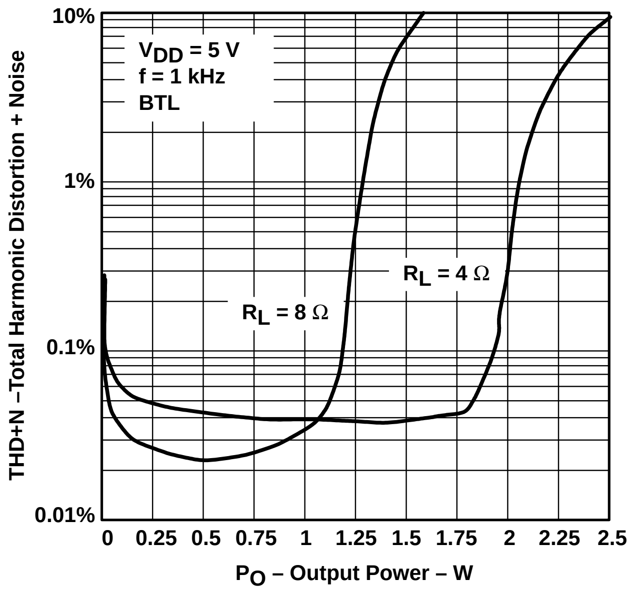


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

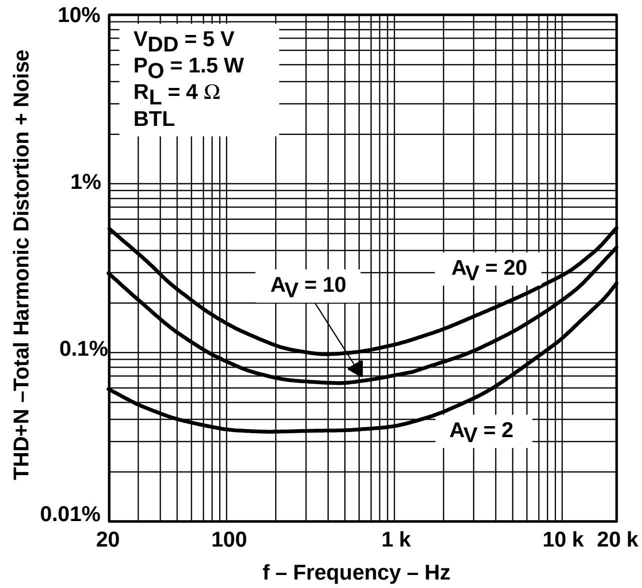


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

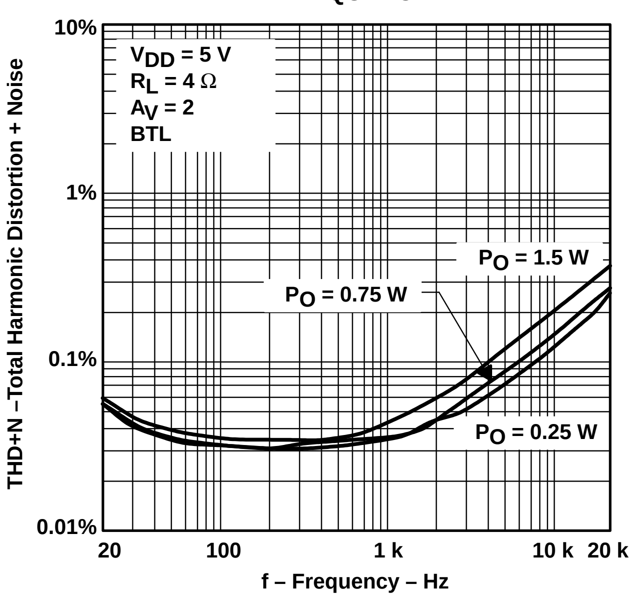


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

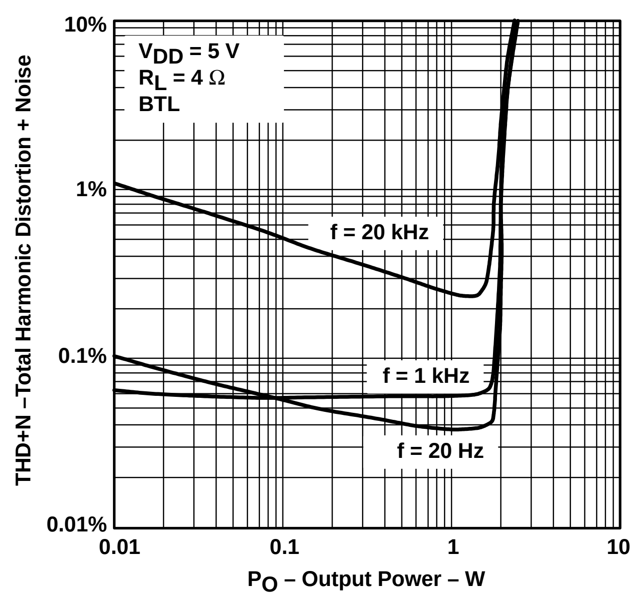


Figure 7

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

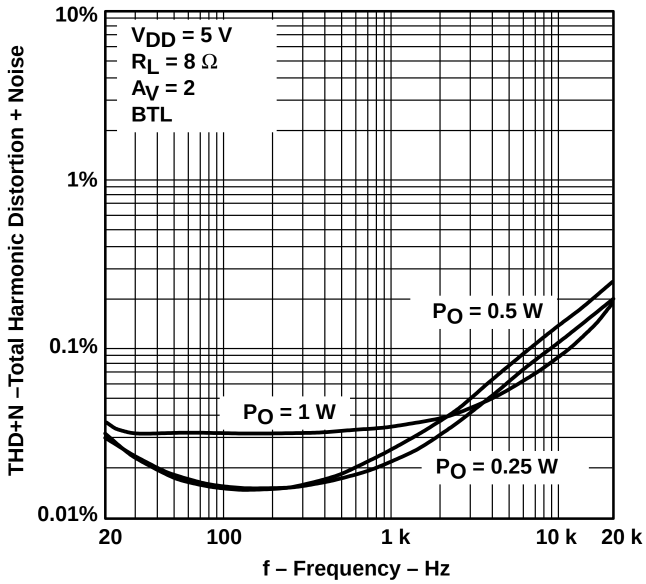


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

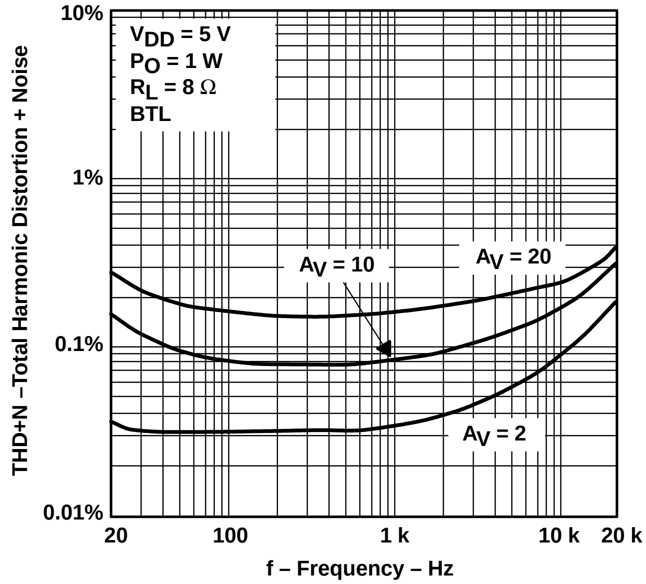


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

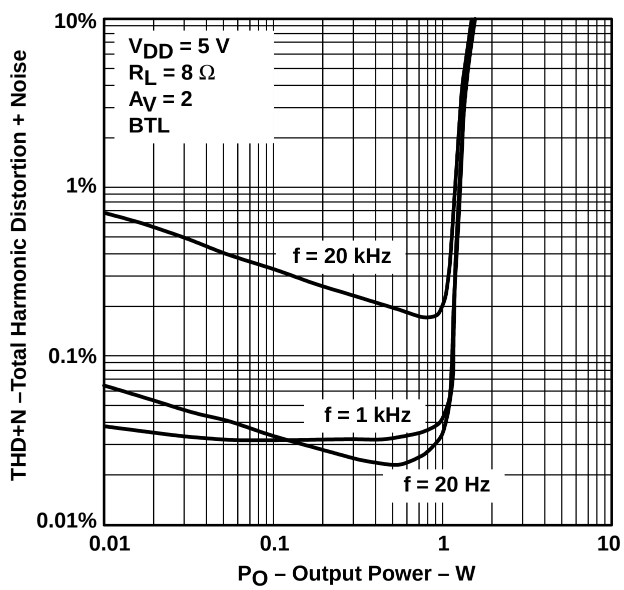


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

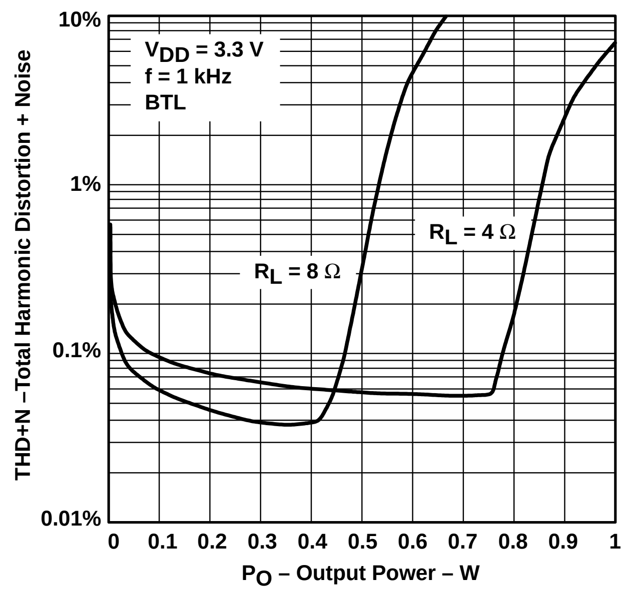


Figure 11

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

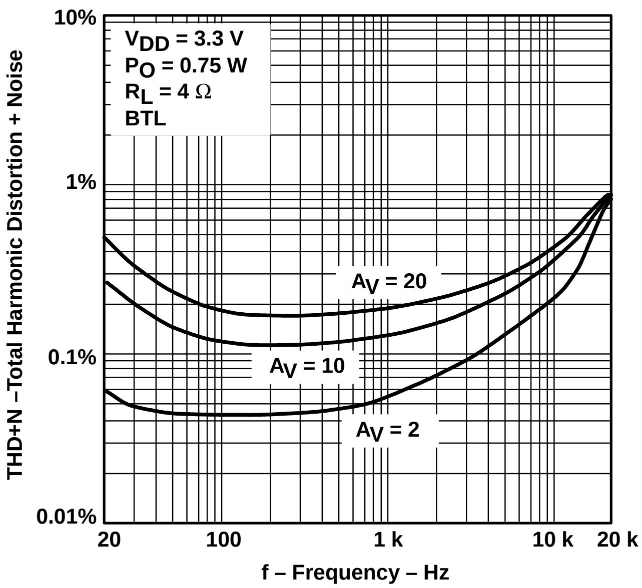


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

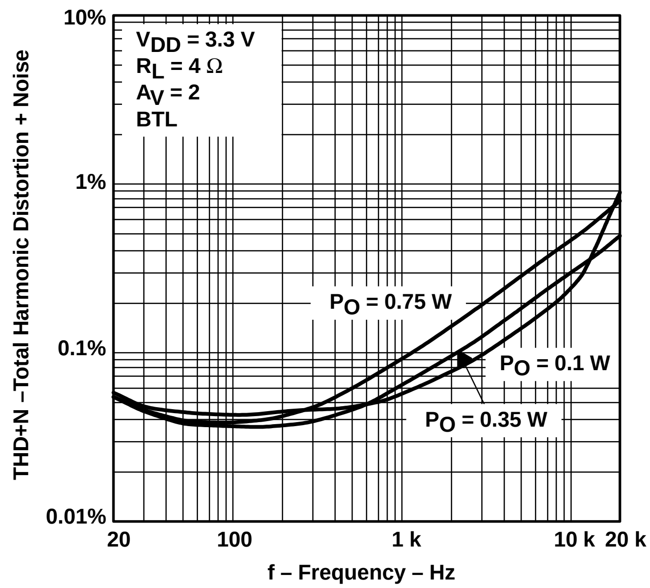


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

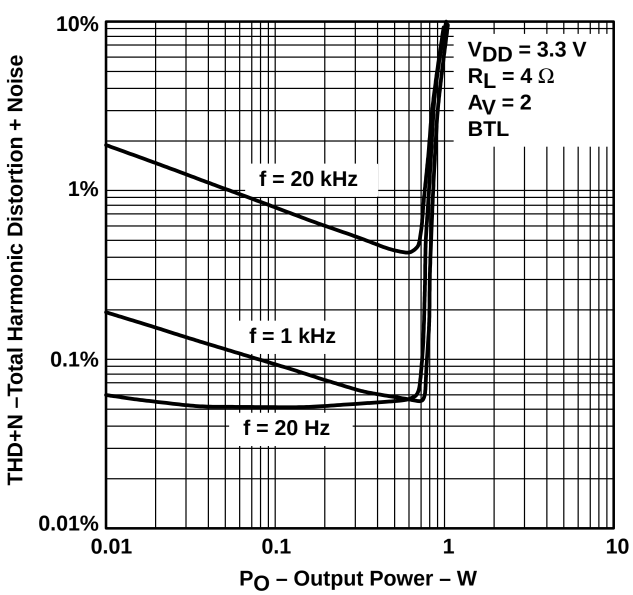


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

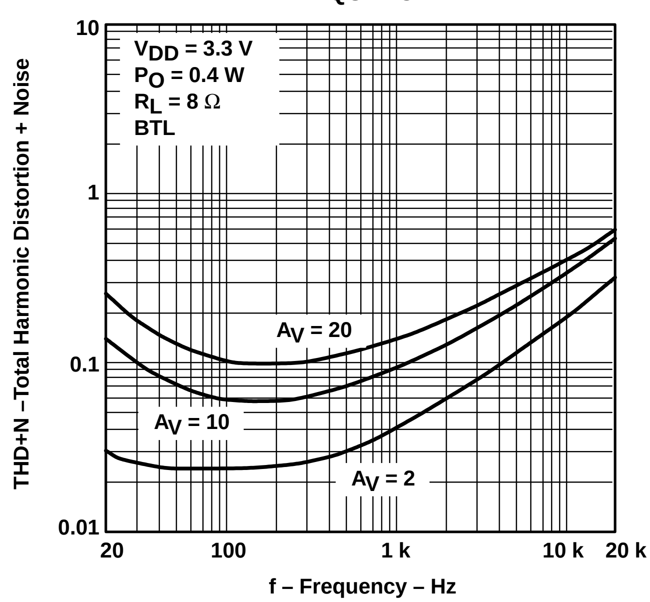


Figure 15

TYPICAL CHARACTERISTICS

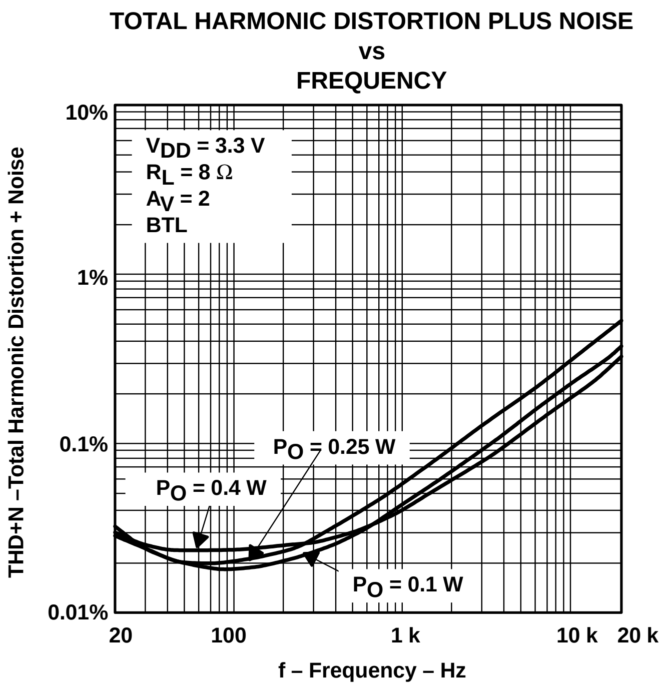


Figure 16

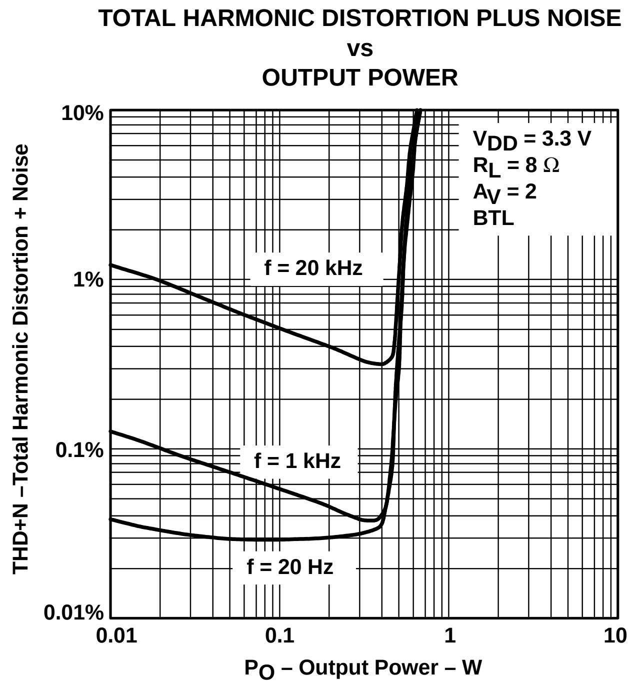


Figure 17

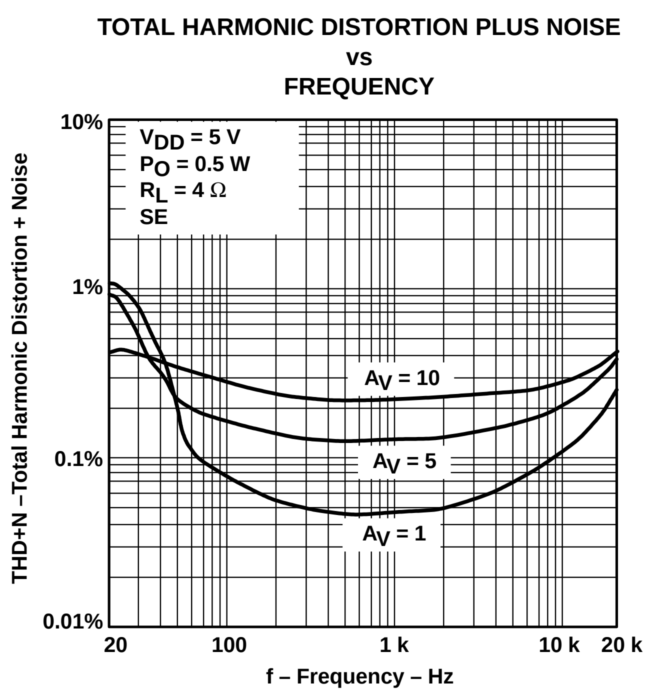


Figure 18

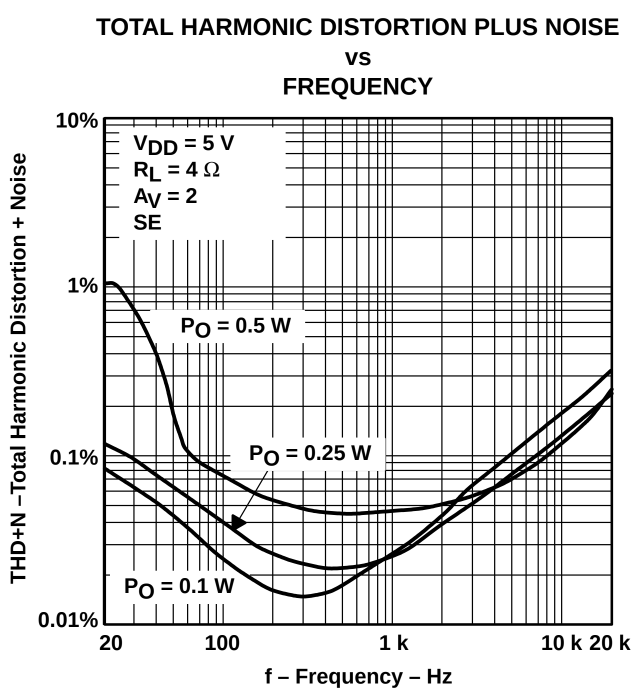


Figure 19

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

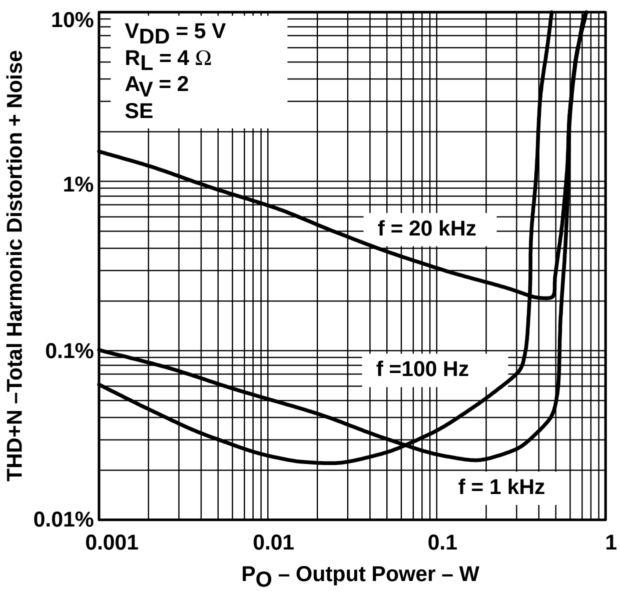


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

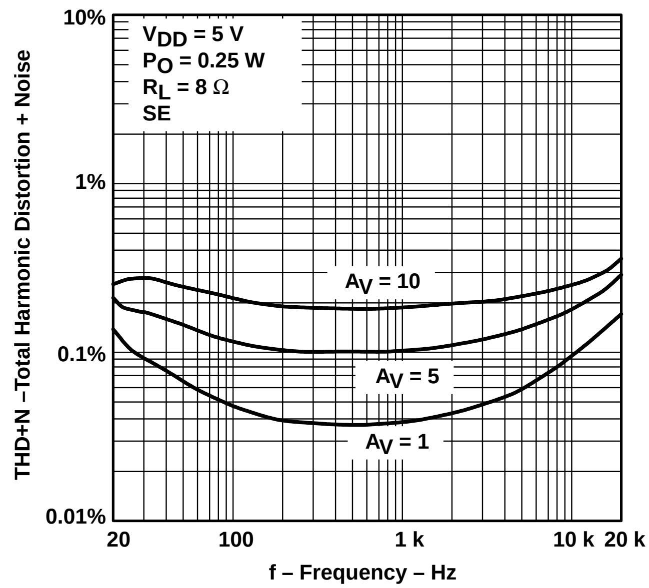


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

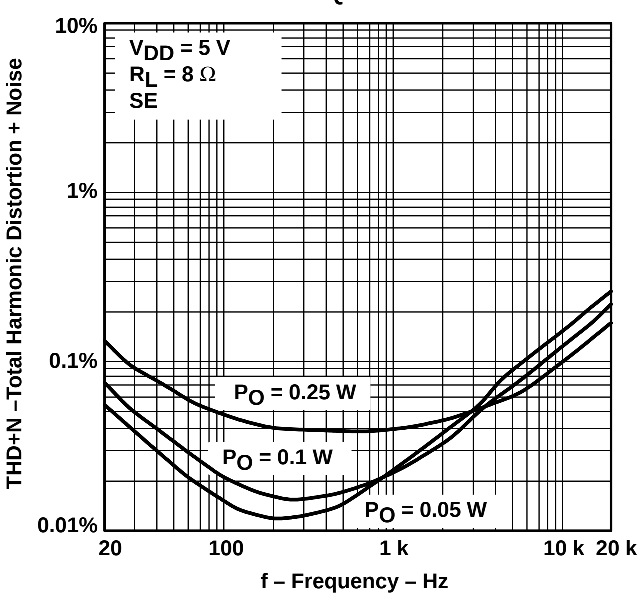


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

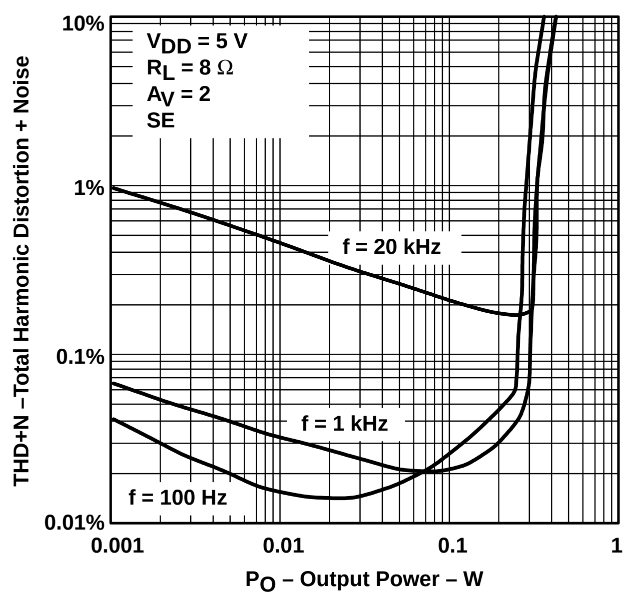


Figure 23

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

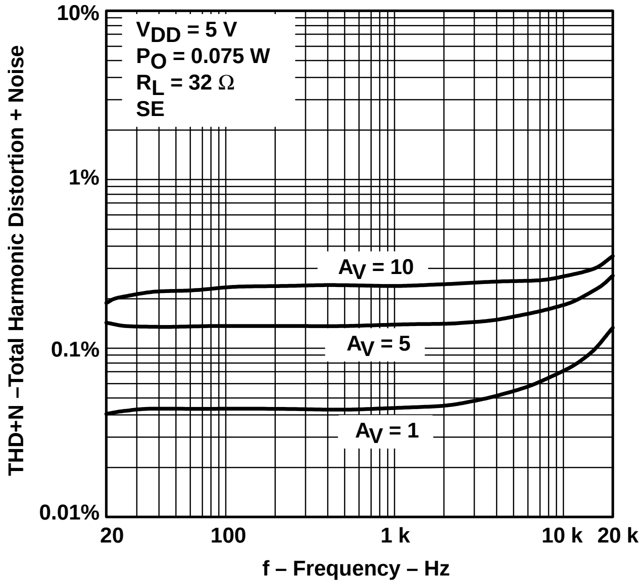


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

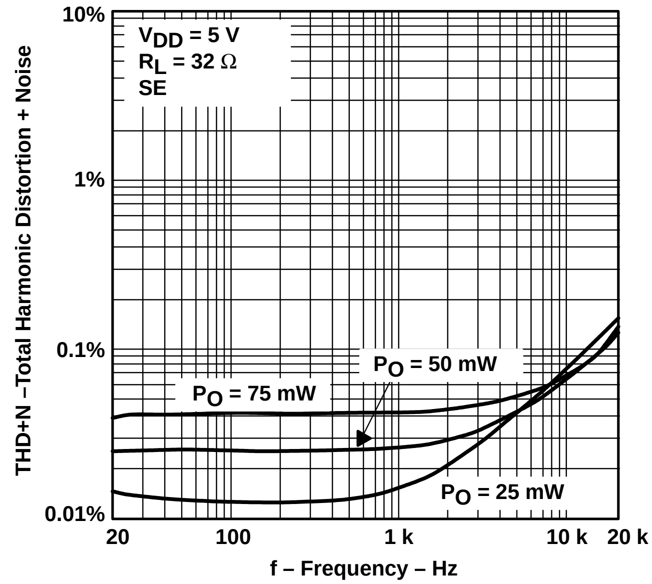


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

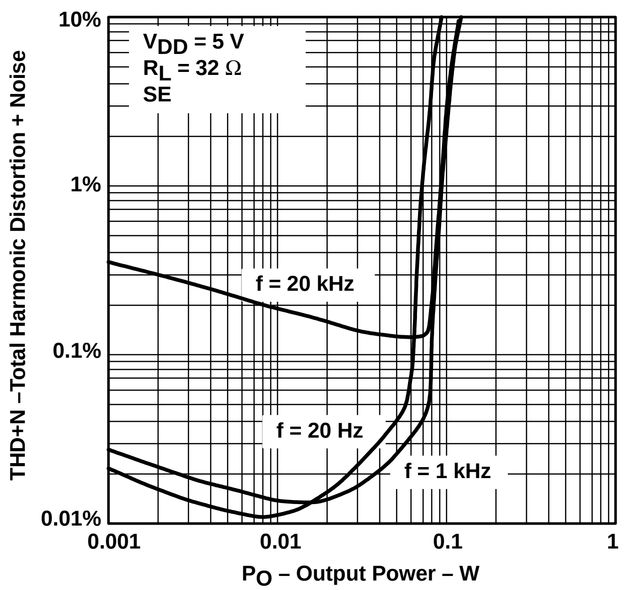


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

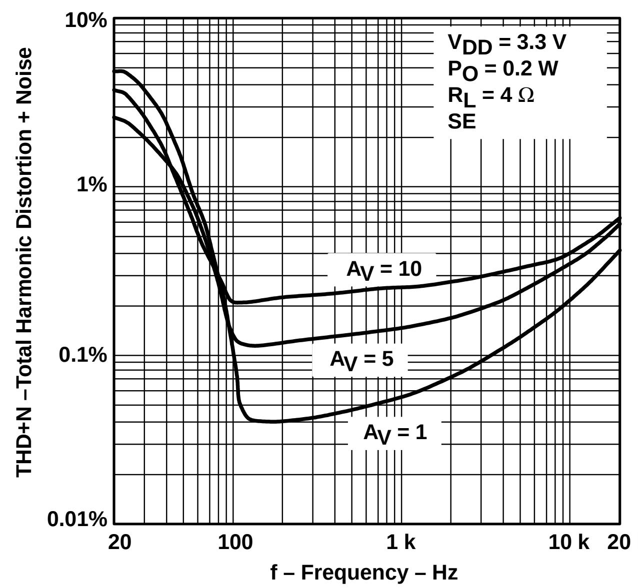


Figure 27

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

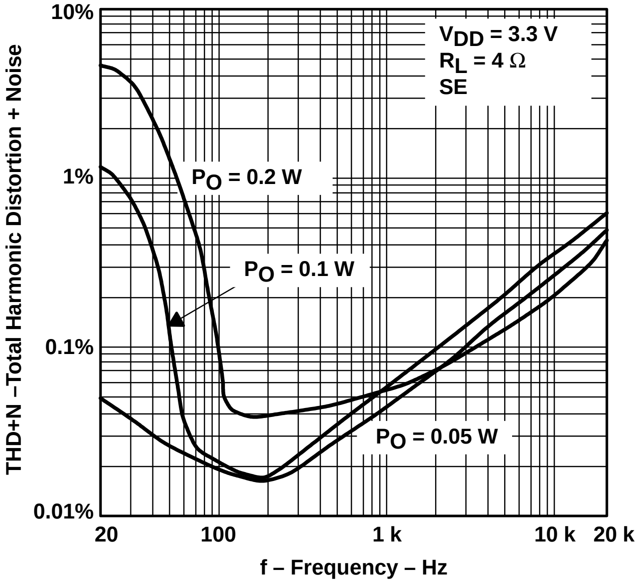


Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

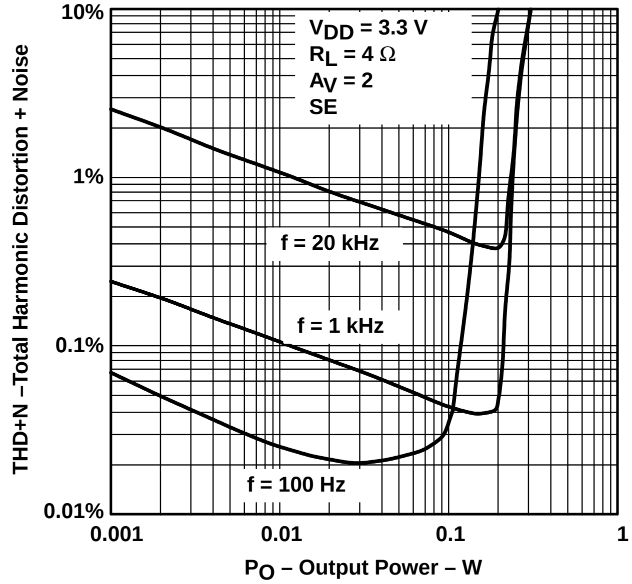


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

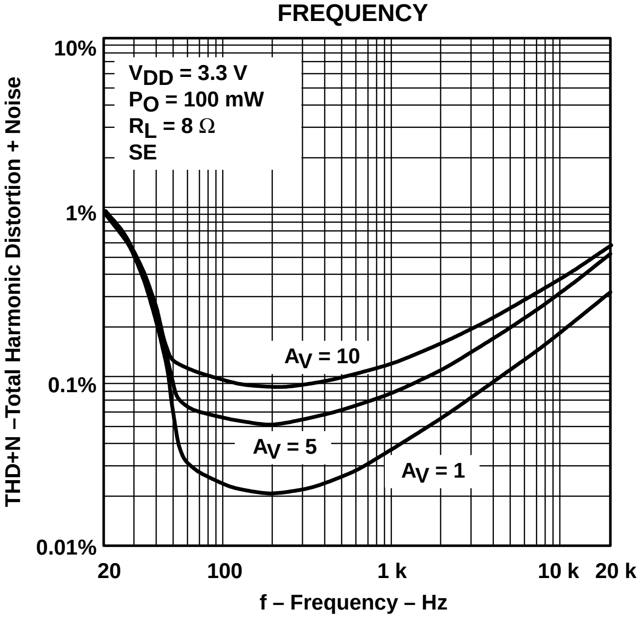


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

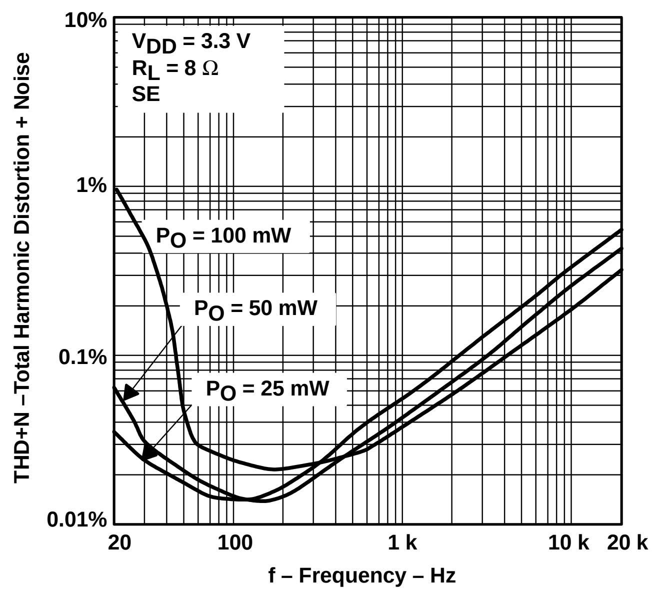


Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

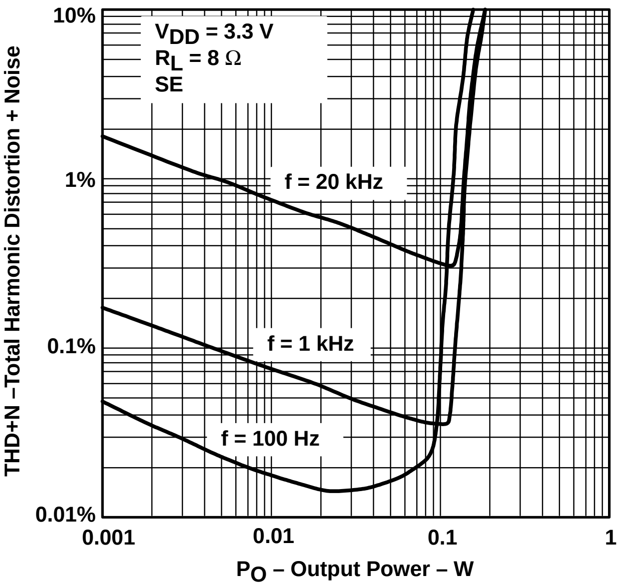


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

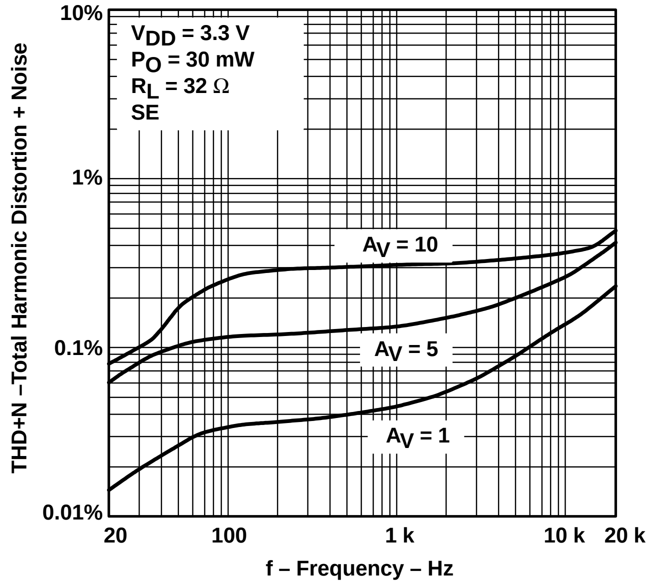


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

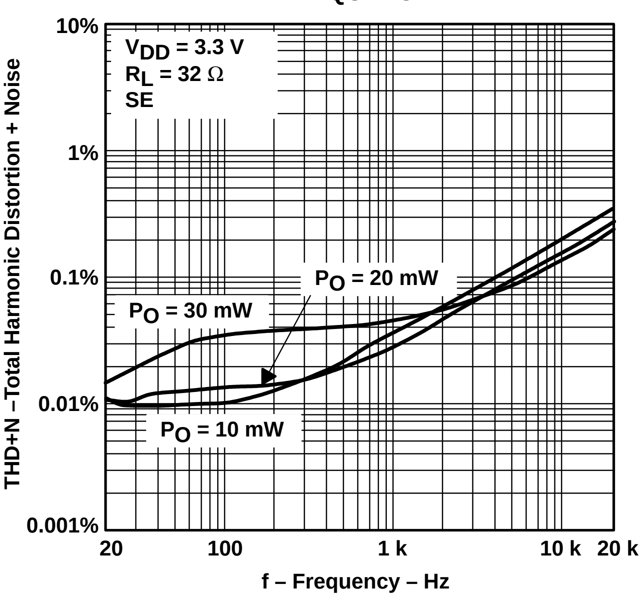


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

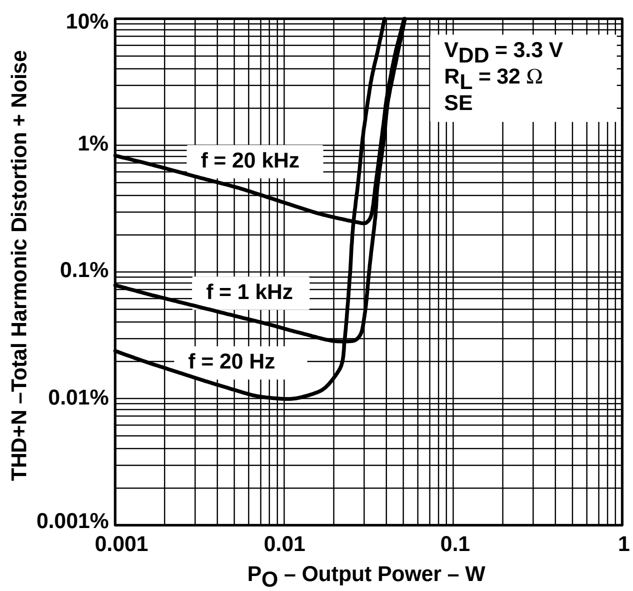


Figure 35

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

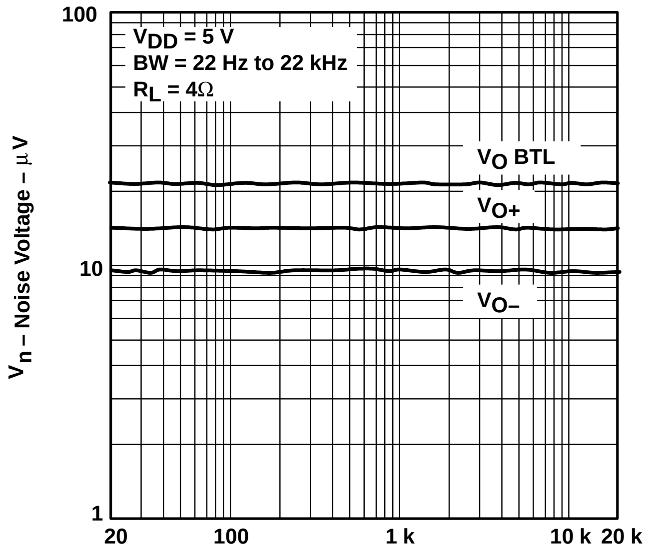


Figure 36

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

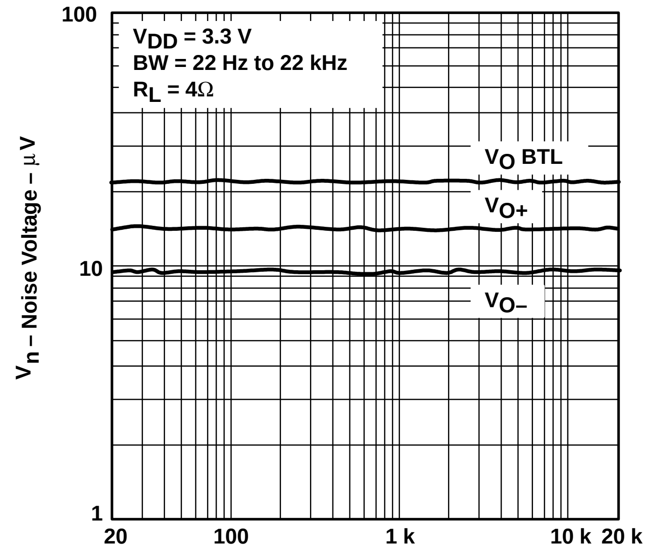


Figure 37

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

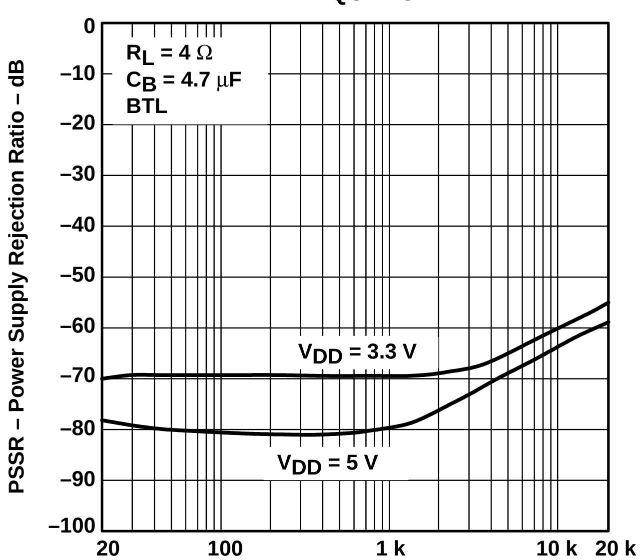


Figure 38

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

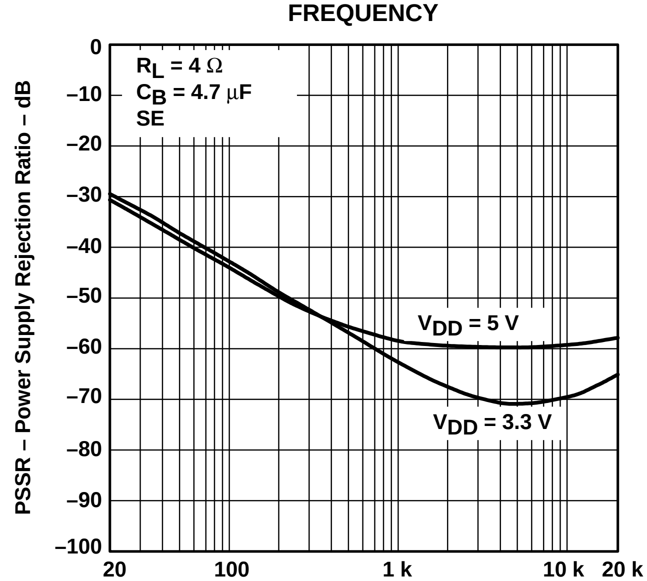


Figure 39

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

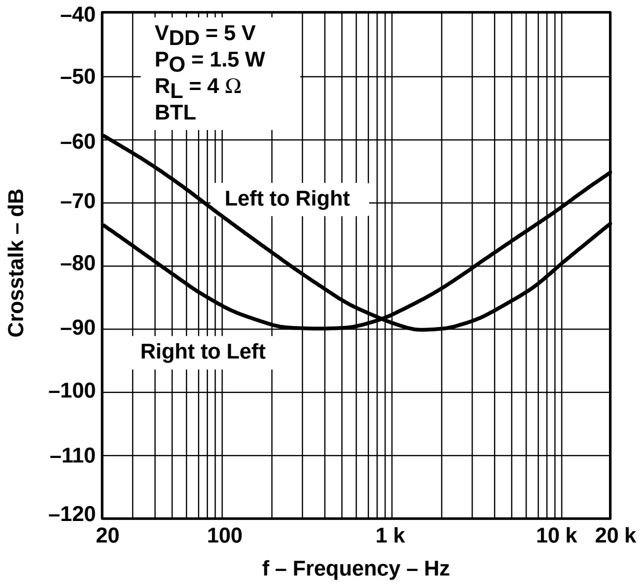


Figure 40

CROSSTALK vs FREQUENCY

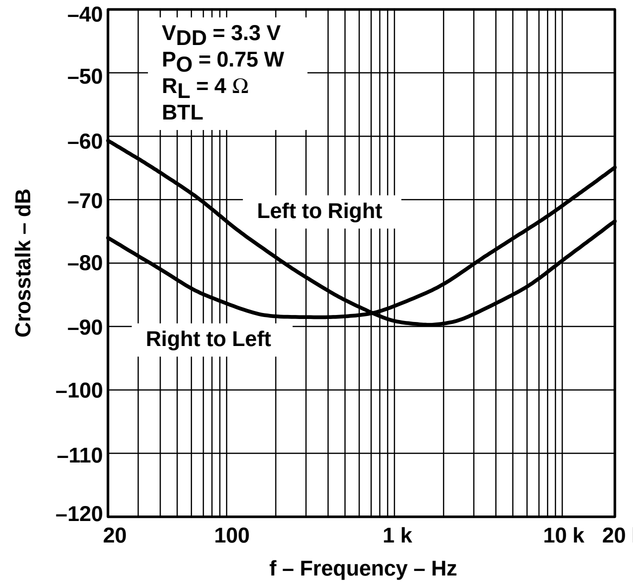


Figure 41

CROSSTALK vs FREQUENCY

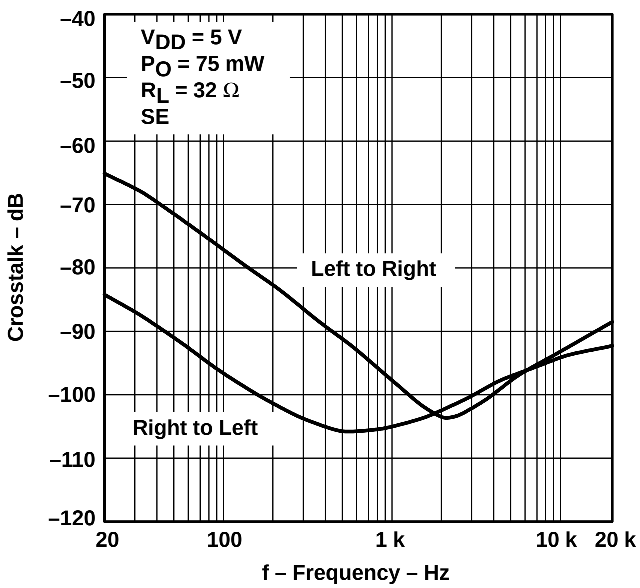


Figure 42

CROSSTALK vs FREQUENCY

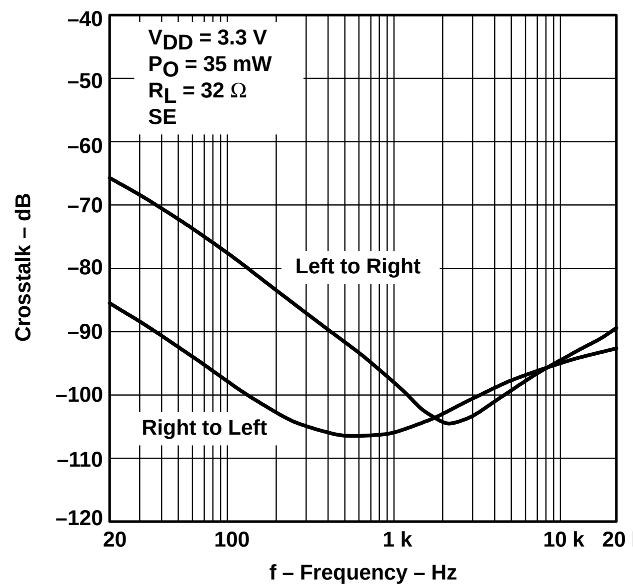


Figure 43

TYPICAL CHARACTERISTICS

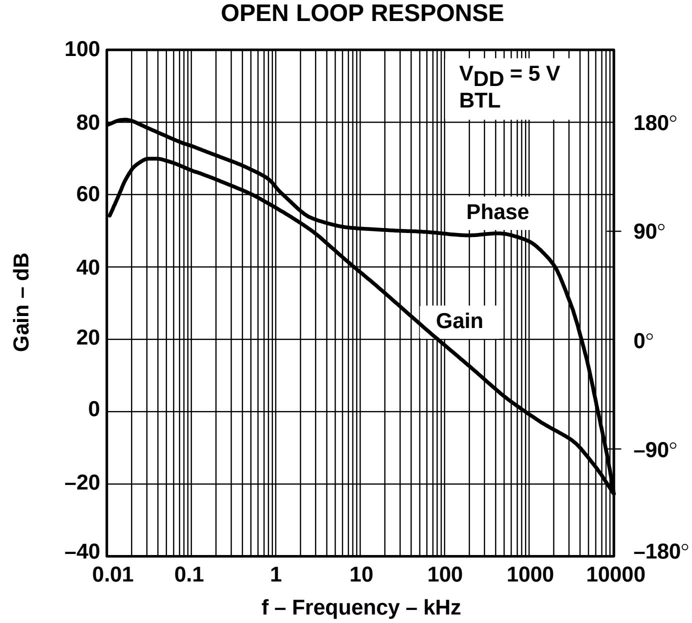


Figure 44

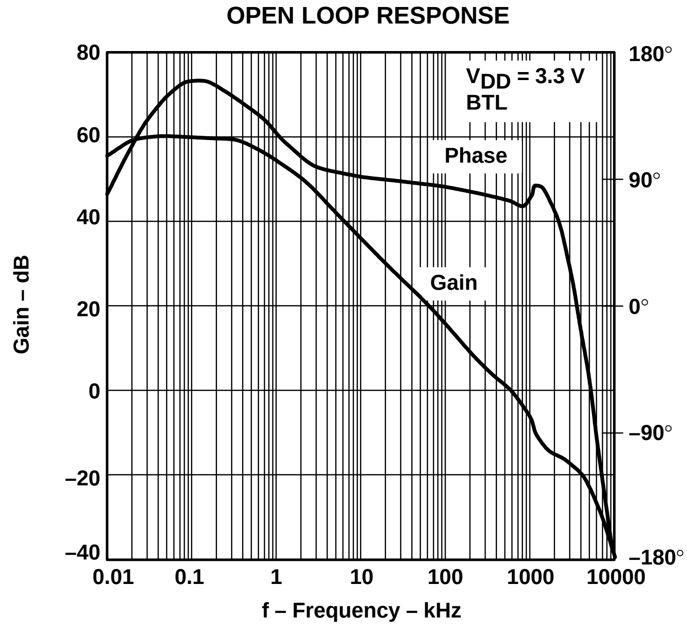


Figure 45

TYPICAL CHARACTERISTICS

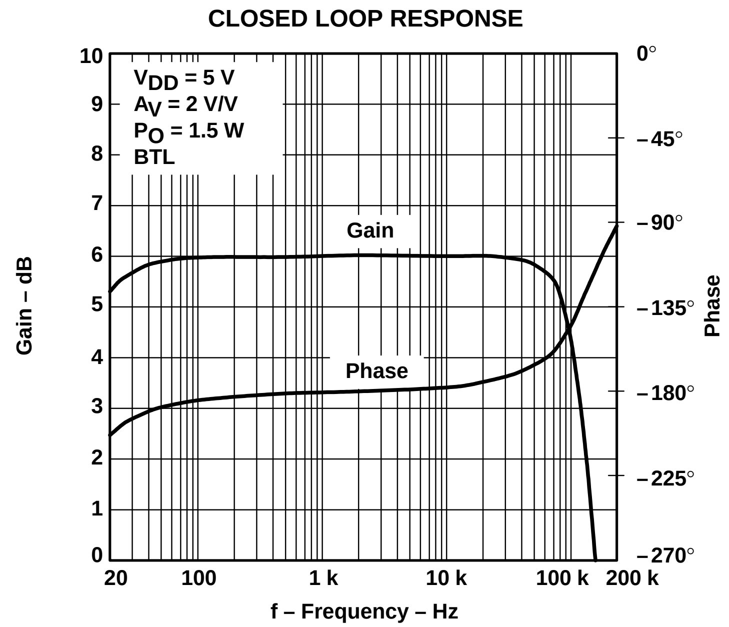


Figure 46

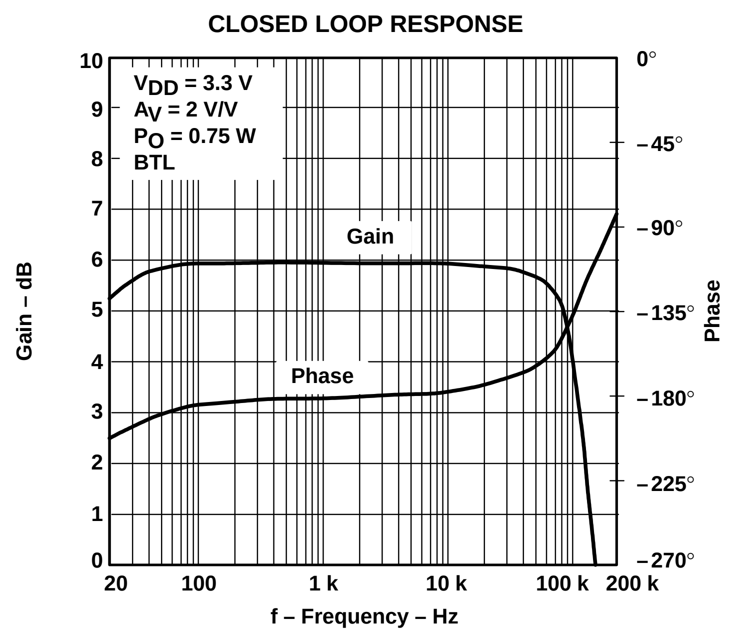


Figure 47

TYPICAL CHARACTERISTICS

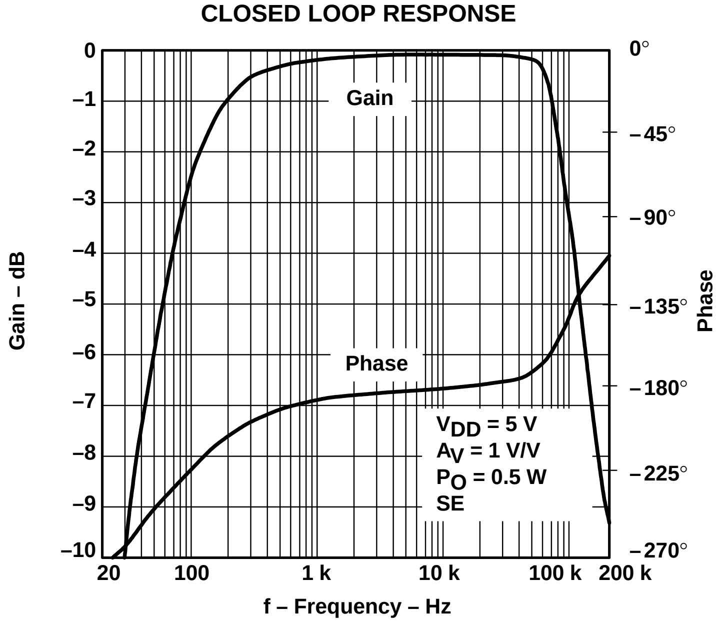


Figure 48

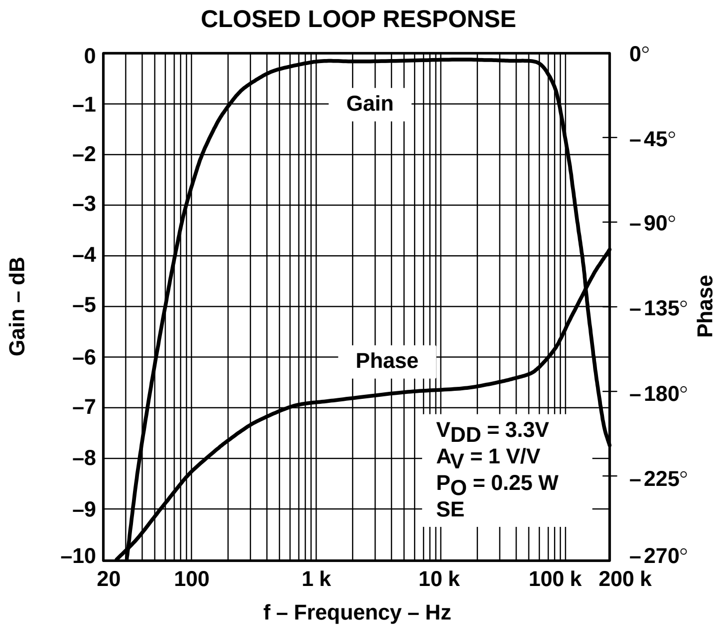


Figure 49

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

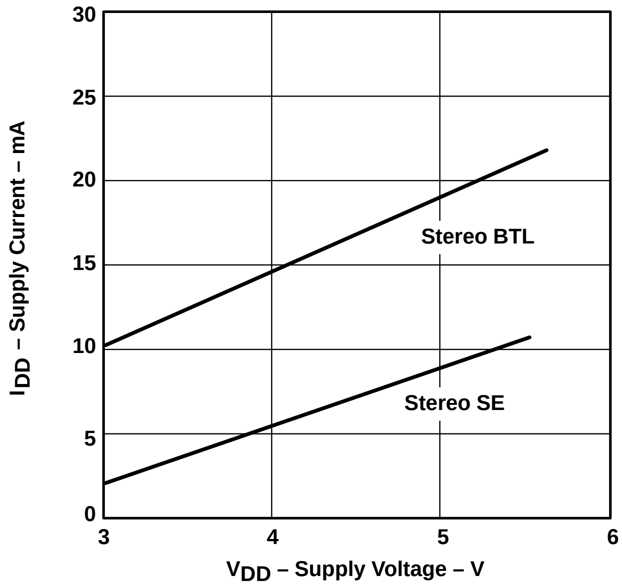


Figure 50

OUTPUT POWER vs SUPPLY VOLTAGE

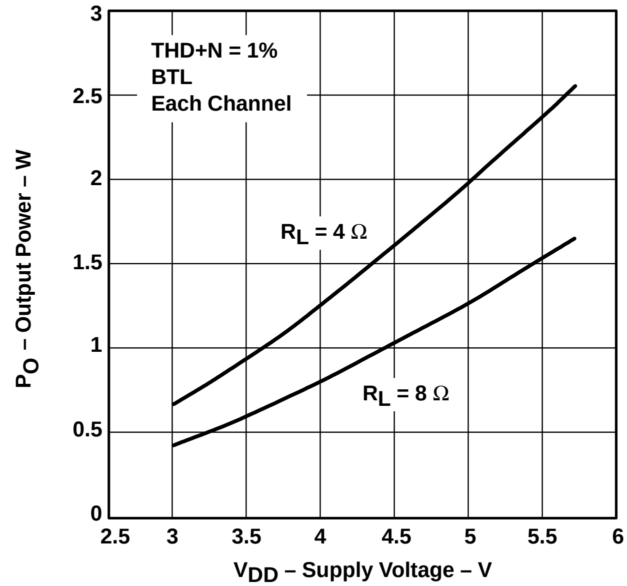


Figure 51

OUTPUT POWER vs SUPPLY VOLTAGE

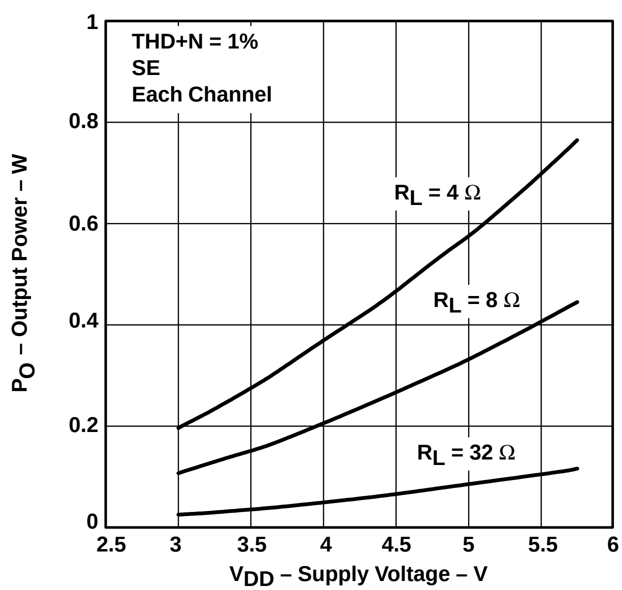


Figure 52

OUTPUT POWER vs LOAD RESISTANCE

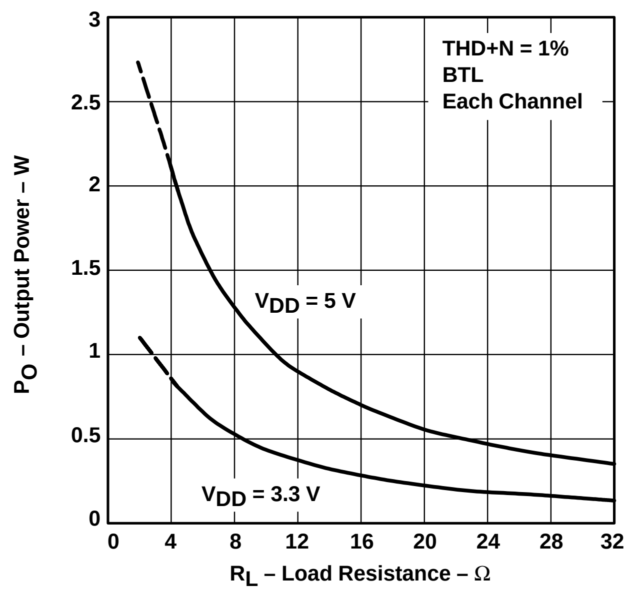


Figure 53

TYPICAL CHARACTERISTICS

OUTPUT POWER vs LOAD RESISTANCE

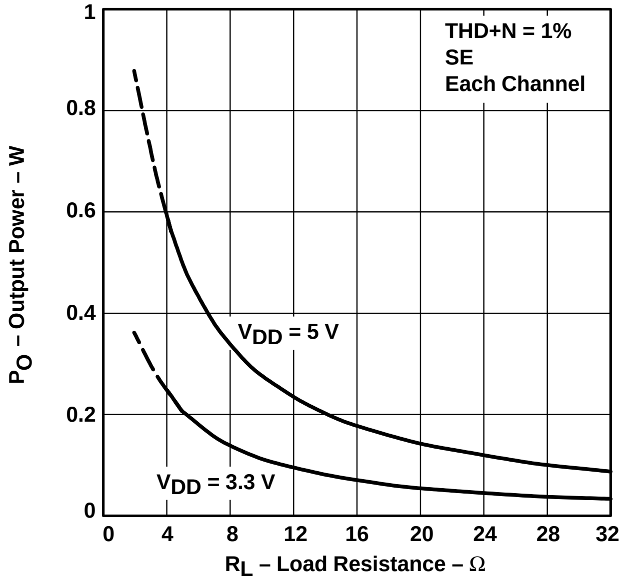


Figure 54

POWER DISSIPATION vs OUTPUT POWER

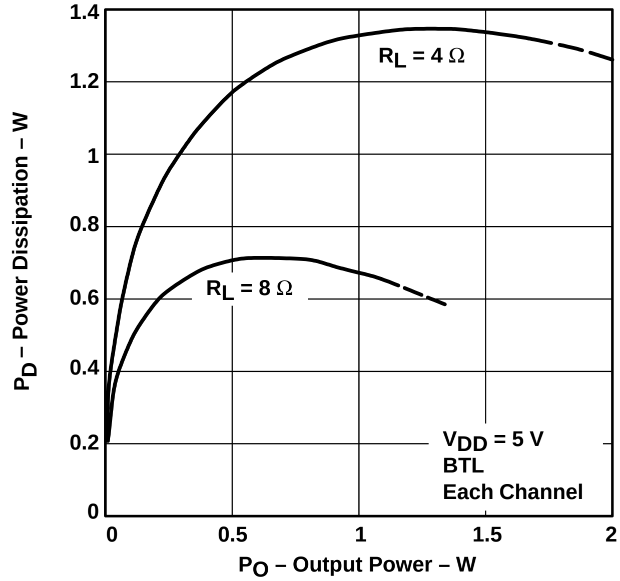


Figure 55

POWER DISSIPATION vs OUTPUT POWER

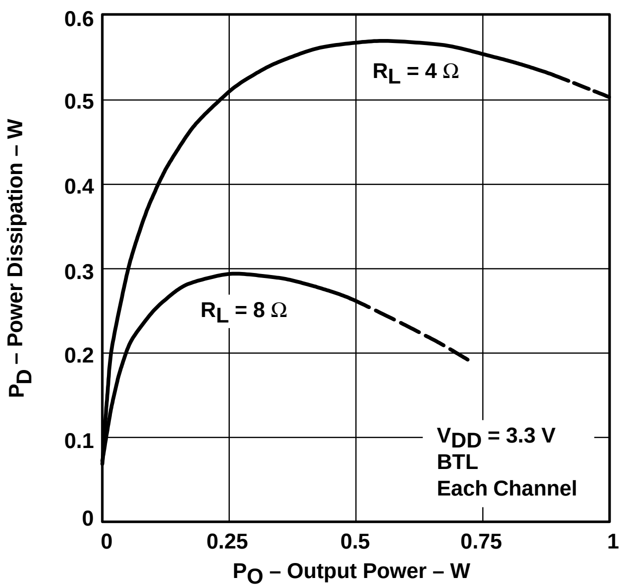


Figure 56

POWER DISSIPATION vs OUTPUT POWER

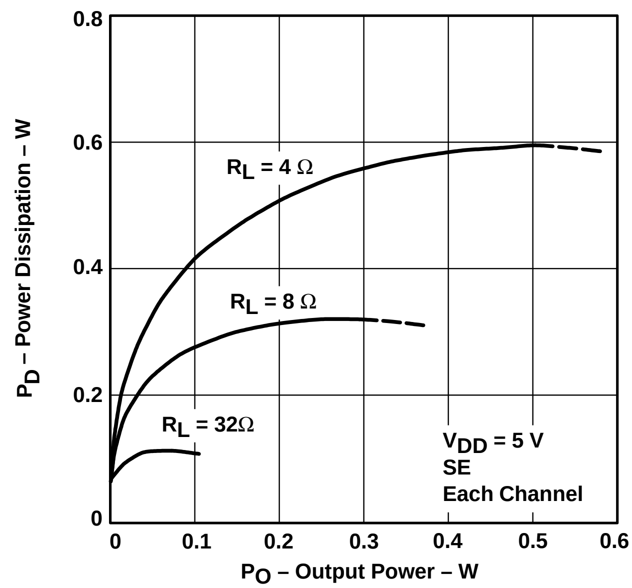


Figure 57

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
OUTPUT POWER

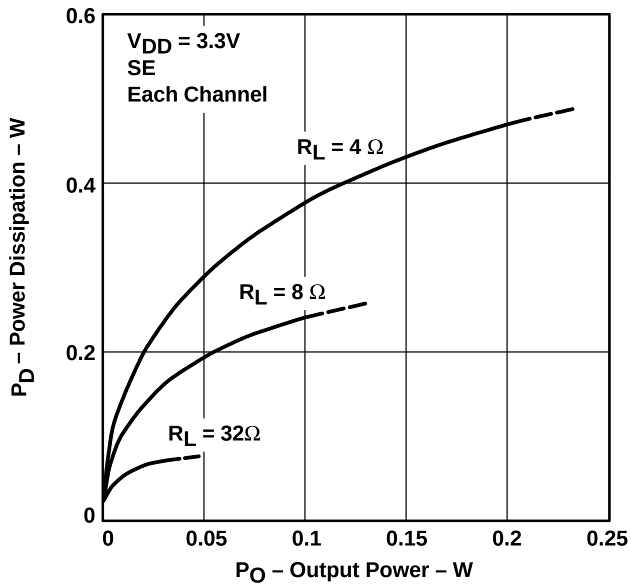


Figure 58

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 59) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

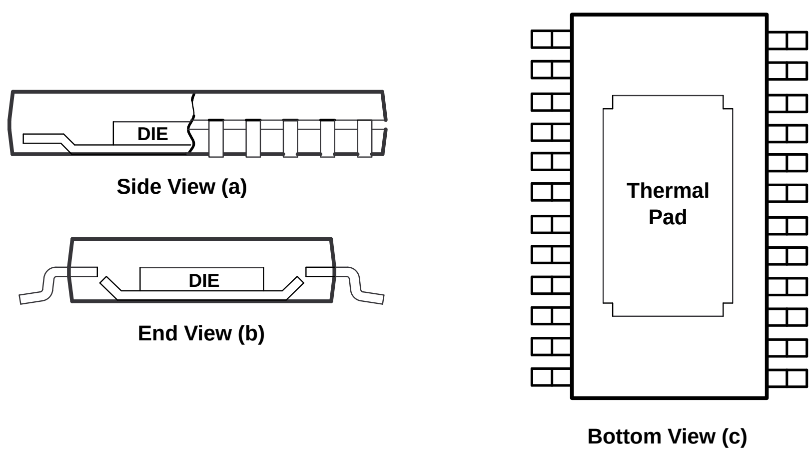


Figure 59. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 60 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0102 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^{\;2}}{R_L} \tag{1}$$

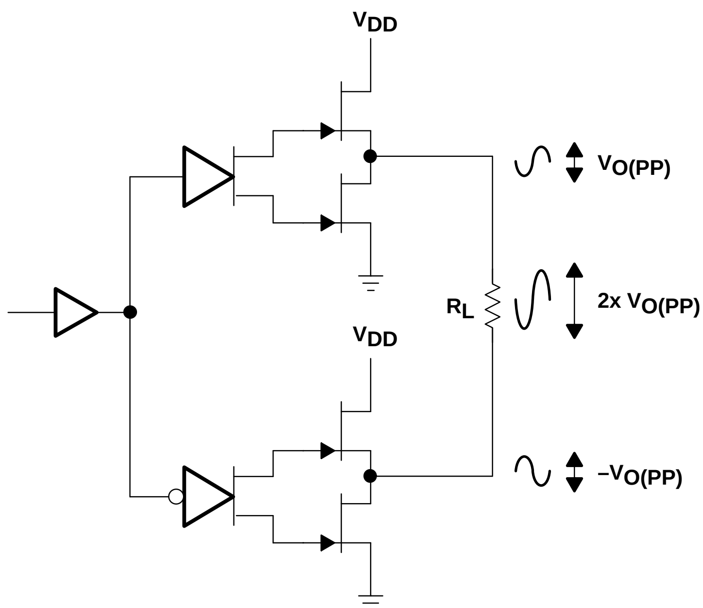


Figure 60. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 61. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

$$f_{(corner)} = \frac{1}{2\pi R_L C_C} \tag{2}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

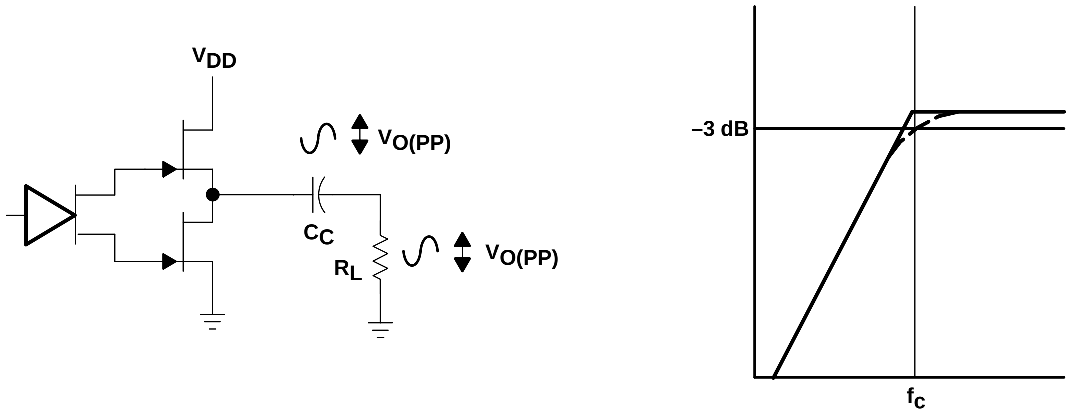


Figure 61. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 62).

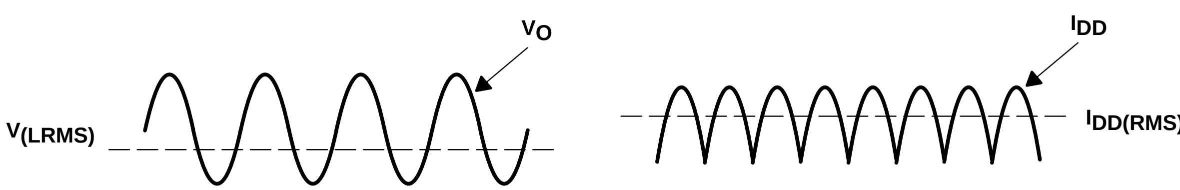


Figure 62. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

where:

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\ I_{DD}\text{rms} = \frac{V_{DD}\ 2V_P}{\pi\ R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\ R_L}$$

$$\begin{array}{c}\text{Effiency of a}\\ \text{BTL Configuration}\end{array} = \frac{\pi\ V_P}{2V_{DD}} = \frac{\pi\left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak-to-Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

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For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0102 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to chose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 63 and Figure 64 are a schematic diagrams of a typical notebook computer application circuits.

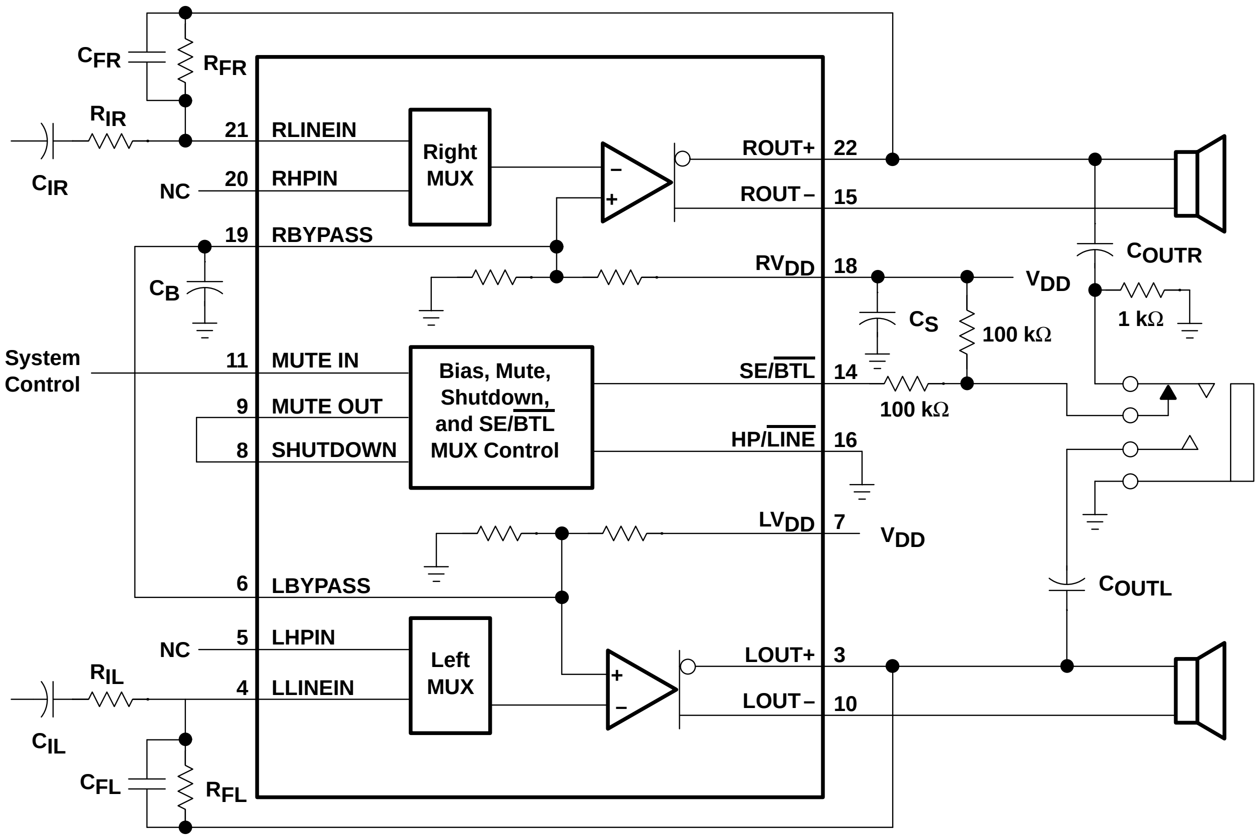
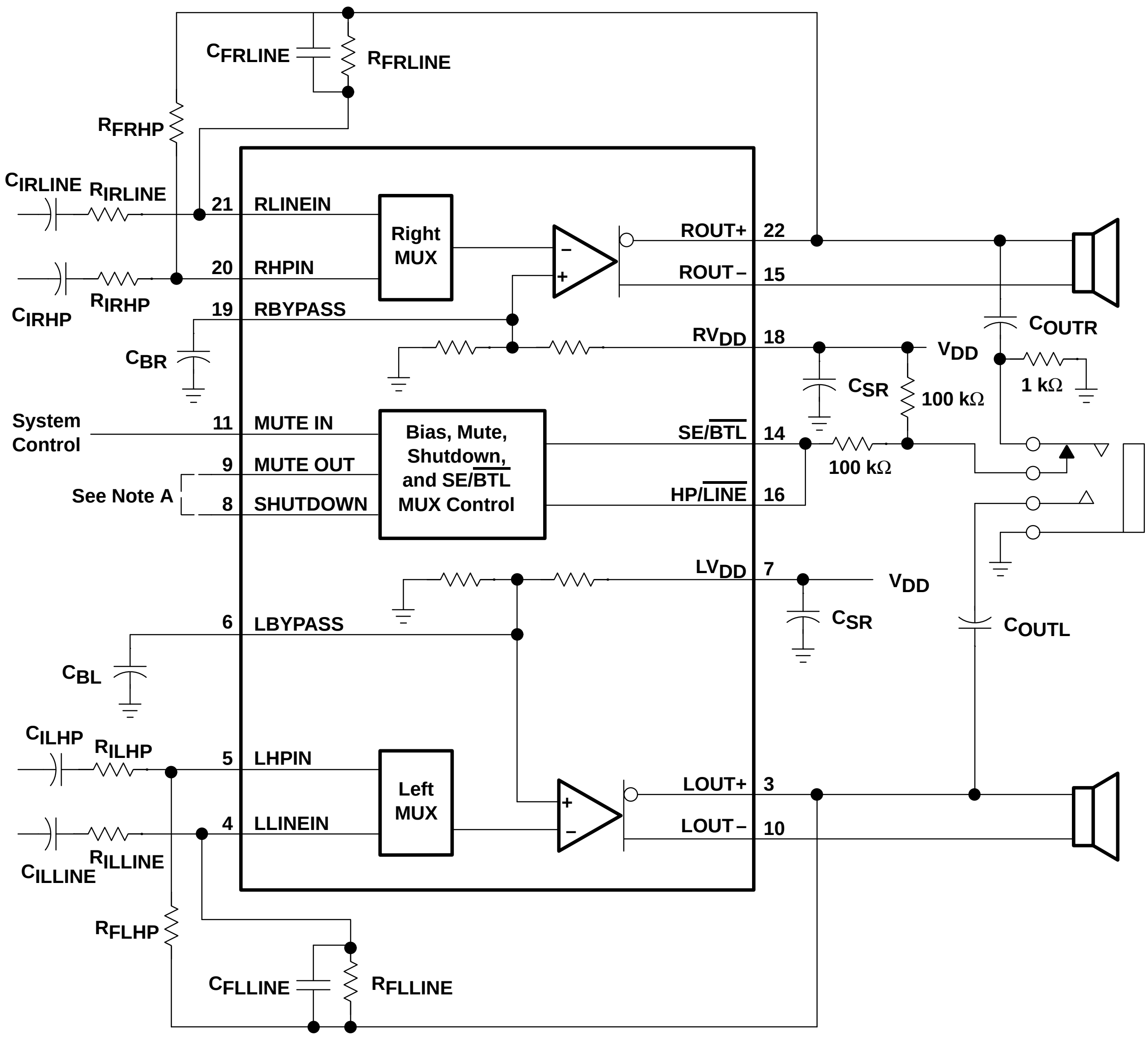


Figure 63. TPA0102 Minimum Configuration Application Circuit

APPLICATION INFORMATION



NOTE A: This connection is for ultra-low current in shutdown mode.

Figure 64. TPA0102 Full Configuration Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0102 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

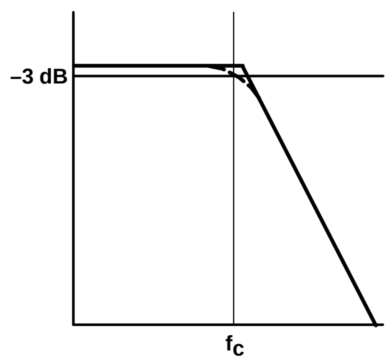
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0102 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{co(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

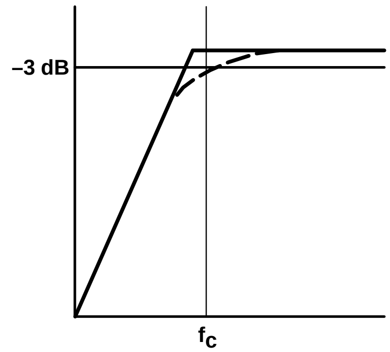


For example, if R_F is 100 kΩ and Cf is 5 pF then f_{co} is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.



$$f_{co(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$

The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_{co}} \tag{9}$$

In this example, C_I is 0.40 µF so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0102 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained.

$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \qquad (10)$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 10 we get:

$$400 \le 454$$

which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

In Figure 64, the full feature configuration, two bypass capacitors are used. This provides the maximum separation between right and left drive circuits. When absolute minimum cost and/or component space is required, one bypass capacitor can be used as shown in Figure 63. It is critical that terminals 6 and 19 be tied together in this configuration.

single-ended operation

In SE mode (see Figure 63 and Figure 64), the load is driven from the primary amplifier output for each channel (OUT+, terminals 22 and 3).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \qquad (11)$$

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

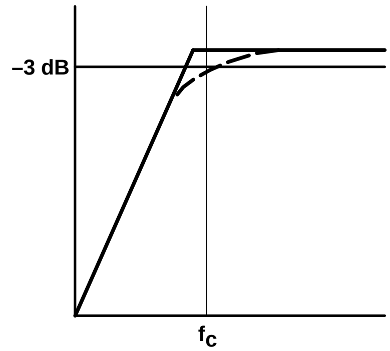
$$\frac{1}{\left(C_B \times 25k\Omega\right)} \le \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \qquad (12)$$

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{out\ high} = \frac{1}{2\pi R_L C_C} \tag{13}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA0102 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the TPA0102, two separate amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input (terminal 14) controls the operation of the follower amplifier that drives LOUT– and ROUT– (terminals 10 and 15). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA0102 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output impedance state, which configures the TPA0102 as an SE driver from LOUT+ and ROUT+ (terminals 3 and 22). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level TTL source or, more typically, from a resistor divider network as shown in Figure 65.

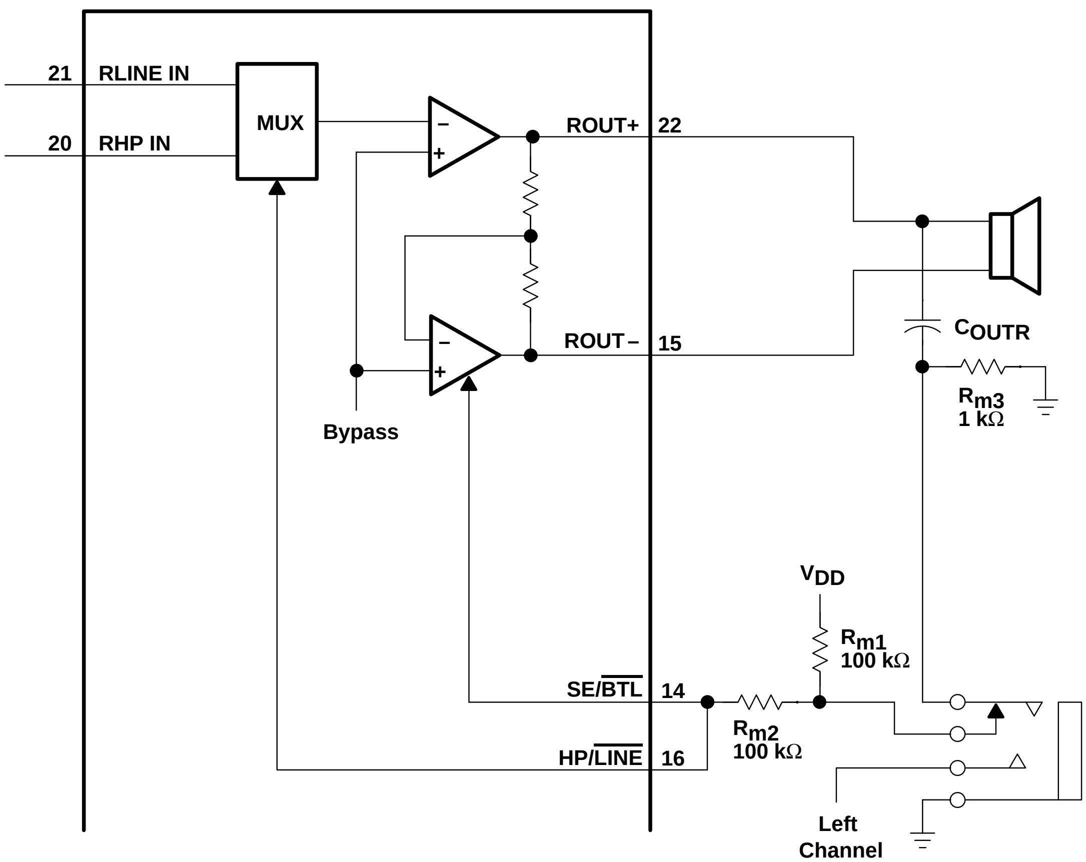


Figure 65. TPA0102 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shutdown causing the speaker to mute (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

As shown in the full feature application (Figure 64), the input MUX control can be tied to the SE/$\overline{\text{BTL}}$ input. The benefits of doing this are described in the following input MUX operation section.

APPLICATION INFORMATION

Input MUX operation

Working in concert with the SE/$\overline{\text{BTL}}$ feature, the HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 66). The primary function of the MUX is to allow different gain settings for BTL versus SE mode. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{SE Gain}_{(HP)} = -\left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \tag{14}$$

If, for example $R_{I(HP)}$ = 20 kΩ and $R_{F(HP)}$ = 20 kΩ then SE $\text{Gain}_{(HP)}$ = –1

$$\text{BTL Gain}_{(LINE)} = -2\left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \tag{15}$$

If, for example $R_{I(LINE)}$ = 20 kΩ and $R_{F(LINE)}$ = 100 kΩ then BTL $\text{Gain}_{(LINE)}$ = –10

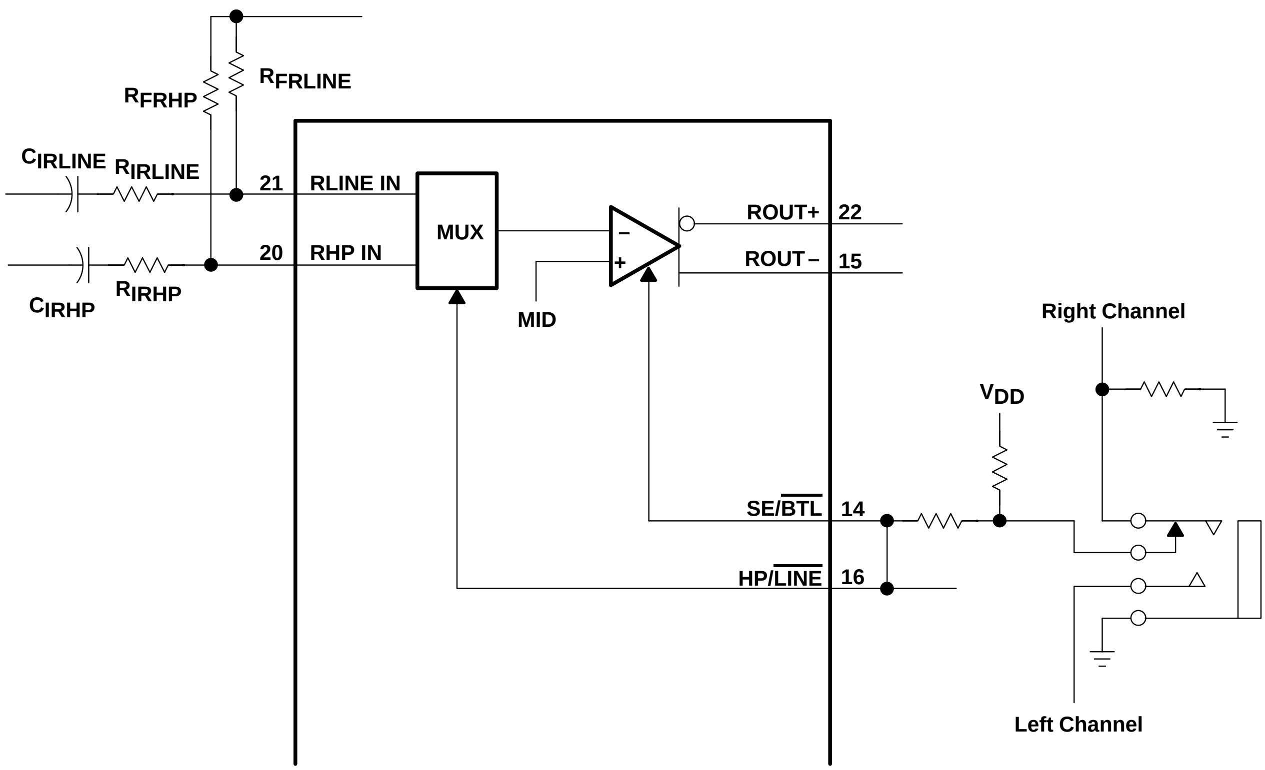


Figure 66. TPA0102 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important. Refer to the SE/$\overline{\text{BTL}}$ operation section for a description of the headphone jack control circuit.

APPLICATION INFORMATION

mute and shutdown modes

The TPA0102 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} < 1 µA. SHUTDOWN or MUTE IN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces I_{DD} < 1 mA.

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	HP/$\overline{\text{LINE}}$	MUTE IN	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	BTL
X	X	—	High	—	X	Mute
X	X	High	—	High	X	Mute
Low	High	Low	Low	Low	L/R HP	BTL
High	Low	Low	Low	Low	L/R Line	SE
High	High	Low	Low	Low	L/R HP	SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0102 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0102 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0102 data sheet, one can see that when the TPA0102 is operating from a 5-V supply into a 4-Ω speaker that 1.5 W peaks are available. Converting Watts to dB:

$$\begin{aligned} P_{dB} &= 10 \operatorname{Log} P_W \\ &= 10 \operatorname{Log} 1.5 \\ &= 1.76 \text{ dB} \end{aligned}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$\begin{aligned} &1.76 \text{ dB} - 15 \text{ dB} = -13.24 \text{ dB (15 dB headroom)} \\ &1.76 \text{ dB} - 12 \text{ dB} = -10.24 \text{ dB (12 dB headroom)} \\ &1.76 \text{ dB} - 9 \text{ dB} = -7.24 \text{ dB (9 dB headroom)} \\ &1.76 \text{ dB} - 6 \text{ dB} = -4.24 \text{ dB (6 dB headroom)} \\ &1.76 \text{ dB} - 3 \text{ dB} = -1.24 \text{ dB (3 dB headroom)} \end{aligned}$$

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{PdB/10} \\ &= 47 \text{ mW (15 dB headroom)} \\ &= 94 \text{ mW (12 dB headroom)} \\ &= 188 \text{ mW (9 dB headroom)} \\ &= 376 \text{ mW (6 dB headroom)} \\ &= 752 \text{ mW (3 dB headroom)} \end{aligned}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 1.5 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA0102 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0102 Power Rating, 5-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE	
			0 CFM	300 CFM
1.5	1.5 W	1.35	28°C	101°C
1.5	752 mW (3 dB)	1.3	33°C	103°C
1.5	376 mW (6 dB)	0.9	69°C	118°C
1.5	188 mW (9 dB)	0.7	87°C	125°C
1.5	94 mW (12 dB)	0.55	100°C	130°C
1.5	47 mW (15 dB)	0.4	114°C	136°C

APPLICATION INFORMATION

headroom and thermal considerations (continued)

DISSIPATION RATING TABLE

PACKAGE	AIR FLOW (CFM)	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	0	2.7 W	21.8 mW/°C	1.7 W	1.4 W
	300	4.0 W	32.1 mW/°C	2.6 W	2.1 W
PWP‡	0	2.8 W	22.1 mW/°C	1.8 W	1.4 W
	300	6.7 W	53.7 mW/°C	4.3 W	3.5 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in^2 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.
‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in^2 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM and 300 CFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in^2 of copper area on a multilayer PCB is 22 mW/°C and 54 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

$$\text{For 0 CFM}: \quad = \frac{1}{0.022} \quad = 45°C/W$$

$$\text{For 300 CFM}: \quad = \frac{1}{0.054} \quad = 18°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0102 is 150 °C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A\ Max = T_J\ Max - \Theta_{JA}\ P_D$$
$$= 150 - 45(0.4 \times 2) = 114°C \text{ (15 dB headroom, 0 CFM)}$$
$$= 150 - 18(0.4 \times 2) = 136°C \text{ (15 dB headroom, 300 CFM)}$$

NOTE:
Internal dissipation of 0.4 W is estimated for a 1.5-W system with 15 dB headroom per channel.

Table 4 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA0102 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.