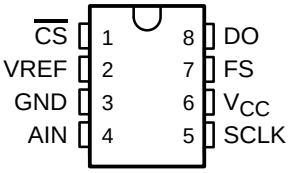
- **Fast Throughput Rate: 1.25 MSPS**
- **8-pin SOIC Package**
- **Differential Nonlinearity Error: < ±1 LSB**
- **Integral Nonlinearity Error: < ±1 LSB**
- **Signal-to-Noise and Distortion Ratio: 59 dB, $f_{(input)}$ = 500 kHz**
- **Single 3-V to 5-V Supply Operation**
- **Very Low Power: 8 mW at 3V; 25mW at 5 V**
- **Auto-Powerdown: 10 μA Maximum**
- **Glueless Serial Interface to TMS320 DSPs and (Q)SPI Compatible Micro-controllers**
- **Inherent Internal Sample and Hold Operation**

D PACKAGE
(TOP VIEW)



Applications

- **Mass Storage and HDD**
- **Automotive**
- **Digital Servos**
- **Process Control**
- **General Purpose DSP**
- **Contact Image Sensor Processing**

description

The TLV1572 is a high-speed 10-bit successive-approximation analog-to-digital converter (ADC) which operates from a single 2.7-V to 5.5-V power supply and is housed in a small 8-pin SOIC package.

The TLV1572 accepts an analog input range from 0 to V_{CC} and digitizes the input at a maximum 1.25MSPS throughput rate. The power dissipation is only 8 mW with 3-V supply or 25 mW with 5-V supply. The part features an auto-powerdown mode that automatically powers down to 10 μA whenever the conversion is not performed.

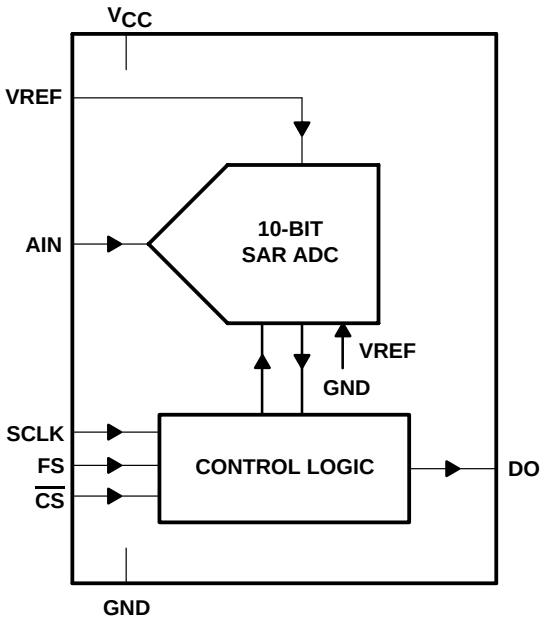
The TLV1572 communicates with digital microprocessors via a simple 3- or 4-wire serial port that interfaces directly to the Texas Instruments' TMS320 DSPs and (Q)SPI compatible microcontrollers without using additional glue logic.

Very high throughput rate, simple serial interface, SO-8 package, 3-V operation, and low power consumption make the TLV1572 an ideal choice for compact or remote high-speed systems.

AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (D)
0°C to 70°C	TLV1572CD
–40°C to 85°C	TLV1572ID

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CS}$/Powerdown	1	I	Chip Select. A logic low on this input enables the TLV1572. A logic high disables the device and disconnects the power to the TLV1572.
AIN	2	I	Analog input
V_{REF}	3	I	Reference voltage input. The voltage applied to this pin defines the input span of the TLV1572.
GND	4		Ground
DO	5	O	Serial data output. A/D conversion results are provided at this output pin.
FS	6	I	Frame sync input in DSP mode. The falling edge of the frame sync pulse from DSP indicates the start of a serial data frame shifted out of the TLV1572. The FS input is tied to V_{CC} when interfacing to a micro-controller.
SCLK	7	I	Serial clock input. This clock synchronizes the serial data transfer and is also used for internal data conversion.
V_{CC}	8		Power supply, recommend connection to analog supply

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, GND to V_{CC} . . . . . –0.3 V to 6.5V
Analog input voltage range . . . . . –0.3 V to V_{CC} + 0.3
Reference input voltage . . . . . V_{CC} + 0.3
Digital input voltage range . . . . . –0.3 V to V_{CC} + 0.3
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supply

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7		5.5	V

analog inputs

		MIN	MAX	UNIT
V_{AIN}	Analog input voltage	GND	V_{REF}	V
V_{REF}	Reference input voltage	2.7	V_{CC}	V

digital inputs

		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}	V_{CC} = 3 V to 5.5 V	2.1	2.4		V
Low-level input voltage, V_{IL}	V_{CC} = 3 V to 5.5 V			0.8	V
Input SCLK frequency	V_{CC} = 4.5 V to 5.5 V			20	MHZ
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	V_{CC} = 4.5 V to 5.5 V	23			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	V_{CC} = 4.5 V to 5.5 V	23			ns
Input SCLK frequency	V_{CC} = 3 V			10	MHZ
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	V_{CC} = 3 V	45			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	V_{CC} = 3 V	45			ns

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, V_{REF} = 5V, f_{SCLK} = 20MHz (unless otherwise noted)

digital specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic inputs						
I_{IH}	High-level input current	V_{CC} = 5V	–50		50	µA
I_{IL}	Low-level input current	V_{CC} = 5V	–50		50	µA
C_i	input capacitance			5		pF
Logic outputs						
V_{OH}	High-level output voltage	I_{OH} = 50µA – 0.5mA	V_{CC}–0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 50µA – 0.5mA		0.4		V
I_{OZ}	High-impedance-state output current		–50		50	µA
C_O	Output capacitance			5		pF

dc specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			10		Bits
Accuracy						
INL	Integral nonlinearity	Best fit		±0.5	±1	LSB
DNL	Differential nonlinearity			±0.3	±1	LSB
	Offset error			±0.1	±0.15	%FSR
	Gain error			±0.1	±0.2	%FSR
Analog input						
	Input full scale range		GND		V_{CC}	V
	Input capacitance			15		pF
	input leakage current	V_{AIN} = 0 to V_{CC}			50	µA
Voltage reference input						
V_{REF+}	Positive reference voltage		3		V_{CC}	V
$V_{REF–}$	Negative reference voltage	Internally connects to GND		GND		V
	Input resistance		2			KΩ
	Input capcitance			300		pF
Power supply						
I_{CC} + I_{REF}	Operating supply current	V_{CC} = 5.5 V, f_{SCLK} = 20MHz		5.5	8.5	mA
		V_{CC} = 3 V, f_{SCLK} = 10MHz		2.7		
I_{PD}	Supply current in powerdown mode	V_{CC}			10	µA
	Power dissipation	V_{CC} = 5 V		25		mW
	Power dissipation	V_{CC} = 3 V		8		mW

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V, V_{REF} = 5V, f_{SCLK} = 20MHz (unless otherwise noted) (continued)

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Signal-to-noise ratio + distortion	$f_{(input)}$ = 200 kHz	54	58		dB
THD	Total harmonic distortion	$f_{(input)}$ = 200 kHz	56	60		dB
	Effective number of bits	$f_{(input)}$ = 200 kHz	8.7	9.35		Bits
	Spurious-free dynamic range	$f_{(input)}$ = 200 kHz	57	62		dB
Analog Input						
BW	Full-power bandwidth	Source impedance = 1 kΩ		12		MHz
BW	Small-signal bandwidth	Source impedance = 1 kΩ		20		Mhz

timing specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	SCLK period	V_{CC} = 4.5 V – 5.5 V	50			ns
t_c	SCLK period	V_{CC} = 2.7 V – 3.3 V	100			ns
t_{rs}	Reset and sampling period			6		SLCK cycles
t_c	Conversion period			10		SLCK cycles
t_{su1}	FS setup time to SCLK falling edge in DSP mode		10			ns
t_{h1}	FS hold time to SCLK falling edge in DSP mode		4			ns
t_{su2}	FS setup time to $\overline{CS}$ falling edge in DSP mode		6			ns
t_{h2}	FS hold time to $\overline{CS}$ falling edge in DSP mode		9			ns
t_{d1}	Output delay after SCLK rising edge in DSP mode			15	25	ns
$t_{d(L)1}$	FS falling edge to next SCLK falling edge in DSP mode		6			ns
$t_L d(L)_2$	SCLK rising edge after $\overline{CS}$ falling edge in µC mode		4			ns
t_{d2}	Output delay after SCLK rising edge in µC mode			15	25	ns

Specifications subject to change without notice.

PARAMETER MEASUREMENT INFORMATION

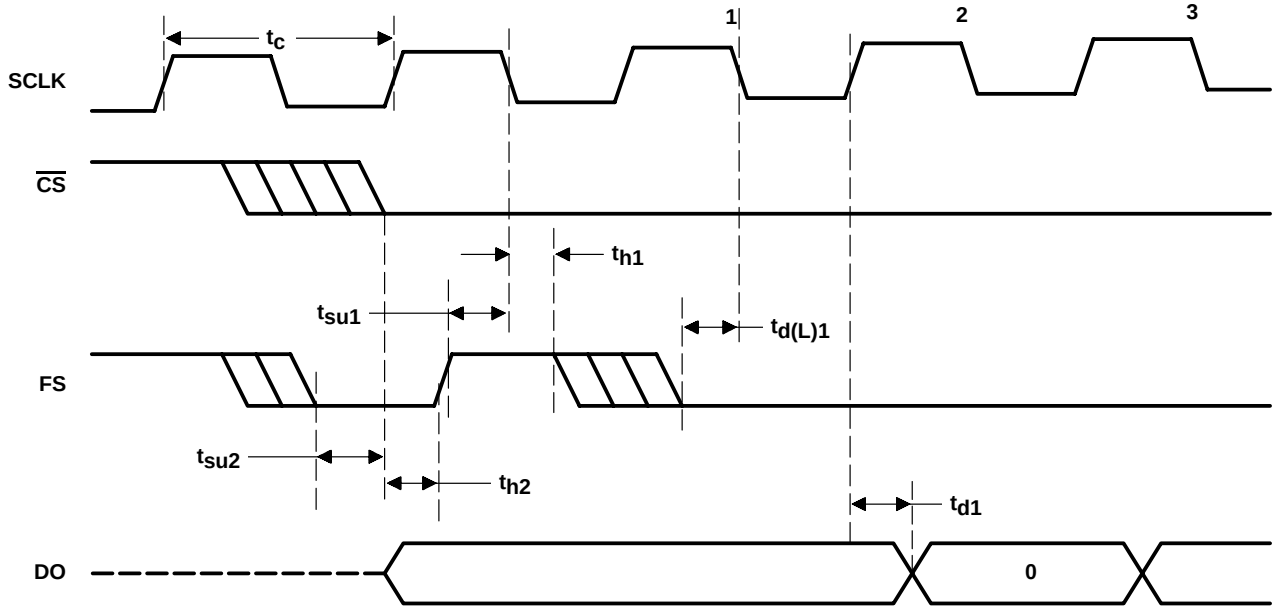


Figure 1. DSP Mode Timing Diagrams

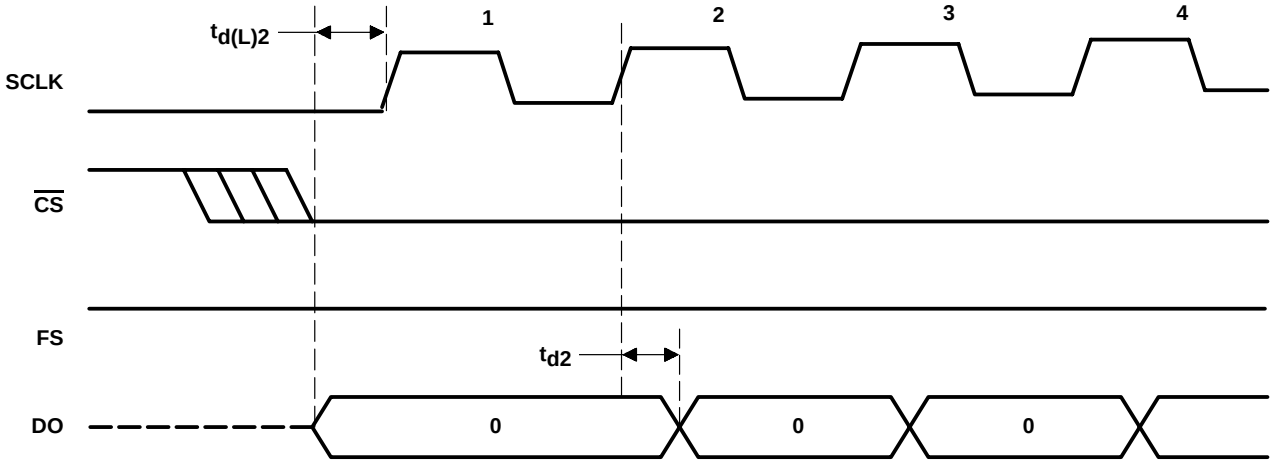


Figure 2. μC Mode Timing Diagrams

definitions of specifications and terminology

integral nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

differential nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

zero offset

The first code transistion should ideally occur at an analog value 1/2 LSB above V_{REF}–. The zero offset error is defined as the error between the ideal first transistion point and the actual first transistion. This error efectively shifts left or right an ADC transfer function

gain error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD – 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the largest peak spurious signal.

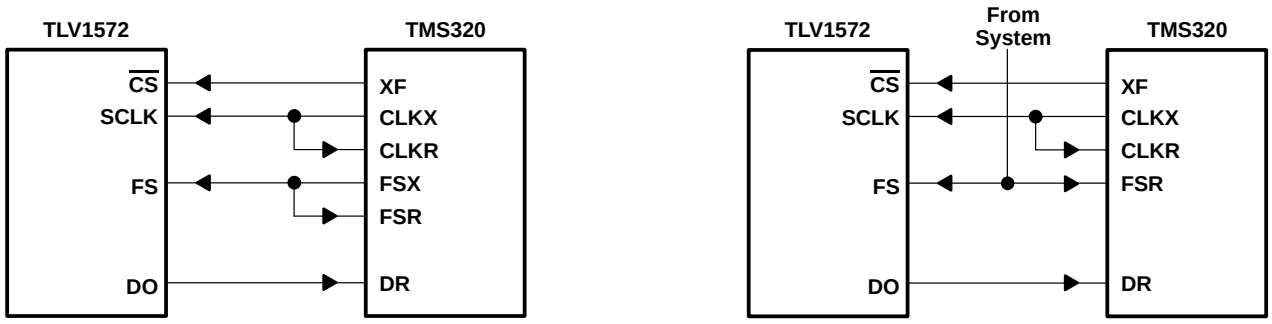
APPLICATION INFORMATION

The TLV1572 is a 600ns, 10-bit analog-to-digital converter with the throughput up to 1.25MSPS at 5V and up to 625KSPS at 3V respectively. To run at its fastest conversion rate, it must be clocked at 20MHz at 5V or 10MHz at 3V. The TLV1572 can be easily interfaced to microcontrollers, ASICs, DSPs, or shift registers. Its serial interface is designed to be fully compatible with Serial Peripheral Interface(SPI) and the TMS320 DSP serial ports. It requires no hardware to interface between the TLV1572 and the microcontrollers (µCs) with the SPI serial port or the TMS320 DSPs. However, the speed will be limited by the SCLK rate of the µC or the DSP.

The TLV1572 interfaces to the DSPs over four lines: $\overline{CS}$, SCLK, DO, and FS, and interfaces to µCs over three lines: $\overline{CS}$, SCLK, and DO. The FS input should be pulled high in µC mode. The chip is in tristate and powerdown mode when the $\overline{CS}$ is high. After the $\overline{CS}$ falls, the TLV1572 checks the FS input at the $\overline{CS}$'s falling edge to determine the operation mode. If the FS is low, the DSP mode is set, else the µC mode is set.

Interfacing TLV1572 to TMS320 DSPs

The TLV1572 is compatible with Texas Instruments TMS320 DSP serial ports. Figures 3 and 4 show the pin connections to interface the TLV1572 to the TMS320 DSPs**.**



a) DSP Serial Port Operating in Burst Mode **b) FS Externally Generated**

Figure 3. DSP to TLV1570 Interface

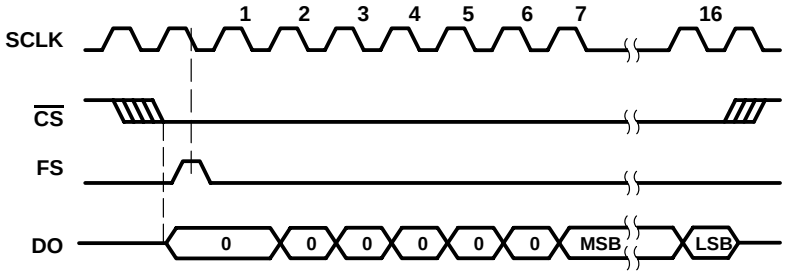


Figure 4. Typical Timing Diagram for DSP Application

In the DSP mode, the FS input should be low when the $\overline{CS}$ goes low. There is a hold time before FS input can go high after the $\overline{CS}$'s falling edge to ensure proper mode latching. With the $\overline{CS}$ going low, the DO comes out of tristate but the chip is still in powerdown until the FS (Frame Sync signal from DSP) comes.

The TLV1572 checks for the FS at the falling edges of SCLK. Once the FS is detected high, the sampling of input is started. As soon as the FS goes low, the chip starts shifting the data out on the DO line. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by DSP on the falling edges. Figure 5 shows the DSP mode timing diagram.

APPLICATION INFORMATION

Interfacing TLV1572 to TMS320 DSPs(continued)

The TLV1572 goes into auto-powerdown after the LSB is shifted out. The next FS pulls it out of auto-powerdown as shown in Fig. 6. If the FS comes on the 16th bit, next conversion cycle starts from next rising edge of the SCLK allowing back to back conversions as shown in Figure 7. An FS in the middle of a conversion cycle resets the chip and starts a new conversion cycle. Therefore variable-bit transfer is supported if the FS appears earlier.

The $\overline{CS}$ can be pulled high asynchronously to put chip into tristate and powerdown. The $\overline{CS}$ can also be pulled low asynchronously to start checking for the FS on the falling edges of clock.

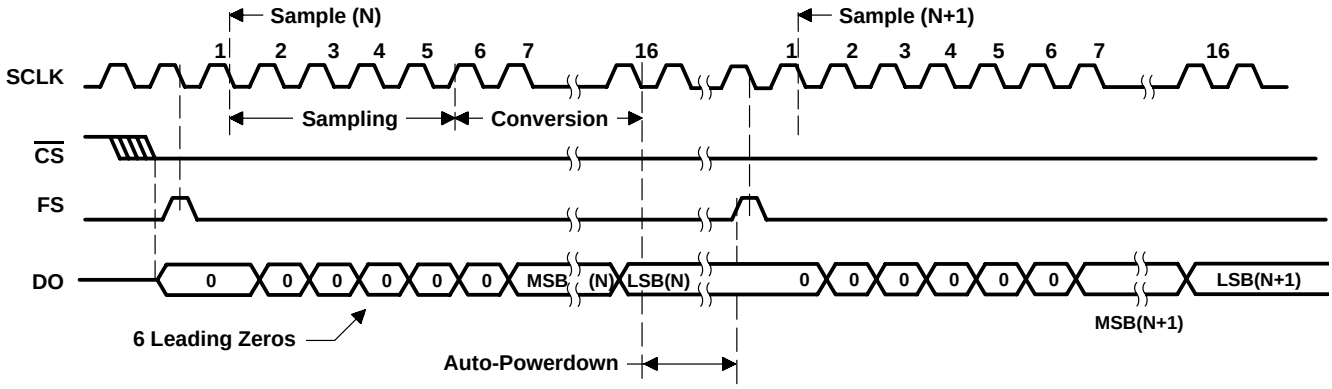


Figure 5. DSP Application Timing (Intermittent Conversion)

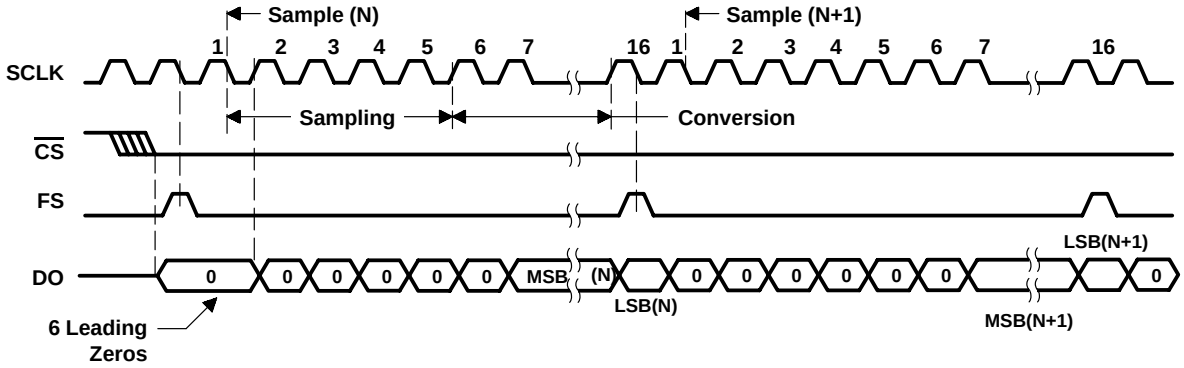


Figure 6. DSP Application Timing (Continuous Conversion)

key points

1. When $\overline{CS}$ goes low, if FS is low, it is DSP mode. FS is sampled twice by $\overline{CS}$ falling edge and again by internally delayed $\overline{CS}$ falling edge. Even if a glitch appears and one latch latches 1 and another latches 0, chip goes into DSP mode (µC mode requires both latches to latch 1). There is a hold time before FS can go high again after $\overline{CS}$ falling edge to ensure proper mode latching as detailed above. With $\overline{CS}$ going low, DO is in tristate and the chip is in powerdown until FS rising edge.
2. 1572 checks for FS at every falling edge of SCLK. If FS is detected high, chip goes into reset. When FS goes low, 1572 waits for DSP to latch the first bit 0.
3. Sampling occurs from first falling edge of SCLK after FS going low till the rising edge when 6th bit 0 is given out. There after decisions are taken on rising edges and data is given out on rising edges a bit delayed. DSP samples on falling edge of SCLK. Data is padded with 6 leading zeros.

APPLICATION INFORMATION

key points (continued)

4. Note that chip goes into autopowerdown on the 17th falling edge of SCLK (just after LSB). FS rising edge pulls it out of autopowerdown. If FS comes on the 16th bit itself, next conversion cycle starts from next rising edge allowing back to back conversions. An FS in the middle of a conversion cycle starts a new conversion cycle. Thus variable-bit transfer is supported if FS appears earlier.
5. DO goes into tristate on the 17th rising edge and comes out on FS rising edge.
6. $\overline{CS}$ can be pulled high asynchronously to put chip into tristate and powerdown. $\overline{CS}$ may also be pulled low asynchronously to start checking for FS on falling edges of clock

For applications where the analog input must be sampled at a precise instant in time, the data conversion can be initiated by an external conversion start pulse which is completely asynchronous to the SCLK as shown in Figure 4. When a conversion start pulse is received, the pulse is used as a Frame Sync (FS) signal to initiate the data conversion and transfer. The corresponding timing diagram is shown in Figure 6.

Interfacing TLV1572 to SPI/QSPI compatible microcontrollers(μCs)

The TLV1572 is compatible with SPI and QSPI serial interface standards (Note: the TLV1572 supports the following SPI clock options: CLOCK_POLARITY= 0, i.e. SCLK idles low, and CLOCK_PHASE = 1). Figure 8 shows the pin connections to interface the TLV1572 to the SPI/QSPI compatible microcontrollers.

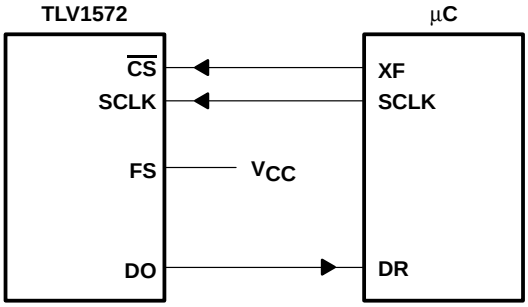


Figure 7. μC to TLV1572 Interface

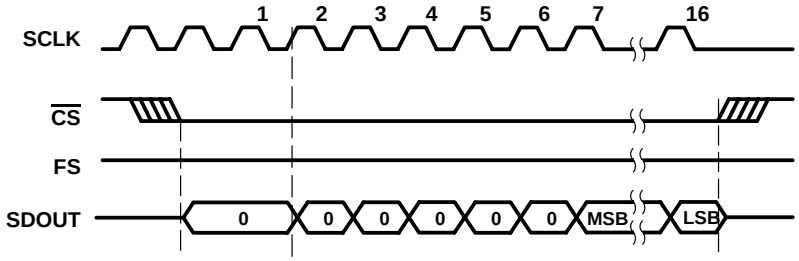


Figure 8. Typical Timing Diagram for μC Application

To use the TLV1572 in a non-DSP application, the FS input should be pulled high as shown in Figure 8.

A total of 16 clocks are normally supplied for each conversion. If μC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks. The $\overline{CS}$ should be kept low throughout the conversion. The delay between these two 8-clock periods should not be longer than 100μs.

APPLICATION INFORMATION

Interfacing TLV1572 to SPI/QSPI compatible microcontrollers(μCs)(continued)

Unlike the DSP mode in which the conversion is initiated by the FS input signal from the DSP, the conversion is initiated by the incoming SCLK after the $\overline{CS}$ falls. The sampling of input is started on the first rising edge of the SCLK after the $\overline{CS}$ goes down. After six null bits, the A/D conversion data becomes available on the SCLK rising edges and is latched by μC on the falling edges. The $\overline{CS}$ can be pulled high during the conversion before the LSB is shifted out to use the chip as a lower resolution ADC. Figure 9 shows the μC mode timing diagram.

The chip goes into autopowerdown after the LSB is shifted out and is brought out of the powerdown by next clock's rising edge as shown in Figure 10.

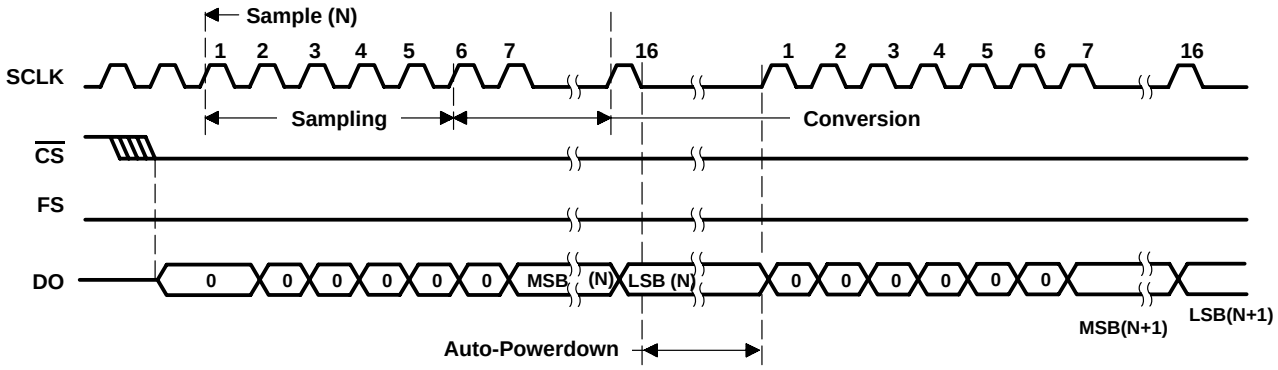


Figure 9. μC Application

key points

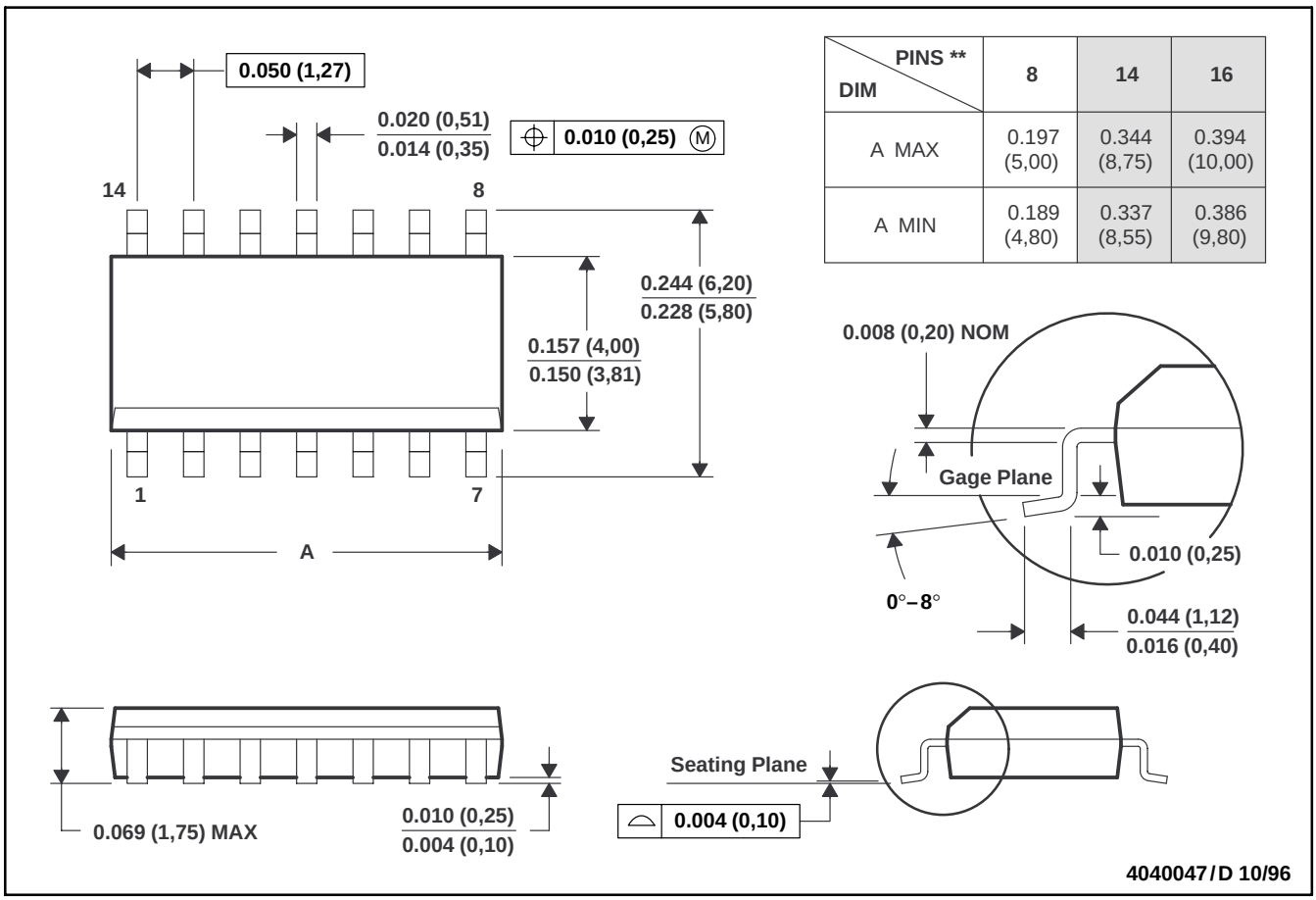
1. When $\overline{CS}$ goes low, if FS is high, it is μC ({Q}SPI) mode. Thus, FS should be tied to VDD. FS is latched twice, on $\overline{CS}$ falling edge and again on internally delayed $\overline{CS}$ falling edge. Only if both latches latch 1, the μC mode is set else DSP mode is set. Only polarity = 0 is supported i.e. SCLK idles low. Only clock_phase = 1 is supported as shown in timing diagrams.
2. 16 clocks have to be supplied for each conversion. If μC cannot take in 16 bits at a time, it may take 8 bits with 8 clocks and next 8 bits with another 8 clocks keeping $\overline{CS}$ low throughout the conversion. The delay between these two 8-clock periods should not be higher than 100 ns.
3. Sampling starts on first falling edge of SCLK and ends on the edge when 6th bit 0 is given out. Decisions are made on the rising edge and data is output on the same edge but a bit delayed to avoid noise.

4. Chip goes into autopowerdown on the 16th clock's falling edge and is brought out of it by next 1st(17th) clock's rising edge.
5. If (Q)SP wants less than 16-bit transfer, $\overline{CS}$ must go high after each transfer. The falling edge of $\overline{CS}$ will reset the 1572 for the next conversion. Thus one may do a 14-bit transfer to use the chip as an 8-bit A/D.
6. $\overline{CS}$ going high puts chip in tristate and complete powerdown. $\overline{CS}$ going low merely sets the mode and pulls DO out of tristate.

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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