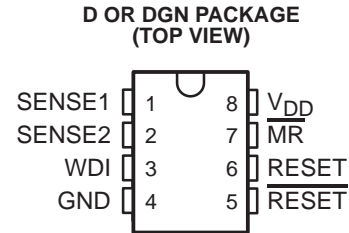
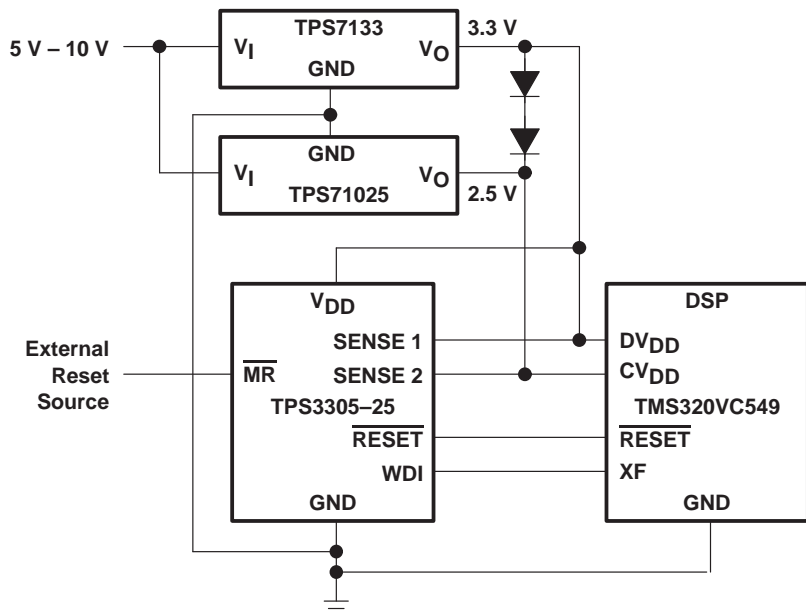


- Dual Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed
- Watchdog Timer Retriggeres the  $\overline{\text{RESET}}$  Output at  $\text{SENSE}_n \geq V_{IT+}$
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40  $\mu\text{A}$
- Supply Voltage Range . . . 2.7 V to 6 V
- Defined  $\overline{\text{RESET}}$  Output from  $V_{DD} \geq 1.1 \text{ V}$
- MSOP-8 and SO-8 Packages
- Temperature Range . . . - 40°C to 85°C



### typical applications

Figure 1 lists some of the typical applications for the TPS3305 family, and a schematic diagram for a DSP-based system application. This application uses TI part numbers TPS3305–25, TPS7133, TPS71025, and TMS320VC549.



- Applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

Figure 1. Applications Using the TPS3305 Family

### description

The TPS3305 family is a series of micropower supply voltage supervisors designed for circuit initialization, primarily in DSP and processor-based systems, which require two supply voltages.

The product spectrum of the TPS3305 is designed for monitoring two independent supply voltages of 3.3 V/1.8 V, 3.3 V/2.5 V or 3.3 V/5 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

# TPS3305-18, TPS3305-25, TPS3305-33 DUAL PROCESSOR SUPERVISORS

SLVS198 – DECEMBER 1998

## description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage, as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3305-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3305-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3305-33	5 V	3.3 V	4.55 V	2.93 V

During power-on,  $\overline{\text{RESET}}$  is asserted when the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps  $\overline{\text{RESET}}$  active as long as SENSEn remains below the threshold voltage  $V_{IT+}$ .

An internal timer delays the return of the  $\overline{\text{RESET}}$  output to the inactive state (high) to ensure proper system reset. The delay time,  $t_{d\text{typ}} = 200 \text{ ms}$ , starts after SENSE1 and SENSE2 inputs have risen above the threshold voltage  $V_{IT+}$ . When the voltage at SENSE1 or SENSE2 input drops below the threshold voltage  $V_{IT-}$ , the  $\overline{\text{RESET}}$  output becomes active (low) again.

The TPS3305-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval,  $t_{t(\text{out})} = 1.6 \text{ s}$ ,  $\overline{\text{RESET}}$  becomes active for the time period  $t_d$ . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3305-xx family of devices incorporates a manual reset input,  $\overline{\text{MR}}$ . A low level at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to become active. In addition to the active-low  $\overline{\text{RESET}}$  output, the TPS3305-xx family includes an active-high RESET output.

The TPS3305-xx devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3305-xx family is characterized for operation over a temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

AVAILABLE OPTIONS

TA	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ $\mu$ -SMALL OUTLINE (DGN)		
$-40^\circ\text{C}$ to $85^\circ\text{C}$	TPS3305-18D	TPS3305-18DGN	TIAAM	TPS3305-18Y
	TPS3305-25D	TPS3305-25DGN	TIAAN	TPS3305-25Y
	TPS3305-33D	TPS3305-33DGN	TIAAO	TPS3305-33Y

PowerPAD is a trademark of Texas Instruments Incorporated.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

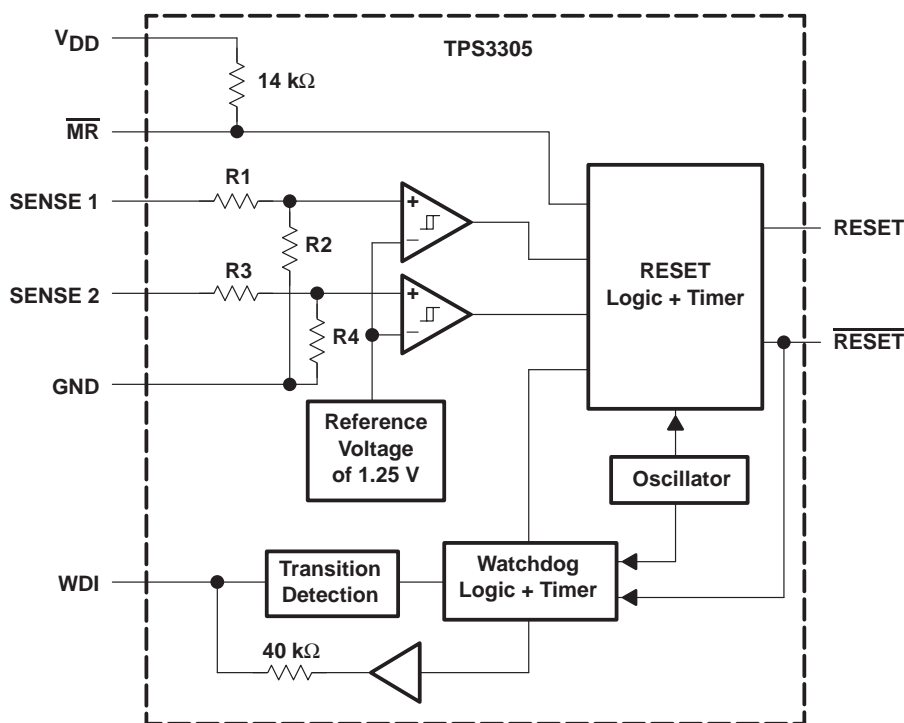
description (continued)

FUNCTION/TRUTH TABLES

$\overline{\text{MR}}$	$\text{SENSE1} > V_{IT1}$	$\text{SENSE2} > V_{IT2}$	$\overline{\text{RESET}}$	RESET
L	X†	X†	L	H
H	0	0	L	H
H	0	0	L	H
H	0	1	L	H
H	0	1	L	H
H	1	0	L	H
H	1	0	L	H
H	1	1	L	H
H	1	1	H	L

† X = Don't care

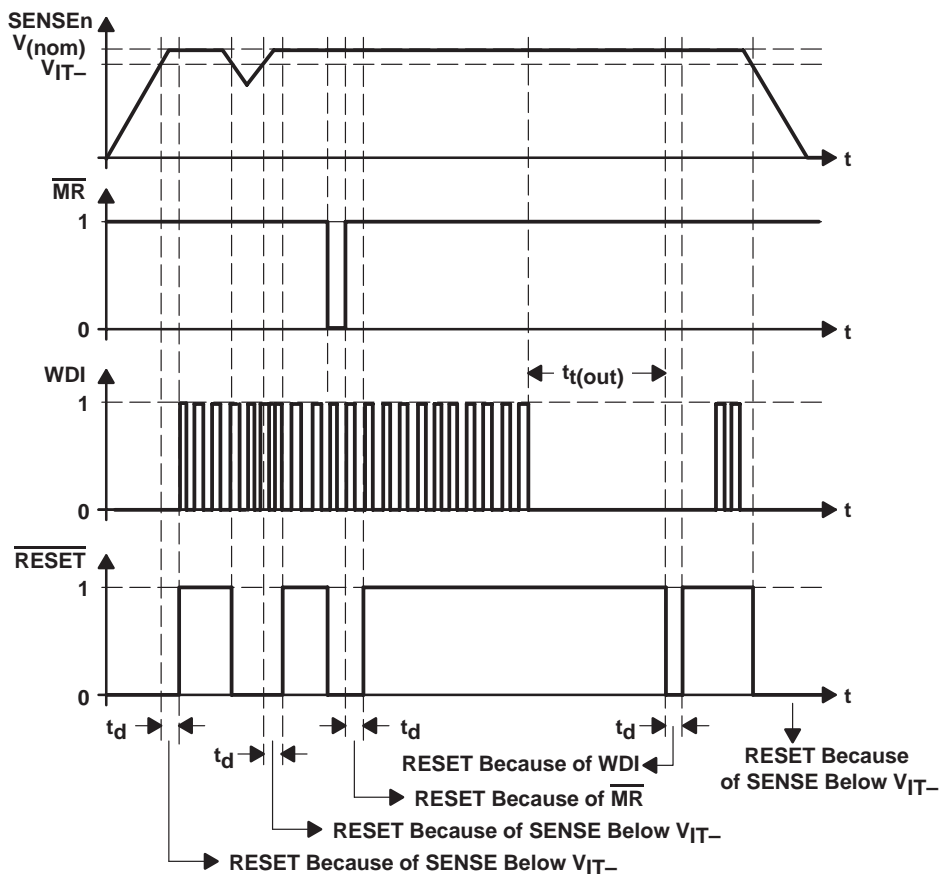
functional block diagram



# TPS3305-18, TPS3305-25, TPS3305-33 DUAL PROCESSOR SUPERVISORS

SLVS198 – DECEMBER 1998

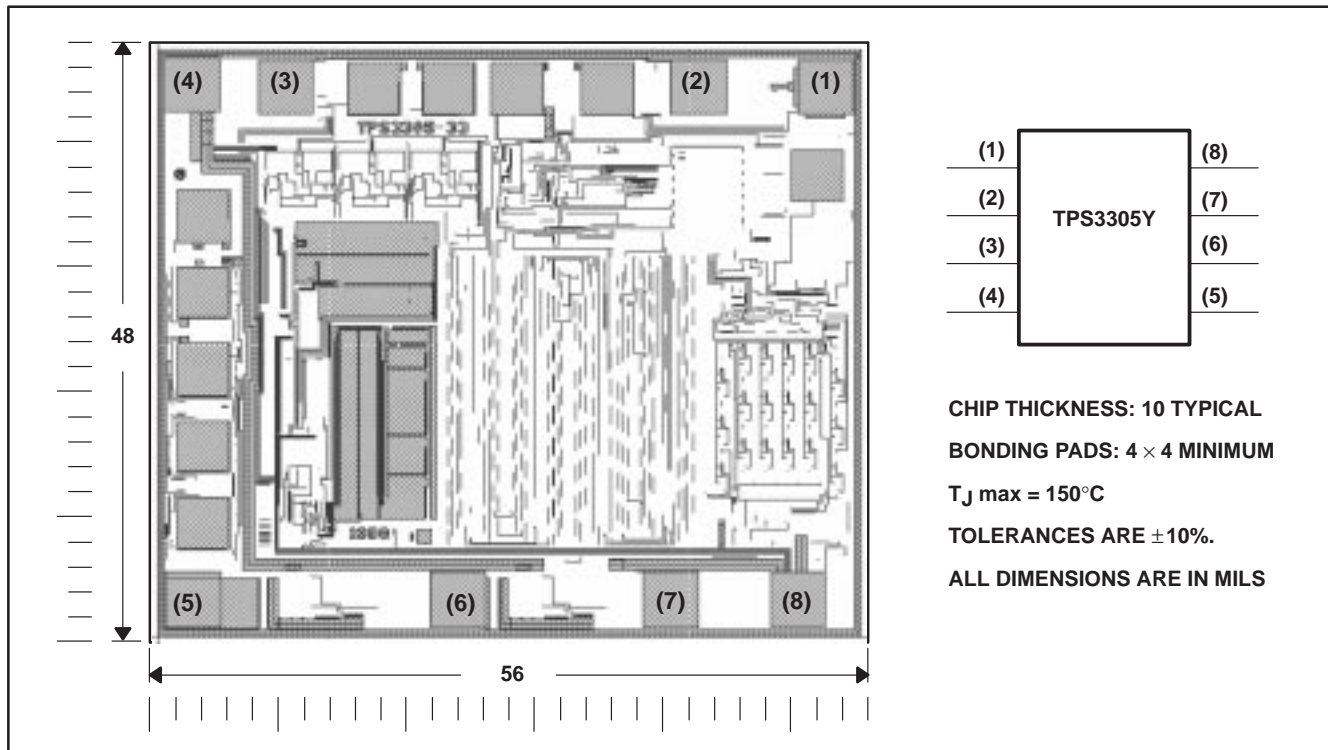
## timing diagram



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**TPS3305Y chip information**

These chips, when properly assembled, display characteristics similar to those of the TPS3305. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



**Terminal Functions**

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{\text{MR}}$	7	I	Manual reset
$\overline{\text{RESET}}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
WDI	3	I	Watchdog timer input
V <sub>DD</sub>	8		Supply voltage

# TPS3305-18, TPS3305-25, TPS3305-33 DUAL PROCESSOR SUPERVISORS

SLVS198 – DECEMBER 1998

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note1)	7 V
All other pins (see Note 1)	- 0.3 V to 7 V
Maximum low output current, $I_{OL}$	5 mA
Maximum high output current, $I_{OH}$	- 5 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{DD}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{DD}$ )	$\pm 20$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	-40°C to 85°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than  $t = 1000$  h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DGN	2.14 mW	17.1 mW/°C	1.37 mW	1.11 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

## recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, $V_{DD}$	2.7	6	V
Input voltage at $\overline{MR}$ and WDI, $V_I$	0	$V_{DD}+0.3$	V
Input voltage at SENSE1 and SENSE2, $V_I$	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$ and WDI, $V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage at $\overline{MR}$ and WDI, $V_{IL}$	$0.3 \times V_{DD}$		V
Input transition rise and fall rate at $\overline{MR}$ , $\Delta t/\Delta V$	50		ns/V
Operating free-air temperature range, $T_A$	-40	85	°C



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	V <sub>DD</sub> = 2.7 V to 6 V, I <sub>OH</sub> = -20 μA	V <sub>DD</sub> - 0.2V			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 mA	V <sub>DD</sub> - 0.4V				
		V <sub>DD</sub> = 6 V, I <sub>OH</sub> = -3 mA	V <sub>DD</sub> - 0.4V				
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 2.7 V to 6 V, I <sub>OL</sub> = 20 μA	0.2			V	
		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA	0.4				
		V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA	0.4				
Power-up reset voltage (see Note 2)		V <sub>DD</sub> ≥ 1.1 V, I <sub>OL</sub> = 20 μA	0.4			V	
V <sub>IT-</sub>	Negative-going input threshold voltage (see Note 3)	V <sub>DD</sub> = 2.7 V to 6 V, T <sub>A</sub> = 0°C to 85°C	1.64	1.68	1.72	V	
			2.20	2.25	2.30		
			2.86	2.93	3		
			4.46	4.55	4.64		
	V <sub>DD</sub> = 2.7 V to 6 V, T <sub>A</sub> = -40°C to 85°C	V <sub>DD</sub> = 2.7 V to 6 V, T <sub>A</sub> = -40°C to 85°C	1.64	1.68	1.73	V	
			2.20	2.25	2.32		
			2.86	2.93	3.02		
			4.46	4.55	4.67		
V <sub>hys</sub>	Hysteresis at VSENSEn input	V <sub>IT-</sub> = 1.68 V	15			mV	
		V <sub>IT-</sub> = 2.25 V	20				
		V <sub>IT-</sub> = 2.93 V	30				
		V <sub>IT-</sub> = 4.55 V	40				
I <sub>H(AV)</sub>	Average high-level input current	WDI	WDI = V <sub>DD</sub> = 6 V Time average (dc = 88%)		100	150	μA
I <sub>L(AV)</sub>	Average low-level input current		WDI = 0 V, V <sub>DD</sub> = 6 V, Time average (dc = 12%)		-15	-20	
I <sub>H</sub>	High-level input current	WDI	WDI = V <sub>DD</sub> = 6 V,		120	170	μA
		$\overline{\text{MR}}$	$\overline{\text{MR}} = 0.7 \times V_{DD}$ , V <sub>DD</sub> = 6 V		-130	-180	
		SENSE1	VSENSE1 = V <sub>DD</sub> = 6 V		5	8	
		SENSE2	VSENSE2 = V <sub>DD</sub> = 6 V		6	9	
I <sub>L</sub>	Low-level input current	WDI	WDI = 0 V, V <sub>DD</sub> = 6 V		-120	-170	μA
		$\overline{\text{MR}}$	$\overline{\text{MR}} = 0V$ , V <sub>DD</sub> = 6 V		-430	-600	
		SENSEn	VSENSE1,2 = 0 V		-1	1	
I <sub>DD</sub>	Supply current		40			μA	
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = 0 V to V <sub>DD</sub>	10			pF	

NOTES: 2. The lowest supply voltage at which RESET becomes active. t<sub>r</sub>, V<sub>DD</sub> ≥ 15 μs/V.  
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

# TPS3305-18, TPS3305-25, TPS3305-33 DUAL PROCESSOR SUPERVISORS

SLVS198 – DECEMBER 1998

## timing requirements at $V_{DD} = 2.7\text{ V to }6\text{ V}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 50\text{ pF}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_w$	Pulse width					
	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2\text{ V}$ , $V_{SENSEnH} = V_{IT+} + 0.2\text{ V}$	6			$\mu\text{s}$
	$\overline{\text{MR}}$	$V_{IH} = 0.7 \times V_{DD}$ , $V_{IL} = 0.3 \times V_{DD}$	100			ns
WDI	100				ns	

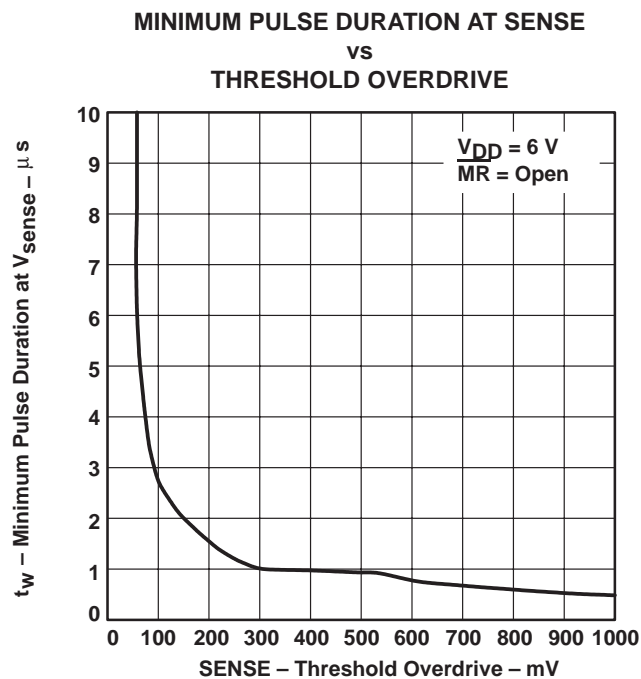
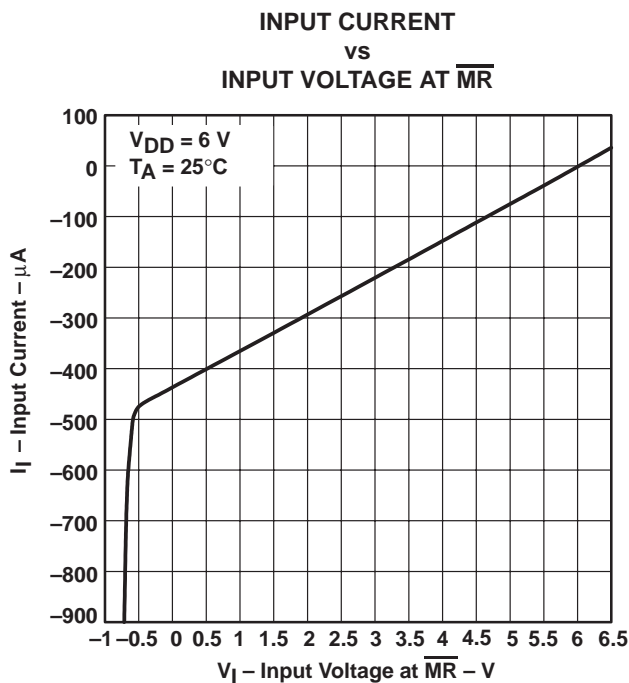
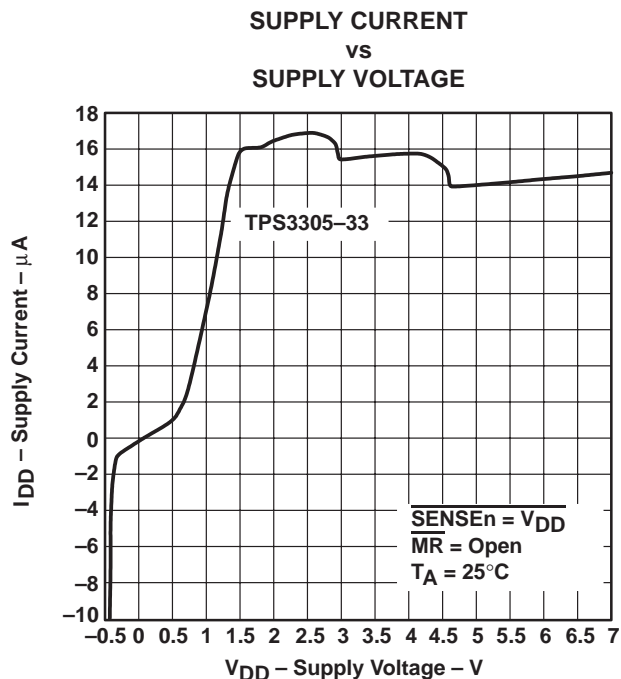
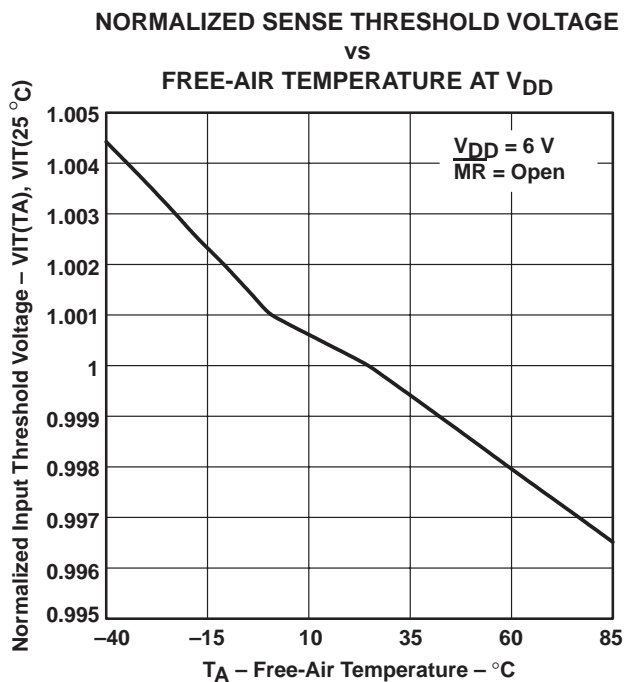
## switching characteristics at $V_{DD} = 2.7\text{ V to }6\text{ V}$ , $R_L = 1\text{ M}\Omega$ , $C_L = 50\text{ pF}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out	$V_{I(SENSEn)} \geq V_{IT+} + 0.2\text{ V}$ , $\overline{\text{MR}} \geq 0.7 \times V_{DD}$ , See timing diagram	1.1	1.6	2.3	s
$t_d$	Delay time	$V_{I(SENSEn)} \geq V_{IT+} + 0.2\text{ V}$ , $\overline{\text{MR}} \geq 0.7 \times V_{DD}$ , See timing diagram	140	200	280	ms
$t_{PHL}$	Propagation (delay) time, high-to-low level output	$\overline{\text{MR}}$ to RESET, $\overline{\text{MR}}$ to RESET		200	500	ns
$t_{PLH}$	Propagation (delay) time, low-to-high level output	$\overline{\text{MR}}$ to RESET, $\overline{\text{MR}}$ to RESET				
$t_{PHL}$	Propagation (delay) time, high-to-low level output	SENSEn to RESET, SENSEn to RESET		1	5	$\mu\text{s}$
$t_{PLH}$	Propagation (delay) time, low-to-high level output	SENSEn to RESET, SENSEn to RESET				





TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

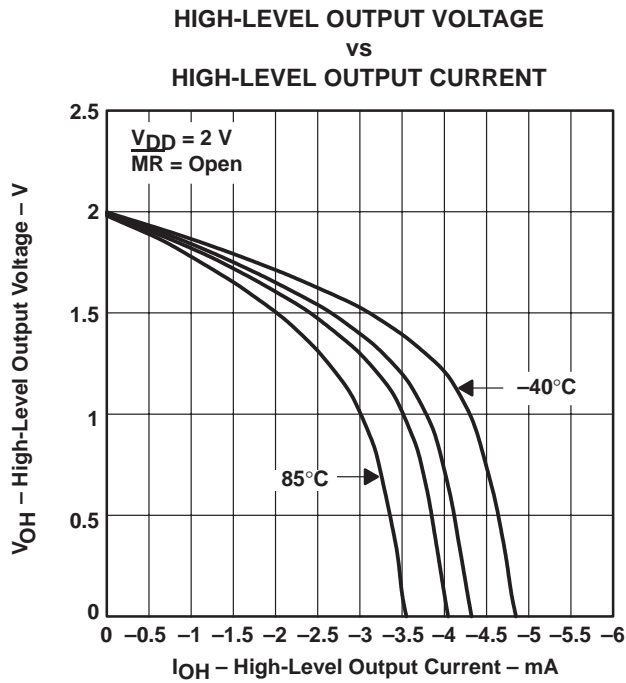


Figure 6

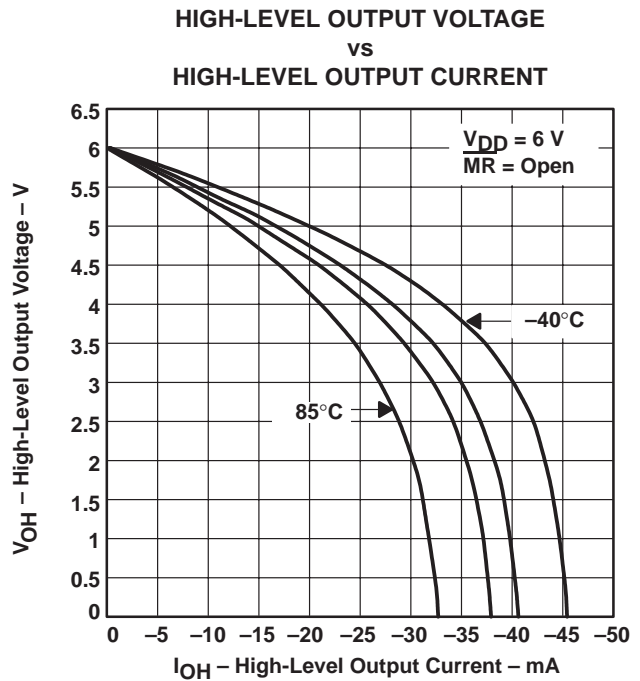


Figure 7

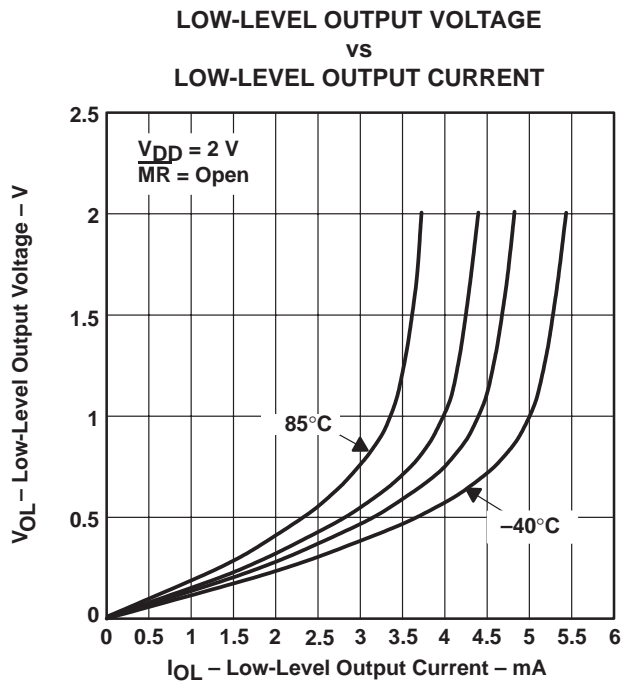


Figure 8

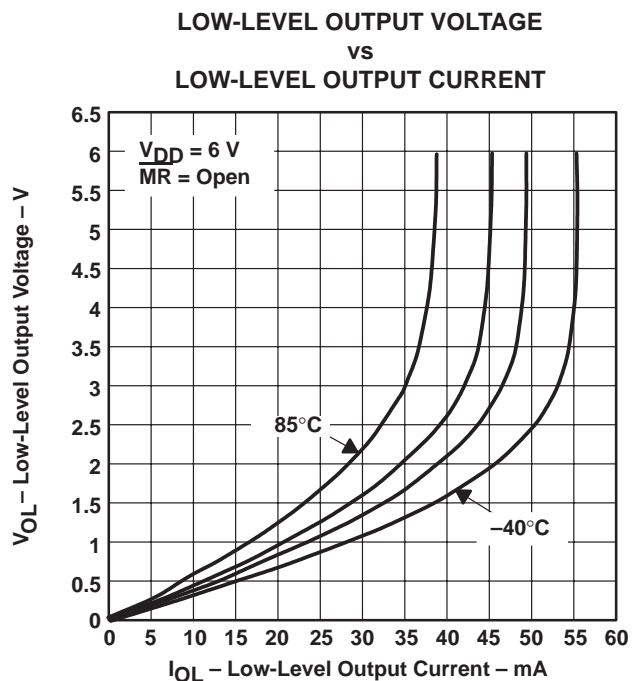


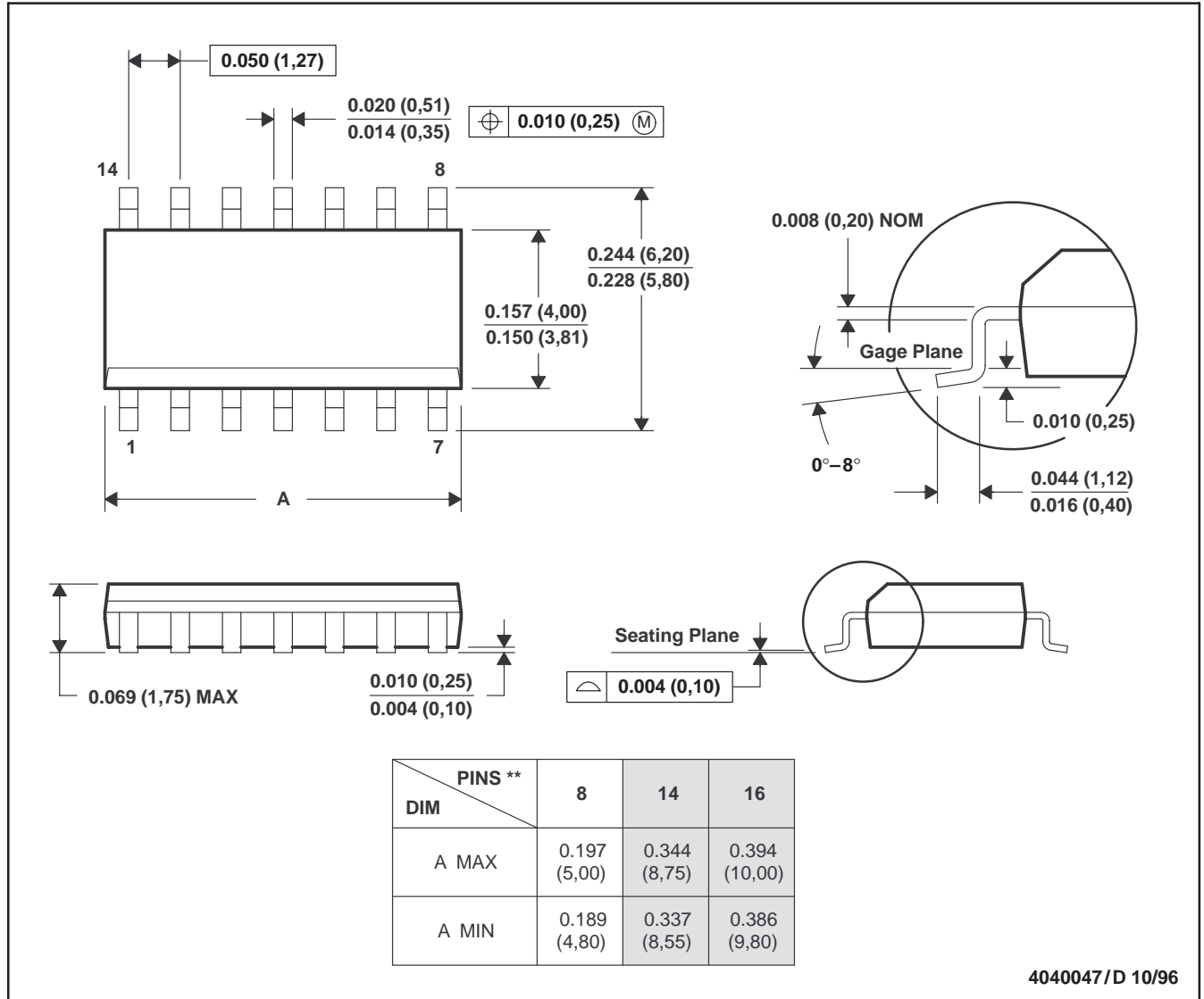
Figure 9

MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

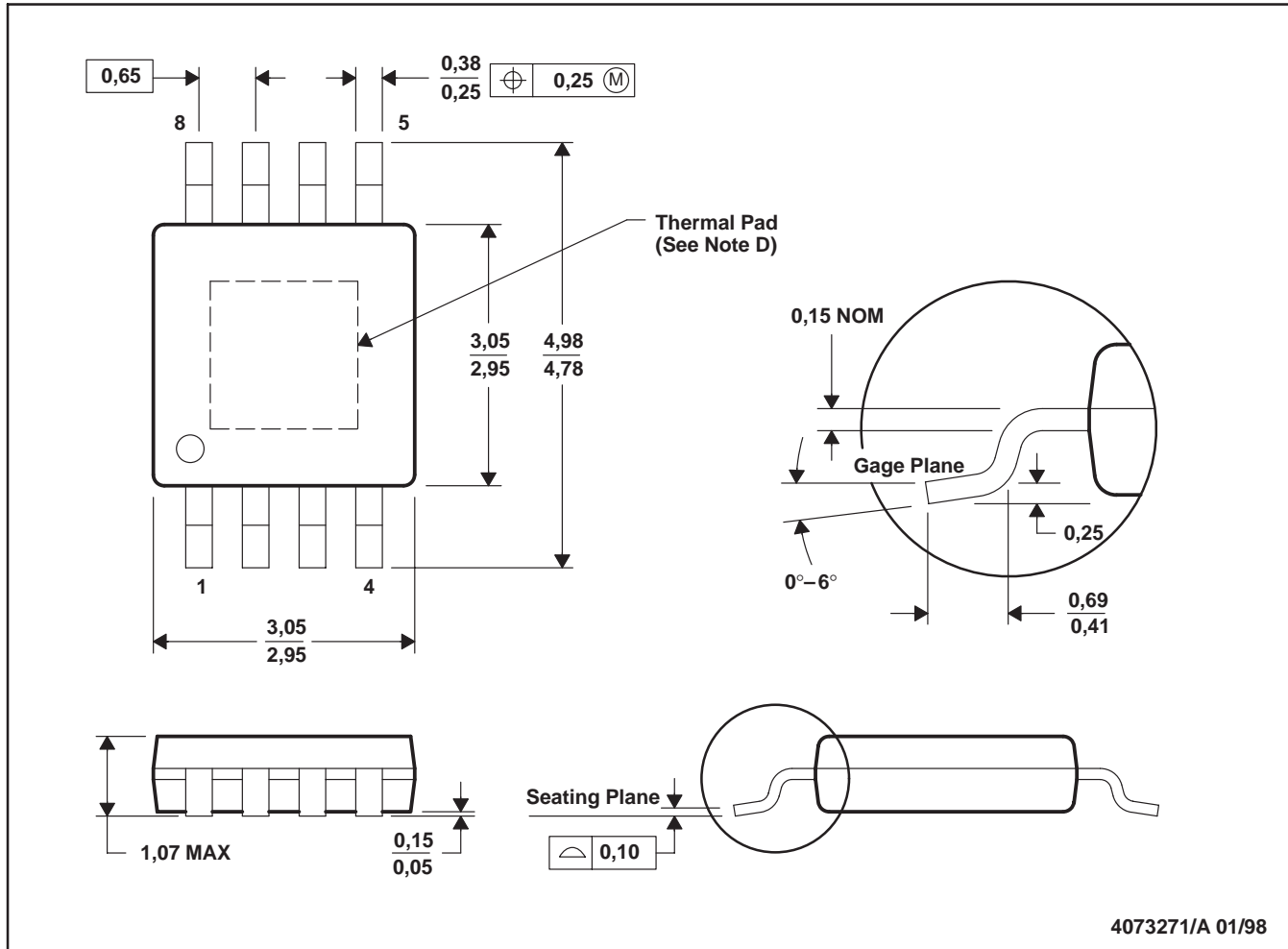
# TPS3305-18, TPS3305-25, TPS3305-33 DUAL PROCESSOR SUPERVISORS

SLVS198 – DECEMBER 1998

## MECHANICAL DATA

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions include mold flash or protrusions.  
 D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.  
 E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.