

TLV5624

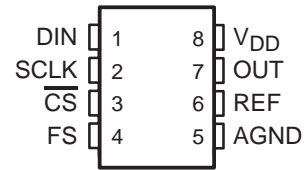
2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

features

- 8-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
1 μ s in Fast Mode,
3.5 μ s in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity . . . <0.2 LSB Typ
- Monotonic Over Temperature

D OR DGK PACKAGE
(TOP VIEW)



applications

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

description

The TLV5624 is a 8-bit voltage output DAC with a flexible 4-wire serial interface. The serial interface allows glueless interface to TMS320 and SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 8 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The programmable settling time of the DAC allows the designer to optimize speed vs power dissipation. With its on-chip programmable precision voltage reference, the TLV5624 simplifies overall system design.

Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC and 8-pin MSOP package to reduce board space in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

| T_A | PACKAGE | |
|---------------|-------------|---------------|
| | SOIC (D) | MSOP (DGK) |
| 0°C to 70°C | TLV5624CD | TLV5624CDGK |
| –40°C to 85°C | TLV5624ID | TLV5624IDGK |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



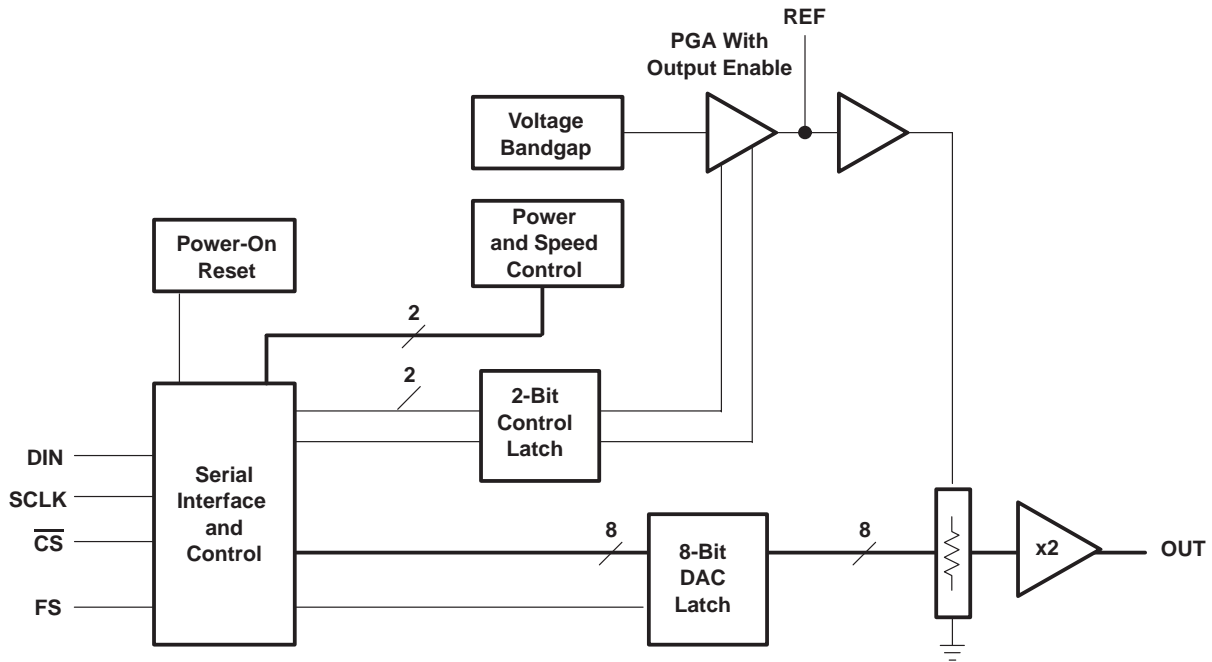
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

TLV5624
2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG
CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

functional block diagram



Terminal Functions

| TERMINAL NAME | NO. | I/O/P | DESCRIPTION |
|-----------------|-----|-------|--|
| AGND | 5 | P | Ground |
| \overline{CS} | 3 | I | Chip select. Digital input active low, used to enable/disable inputs |
| DIN | 1 | I | Digital serial data input |
| FS | 4 | I | Frame sync input |
| OUT | 7 | O | DAC A analog voltage output |
| REF | 6 | I/O | Analog reference voltage input/output |
| SCLK | 2 | I | Digital serial clock input |
| VDD | 8 | P | Positive power supply |

TLV5624

2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|-----------------------------|
| Supply voltage (V_{DD} to AGND) | 7 V |
| Reference input voltage range | – 0.3 V to $V_{DD} + 0.3$ V |
| Digital input voltage range | – 0.3 V to $V_{DD} + 0.3$ V |
| Operating free-air temperature range, T_A : TLV5624C | 0°C to 70°C |
| TLV5624I | –40°C to 85°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|--|-----------------------------|------|-------|----------------|------------|
| Supply voltage, V_{DD} | $V_{DD} = 5$ V | 4.5 | 5 | 5.5 | V |
| | $V_{DD} = 3$ V | 2.7 | 3 | 3.3 | V |
| Power on reset, POR | | 0.55 | | 2 | V |
| High-level digital input voltage, V_{IH} | $V_{DD} = 2.7$ V to 5.5 V | 2 | | | V |
| Low-level digital input voltage, V_{IL} | $V_{DD} = 2.7$ V to 5.5 V | | | 0.8 | V |
| Reference voltage, V_{ref} to REF terminal | $V_{DD} = 5$ V (see Note 1) | AGND | 2.048 | $V_{DD} - 1.5$ | V |
| Reference voltage, V_{ref} to REF terminal | $V_{DD} = 3$ V (see Note 1) | AGND | 1.024 | $V_{DD} - 1.5$ | V |
| Load resistance, R_L | | 2 | | | k Ω |
| Load capacitance, C_L | | | | 100 | pF |
| Clock frequency, f_{CLK} | | | | 20 | MHz |
| Operating free-air temperature, T_A | TLV5624C | 0 | | 70 | °C |
| | TLV5624I | –40 | | 85 | |

NOTE 1: Due to the x2 output buffer, a reference input voltage $\geq (V_{DD} - 0.4$ V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.



2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)

power supply

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|------------------------------|---|------|------|-----|------|
| I _{DD} | Power supply current | No load, All inputs = AGND or V _{DD} , DAC latch = 0x800 | Fast | 2.3 | 3.3 | mA |
| | | | Slow | 1.5 | 1.9 | |
| Power down supply current | | See Figure 8 | | 0.01 | 10 | μA |
| PSRR | Power supply rejection ratio | Zero scale, See Note 2 | | -65 | | dB |
| | | Full scale, See Note 3 | | -65 | | |

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by:

$$PSRR = 20 \log [(E_{ZS}(V_{DDmax}) - E_{ZS}(V_{DDmin})) / V_{DDmax}]$$

3. Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by:

$$PSRR = 20 \log [(E_G(V_{DDmax}) - E_G(V_{DDmin})) / V_{DDmax}]$$

static DAC specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|-----------------|-----|-------|------|----------------|
| Resolution | | | 8 | | | bits |
| INL | Integral nonlinearity, end point adjusted | See Note 4 | | ±0.3 | ±0.5 | LSB |
| DNL | Differential nonlinearity | See Note 5 | | ±0.07 | ±0.2 | LSB |
| E _{ZS} | Zero-scale error (offset error at zero scale) | See Note 6 | | | ±10 | mV |
| E _{ZS} TC | Zero-scale-error temperature coefficient | See Note 7 | | 10 | | ppm/°C |
| E _G | Gain error | See Note 8 | | | ±0.6 | % full scale V |
| E _G TC | Gain error temperature coefficient | See Note 9 | | 10 | | ppm/°C |

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.

7. Zero-scale-error temperature coefficient is given by: $E_{ZS} TC = [E_{ZS}(T_{max}) - E_{ZS}(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.

8. Gain error is the deviation from the ideal output ($2V_{ref} - 1$ LSB) with an output load of 10 kΩ excluding the effects of the zero-error.

9. Gain temperature coefficient is given by: $E_G TC = [E_G(T_{max}) - E_G(T_{min})] / V_{ref} \times 10^6 / (T_{max} - T_{min})$.

output specifications

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|----------------|---|-----|-------|----------------------|----------------|
| V _O | Output voltage | R _L = 10 kΩ | 0 | | V _{DD} -0.4 | V |
| Output load regulation accuracy | | V _O = 4.096 V, 2.048 V R _L = 2 kΩ | | ±0.10 | ±0.25 | % full scale V |

reference pin configured as output (REF)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|------------------------------|--------------------------|-------|-------|-------|------|
| V _{ref} (OUTL) | Low reference voltage | | 1.003 | 1.024 | 1.045 | V |
| V _{ref} (OUTH) | High reference voltage | V _{DD} > 4.75 V | 2.027 | 2.048 | 2.069 | V |
| I _{ref} (source) | Output source current | | | | 1 | mA |
| I _{ref} (sink) | Output sink current | | -1 | | | mA |
| Load capacitance | | | | | 100 | pF |
| PSRR | Power supply rejection ratio | | | -65 | | dB |

TLV5624
2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG
CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

electrical characteristics over recommended operating conditions (unless otherwise noted)
(Continued)

reference pin configured as input (REF)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|------|----------------------|-----|------|
| V _I Input voltage | | 0 | V _{DD} -1.5 | | V |
| R _I Input resistance | | | 10 | | MΩ |
| C _I Input capacitance | | | 5 | | pF |
| Reference input bandwidth | REF = 0.2 V _{pp} + 1.024 V dc | Fast | 1.3 | | MHz |
| | | Slow | 525 | | kHz |
| Reference feedthrough | REF = 1 V _{pp} at 1 kHz + 1.024 V dc (see Note 10) | | -80 | | dB |

NOTE 10: Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------------|-----|-----|-----|------|
| I _{IH} High-level digital input current | V _I = V _{DD} | | | 1 | μA |
| I _{IL} Low-level digital input current | V _I = 0 V | -1 | | | μA |
| C _i Input capacitance | | | 8 | | pF |

analog output dynamic performance

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|------|-----|-----|------|
| t _s (FS) Output settling time, full scale | R _L = 10 kΩ, C _L = 100 pF, See Note 11 | Fast | 1 | 3 | μs |
| | | Slow | 3.5 | 7 | |
| t _s (CC) Output settling time, code to code | R _L = 10 kΩ, C _L = 100 pF, See Note 12 | Fast | 0.5 | 1.5 | μs |
| | | Slow | 1 | 2 | |
| SR Slew rate | R _L = 10 kΩ, C _L = 100 pF, See Note 13 | Fast | 8 | | V/μs |
| | | Slow | 1.5 | | |
| Glitch energy | D _{IN} = 0 to 1, f _{CLK} = 100 kHz, CS = V _{DD} | | 5 | | nV-S |
| SNR Signal-to-noise ratio | f _s = 480 kSPS, f _{out} = 1 kHz, R _L = 10 kΩ, C _L = 100 pF | | 53 | 57 | dB |
| S/(N+D) Signal-to-noise + distortion | | | 48 | 47 | |
| THD Total harmonic distortion | | | -50 | -48 | |
| Spurious free dynamic range | | | 50 | 62 | |

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively. Not tested, assured by design.

12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.

13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

TLV5624
2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG
CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

digital input timing requirements

| | | MIN | NOM | MAX | UNIT |
|------------------|---|-----|-----|-----|------|
| $t_{su}(CS-FS)$ | Setup time, \overline{CS} low before FS falling edge | 10 | | | ns |
| $t_{su}(FS-CK)$ | Setup time, FS low before first negative SCLK edge | 8 | | | ns |
| $t_{su}(C16-FS)$ | Setup time, 16 th negative SCLK edge after FS low on which bit D0 is sampled before rising edge of FS | 10 | | | ns |
| $t_{su}(C16-CS)$ | Setup time, 16 th positive SCLK edge (first positive after D0 is sampled) before \overline{CS} rising edge. If FS is used instead of 16 th positive edge to update DAC, then setup time between FS rising edge and \overline{CS} rising edge. | 10 | | | ns |
| t_{wH} | SCLK pulse duration high | 25 | | | ns |
| t_{wL} | SCLK pulse duration low | 25 | | | ns |
| $t_{su}(D)$ | Setup time, data ready before SCLK falling edge | 8 | | | ns |
| $t_{H}(D)$ | Hold time, data held valid after SCLK falling edge | 5 | | | ns |
| $t_{wH}(FS)$ | FS pulse duration high | 25 | | | ns |

PARAMETER MEASUREMENT INFORMATION

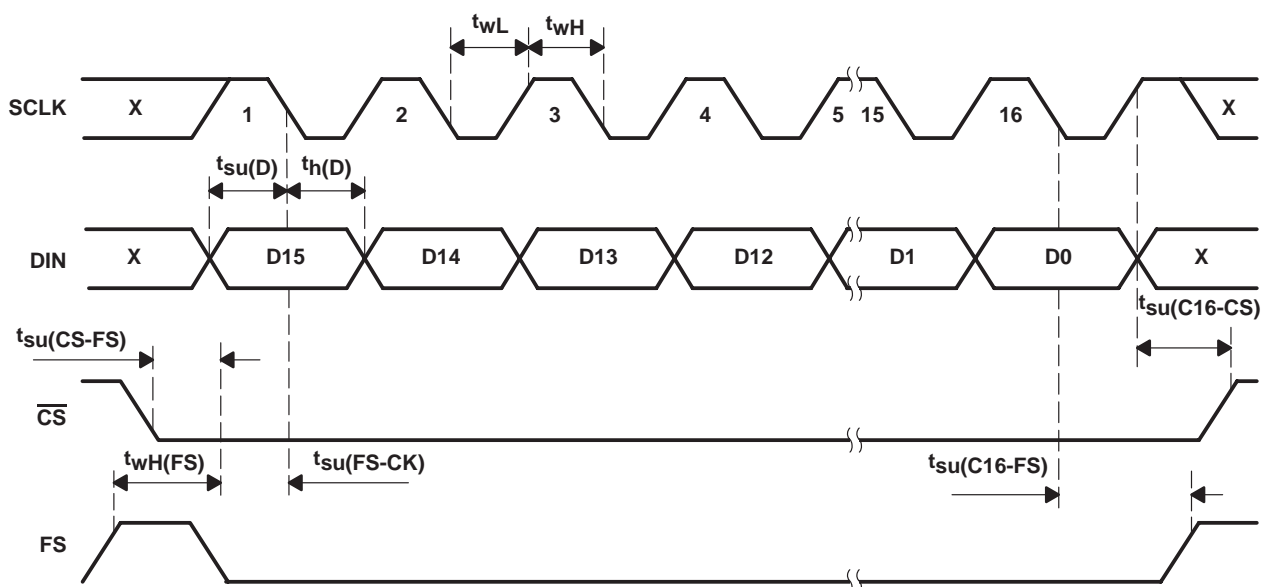


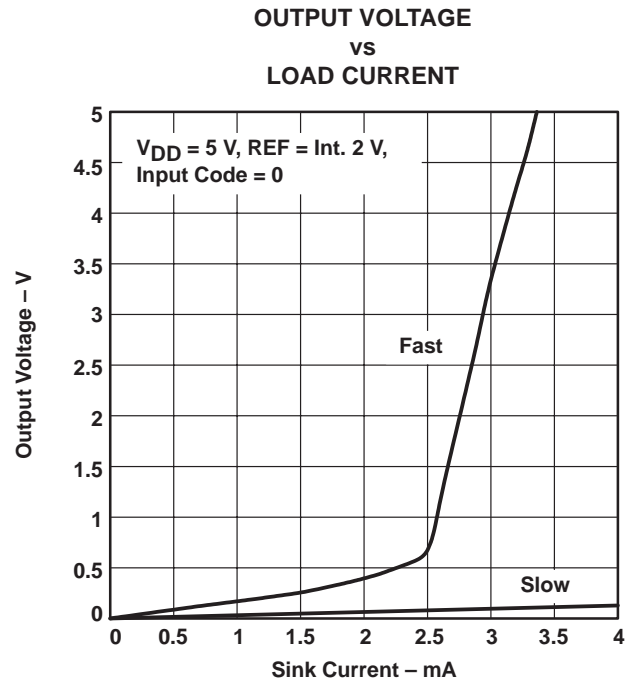
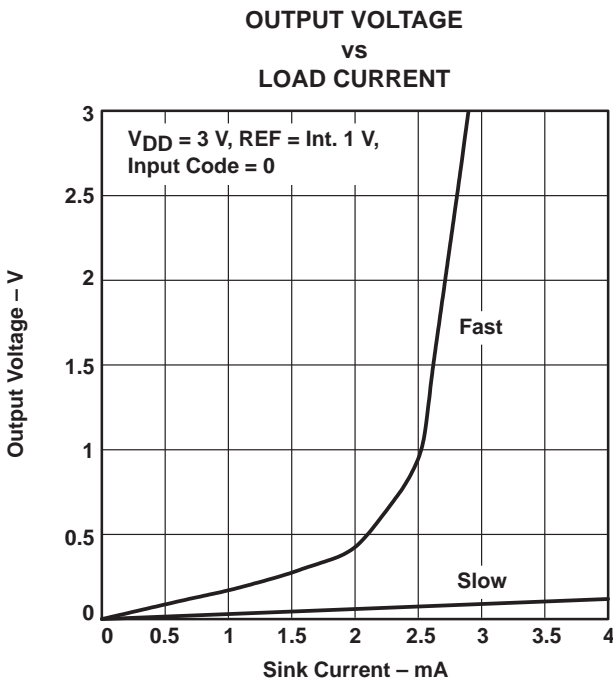
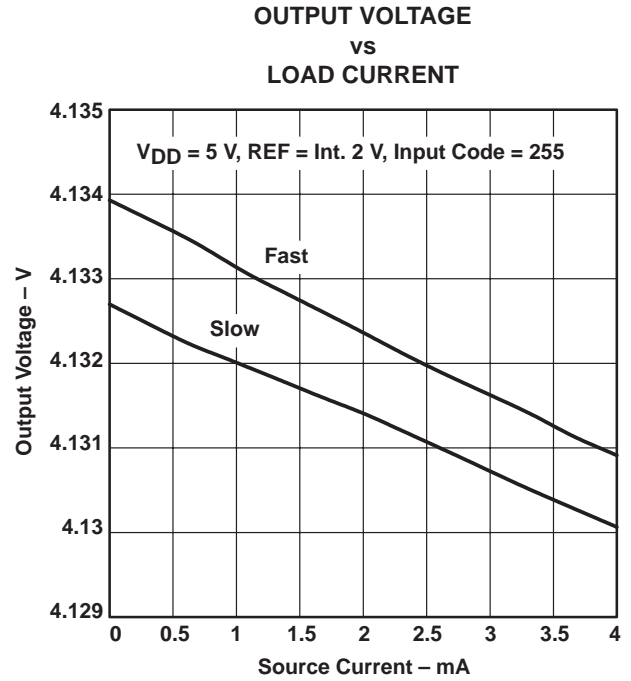
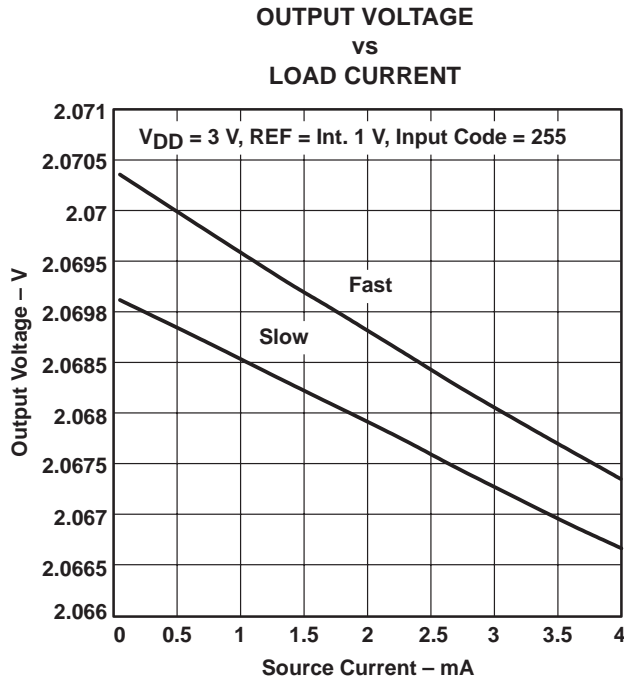
Figure 1. Timing Diagram



TLV5624 2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

SUPPLY CURRENT
 VS
 TEMPERATURE

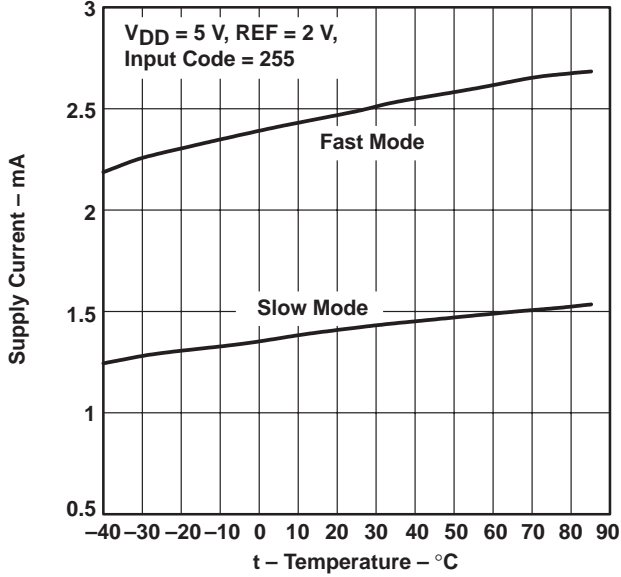


Figure 6

SUPPLY CURRENT
 VS
 TEMPERATURE

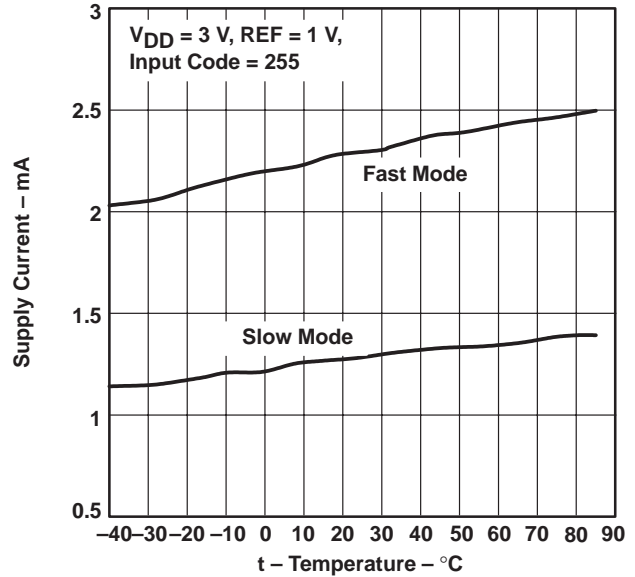


Figure 7

POWER DOWN SUPPLY CURRENT
 VS
 TIME

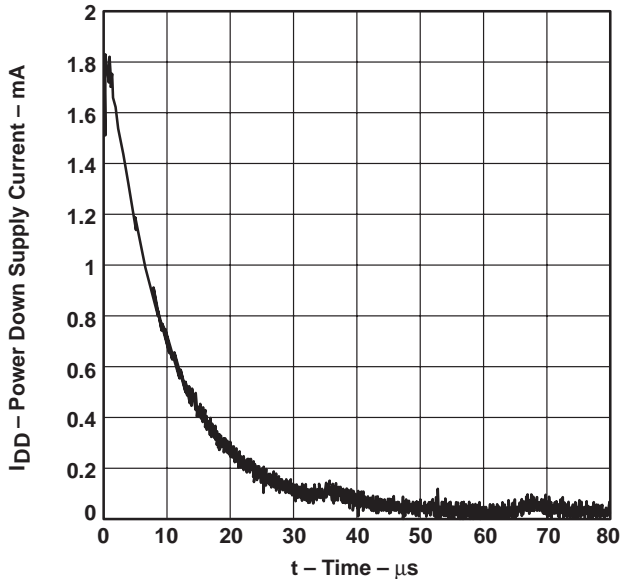


Figure 8

TOTAL HARMONIC DISTORTION AND NOISE
 VS
 FREQUENCY

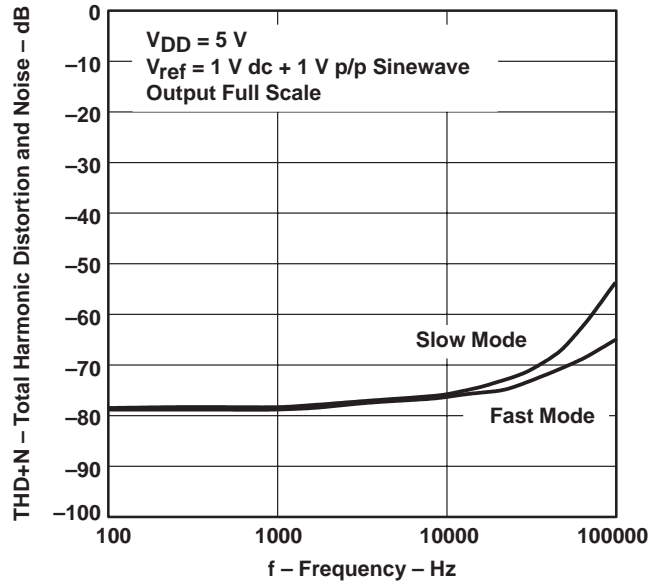


Figure 9

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
 VS
 FREQUENCY

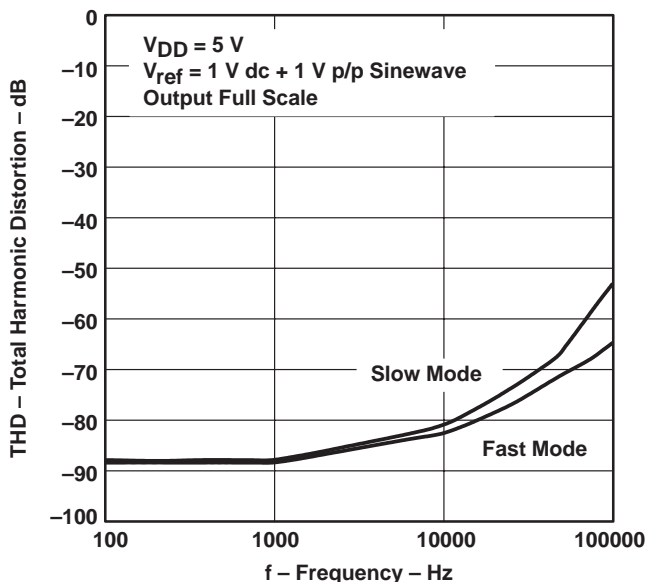


Figure 10

DIFFERENTIAL NONLINEARITY
 VS
 DIGITAL OUTPUT CODE

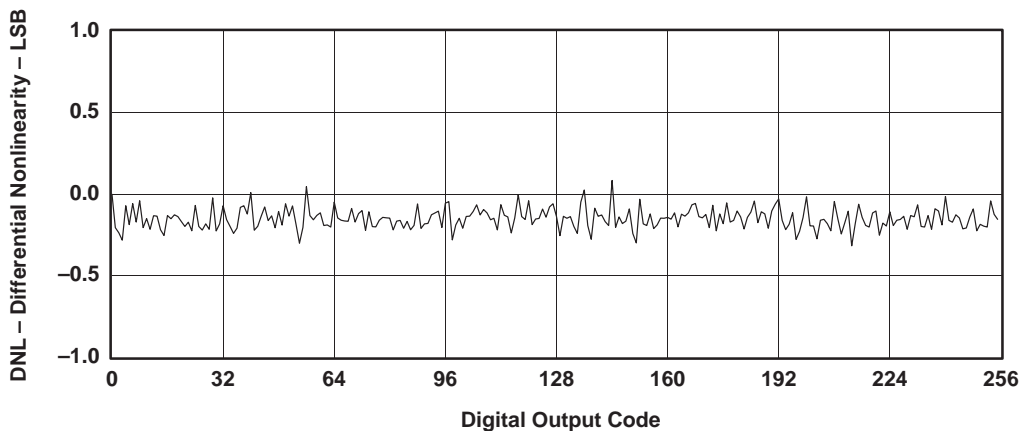


Figure 11

TLV5624

2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

TYPICAL CHARACTERISTICS

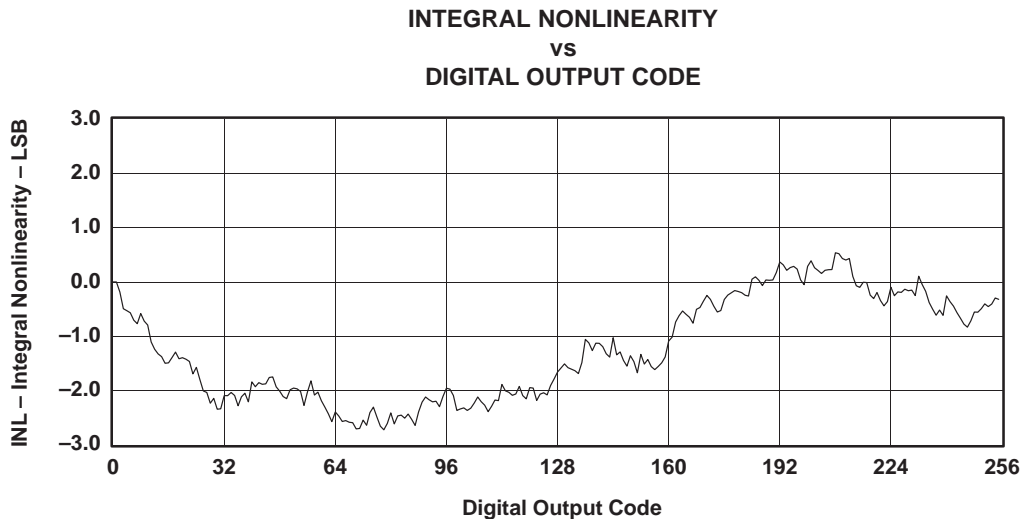


Figure 12

APPLICATION INFORMATION

general function

The TLV5624 is an 8-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2 \text{ REF} \frac{\text{CODE}}{0x1000} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFF0. Bits 3 to 0 must be set to 0. A power on reset initially puts the internal latches to a defined state (all bits zero).

serial interface

The device has to be enabled with $\overline{\text{CS}}$ set to low. A falling edge of FS starts shifting the data bit-per-bit (starting with the MSB) to the internal register on high-low transitions of SCLK. After 16 bits have been transferred or FS rises, the content of the shift register is moved to the DAC latch, which updates the voltage output to the new level.

The serial interface of the TLV5624 can be used in two basic modes:

- Four wire (with chip select)
- Three wire (without chip select)

Using chip select (four-wire mode), it is possible to have more than one device connected to the serial port of the data source (DSP or microcontroller). Figure 13 shows an example with two TLV5624s connected directly to a TMS320 DSP.

APPLICATION INFORMATION

serial interface (continued)

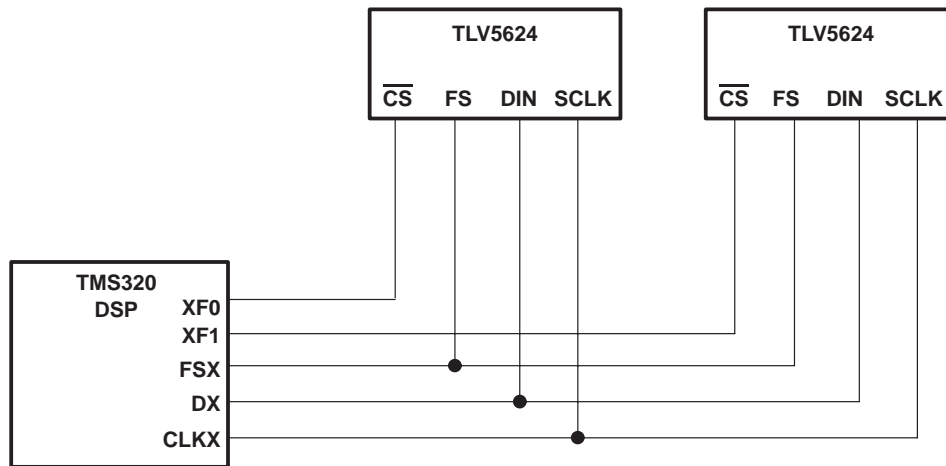


Figure 13. TMS320 Interface

If there is no need to have more than one device on the serial bus, then \overline{CS} can be tied low. Figure 14 shows an example of how to connect the TLV5624 to TMS320, SPI™ or Microwire™ using only three pins.

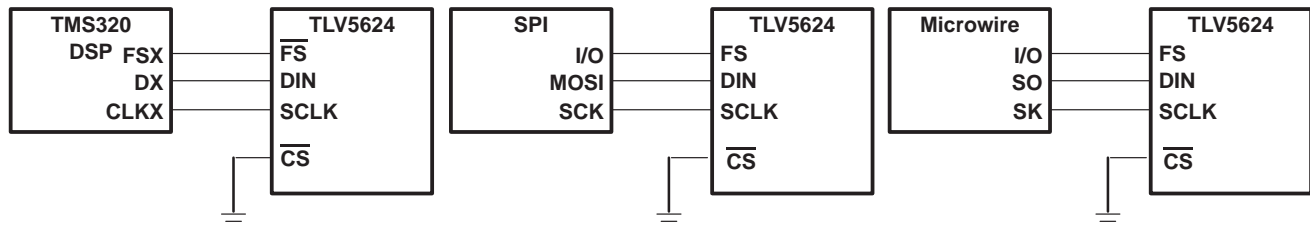


Figure 14. Three-Wire Interface

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to FS. If the word width is 8 bits (SPI™ and Microwire™), two write operations must be performed to program the TLV5624. After the write operation(s), the DAC output is updated automatically on the 16th positive clock edge.

serial clock frequency and update rate

The maximum serial clock frequency is given by:

$$f_{\text{sclkmax}} = \frac{1}{t_{\text{whmin}} + t_{\text{wlmin}}} = 20 \text{ MHz}$$

The maximum update rate is:

$$f_{\text{updatemax}} = \frac{1}{16 (t_{\text{whmin}} + t_{\text{wlmin}})} = 1.25 \text{ MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5624 has to be considered, too.

TLV5624

2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

SLAS235 – JULY 1999

APPLICATION INFORMATION

data format

The 16-bit data word for the TLV5624 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

| | | | | | | | | | | | | | | | |
|-----|-----|-----|-----|--------------|-----|----|----|----|----|----|----|----|----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R1 | SPD | PWR | R0 | 12 Data bits | | | | | | | | | | | |

SPD: Speed control bit 1 → fast mode 0 → slow mode
PWR: Power control bit 1 → power down 0 → normal operation

The following table lists the possible combination of the register select bits:

register select bits

| R1 | R0 | REGISTER |
|----|----|--------------------------------|
| 0 | 0 | Write data to DAC |
| 0 | 1 | Reserved |
| 1 | 0 | Reserved |
| 1 | 1 | Write data to control register |

The meaning of the 12 data bits depends on the selected register. For the DAC register, bits D11...D4 determine the new DAC output value:

data bits: DAC

| | | | | | | | | | | | |
|---------------|-----|----|----|----|----|----|----|----|----|----|----|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| New DAC Value | | | | | | | | 0 | 0 | 0 | 0 |

If the control register is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

data bits: CONTROL

| | | | | | | | | | | | |
|-----|-----|----|----|----|----|----|----|----|----|------|------|
| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| X | X | X | X | X | X | X | X | X | X | REF1 | REF2 |

X: don't care

REF1 and REF0 determine the reference source and, if internal reference is selected, the reference voltage.

reference bits

| REF1 | REF0 | REFERENCE |
|------|------|-----------|
| 0 | 0 | External |
| 0 | 1 | 1.024 V |
| 1 | 0 | 2.048 V |
| 1 | 1 | External |

CAUTION:

If external reference voltage is applied to the REF pin, external reference MUST be selected.



APPLICATION INFORMATION

Example:

- Set DAC output, select fast mode, select internal reference at 2.048 V:

1. Set reference voltage to 2.048 V (CONTROL register):

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

2. Write new DAC value and update DAC output:

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|-----|-----|----------------------|-----|----|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | New DAC output value | | | | | | | | 0 | 0 | 0 | 0 |

The DAC output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

linearity, offset, and gain error using single ended supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 15.

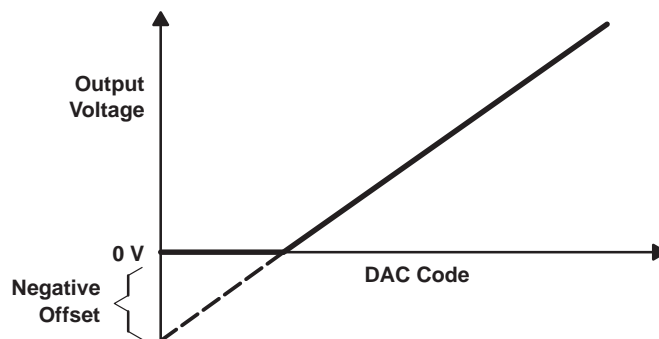


Figure 15. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed-circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane, making sure that analog ground currents are well managed and there are negligible voltage drops across the ground plane.

A 0.1- μF ceramic-capacitor bypass should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog supply from the digital power supply.

Figure 16 shows the ground plane layout and bypassing technique.

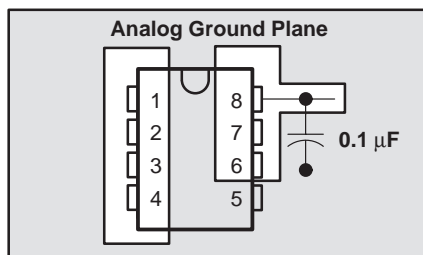


Figure 16. Power-Supply Bypassing

definitions of specifications and terminology**integral nonlinearity (INL)**

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_{G})

Gain error is the error in slope of the DAC transfer function.

total harmonic distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

TLV5624
**2.7 V TO 5.5 V LOW POWER 8-BIT DIGITAL-TO-ANALOG
 CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN**

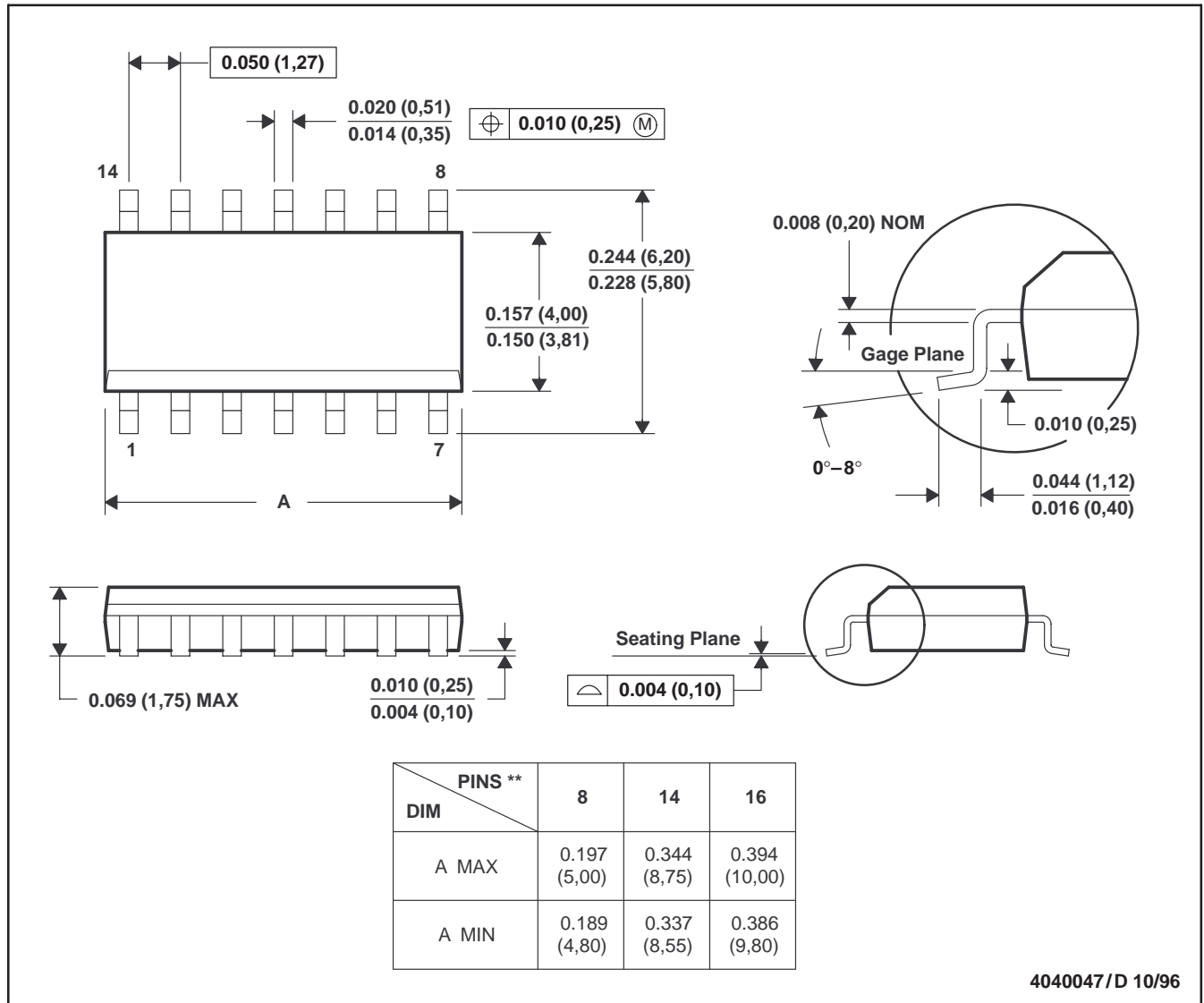
SLAS235 – JULY 1999

MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

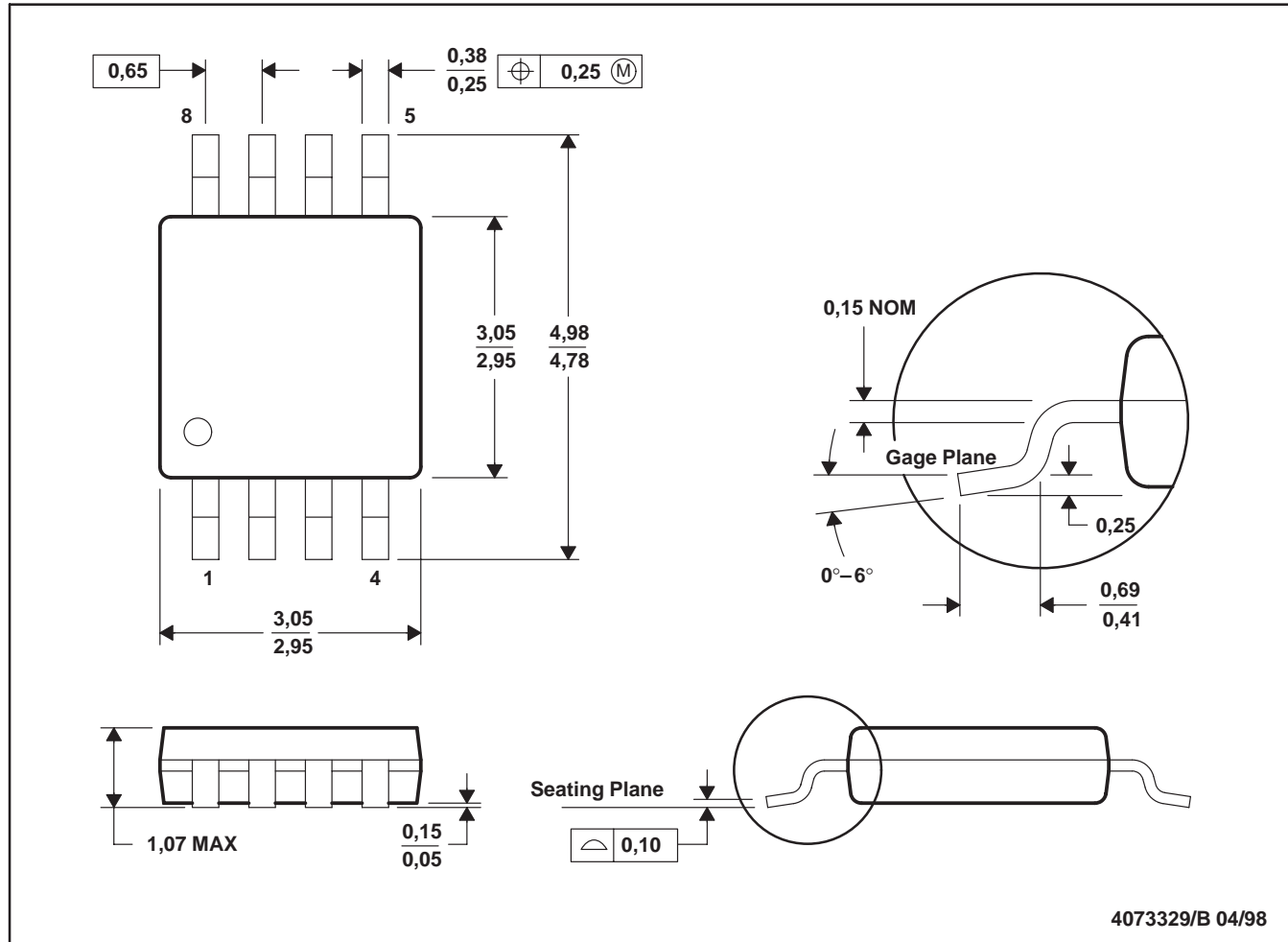


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/B 04/98

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-187

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.