TMP100
TMP101

SBOS231C – JANUARY 2002 – REVISED JULY 2003

Digital Temperature Sensor with I²C Interface

FEATURES

- **DIGITAL OUTPUT: I²C Serial 2-Wire**
- **RESOLUTION: 9- to 12-Bits, User-Selectable**
- **ACCURACY: ±2.0°C from –25°C to +85°C (max)**
  ±3.0°C from –55°C to +125°C (max)
- **LOW QUIESCENT CURRENT: 45μA, 0.1μA Standby**
- **WIDE SUPPLY RANGE: 2.7V to 5.5V**
- **TINY SOT23-6 PACKAGE**

APPLICATIONS

- **POWER-SUPPLY TEMPERATURE MONITORING**
- **COMPUTER PERIPHERAL THERMAL PROTECTION**
- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **BATTERY MANAGEMENT**
- **OFFICE MACHINES**
- **THERMOSTAT CONTROLS**
- **ENVIRONMENTAL MONITORING and HVAC**
- **ELECTROMECHANICAL DEVICE TEMPERATURE**

DESCRIPTION

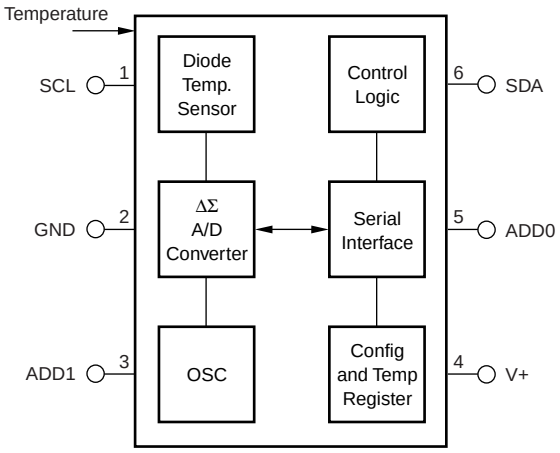
The TMP100 and TMP101 are 2-wire, serial output temperature sensors available in SOT23-6 packages. Requiring no external components, the TMP100 and TMP101 are capable of reading temperatures with a resolution of 0.0625°C.

The TMP100 and TMP101 feature SMBus and I²C™ interface compatibility, with the TMP100 allowing up to eight devices on one bus. The TMP101 offers SMBus alert function with up to three devices per bus.

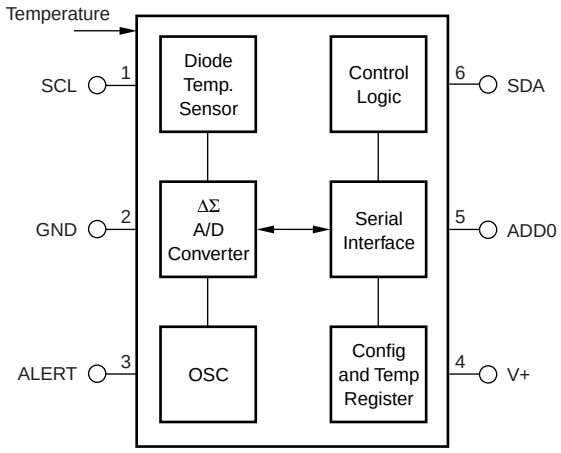
The TMP100 and TMP101 are ideal for extended temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP100 and TMP101 are specified for operation over a temperature range of –55°C to +125°C.

I²C is a registered trademark of Philips Incorporated.



TMP100



TMP101

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply, V+	7.5V
Input Voltage[2]	–0.5V to 7.5V
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–60°C to +150°C
Junction Temperature (T_J Max)	+150°C
Lead Temperature (soldering)	+300°C

NOTES: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability. (2) Input voltage rating applies to all TMP100 and TMP101 input voltages.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

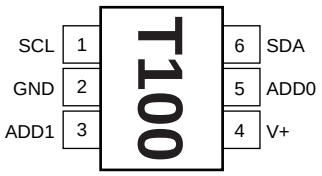
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TMP100	SOT23-6	DBV	–55°C to +125°C	T100	TMP100NA/250	Tape and Reel, 250
"	"	"	"	"	TMP100NA/3K	Tape and Reel, 3000
TMP101	SOT23-6	DBV	–55°C to +125°C	T101	TMP101NA/250	Tape and Reel, 250
"	"	"	"	"	TMP101NA/3K	Tape and Reel, 3000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

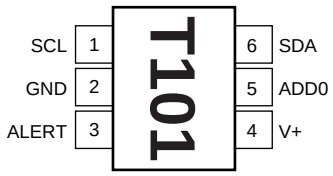
PIN CONFIGURATIONS

Top View **SOT23**



TMP100

Top View **SOT23**



TMP101

ELECTRICAL CHARACTERISTICS

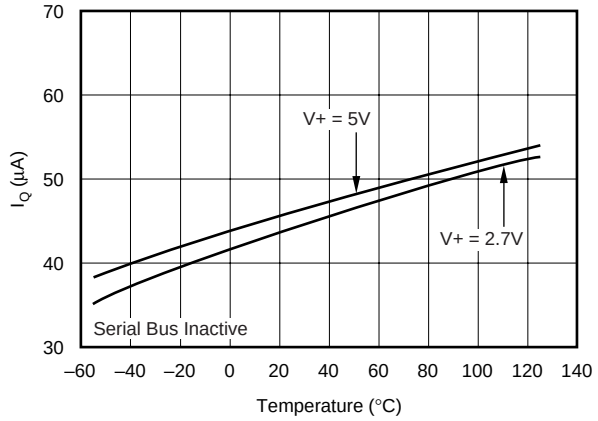
At T_A = –55°C to +125°C, and V+ = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		CONDITION	TMP100, TMP101 MIN	TYP	MAX	UNITS
TEMPERATURE INPUT						
Range			–55		+125	°C
Accuracy (Temperature Error)		–25°C to +85°C		±0.5	±2.0	°C
		–55°C to +125°C		±1.0	±3.0	°C
Resolution		Selectable		±0.0625		°C
DIGITAL INPUT/OUTPUT						
Input Logic Levels:						
V_{IH}			0.7(V+)		6.0	V
V_{IL}			–0.5		0.3(V+)	V
Input Current, I_{IN}		0V ≤ V_{IN} ≤ 6V			1	µA
Output Logic Levels:						
V_{OL} SDA		I_{OL} = 3mA	0	0.15	0.4	V
V_{OL} ALERT		I_{OL} = 4mA	0	0.15	0.4	V
Resolution		Selectable		9 to 12		Bits
Conversion Time		9-Bit		40	75	ms
		10-Bit		80	150	ms
		11-Bit		160	300	ms
		12-Bit		320	600	ms
Conversion Rate		9-Bit		25		s/s
		10-Bit		12		s/s
		11-Bit		6		s/s
		12-Bit		3		s/s
POWER SUPPLY						
Operating Range			2.7		5.5	V
Quiescent Current	I_Q	Serial Bus Inactive		45	75	µA
		Serial Bus Active, SCL Freq = 400kHz		70		µA
		Serial Bus Active, SCL Freq = 3.4MHz		150		µA
Shutdown Current	I_{SD}	Serial Bus Inactive		0.1	1	µA
		Serial Bus Active, SCL Freq = 400kHz		20		µA
		Serial Bus Active, SCL Freq = 3.4MHz		100		µA
TEMPERATURE RANGE						
Specified Range			–55		+125	°C
Storage Range			–60		+150	°C
Thermal Resistance, θ_{JA}		SOT23-6 Surface-Mount		150		°C/W

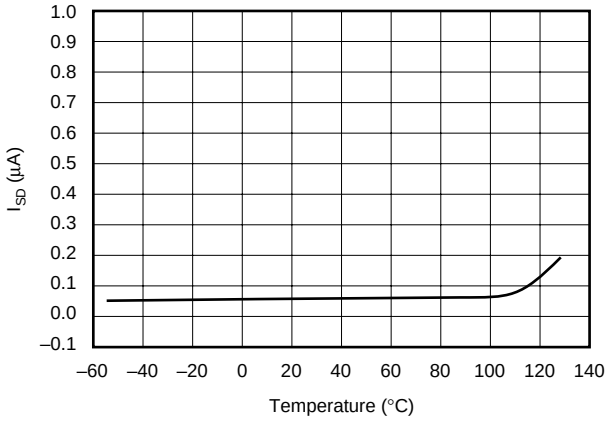
TYPICAL CHARACTERISTICS

At T_A = +25°C, V+ = 5.0V, unless otherwise noted.

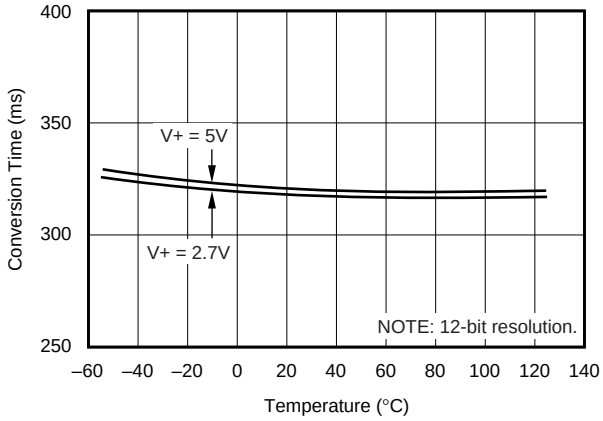
QUIESCENT CURRENT vs TEMPERATURE



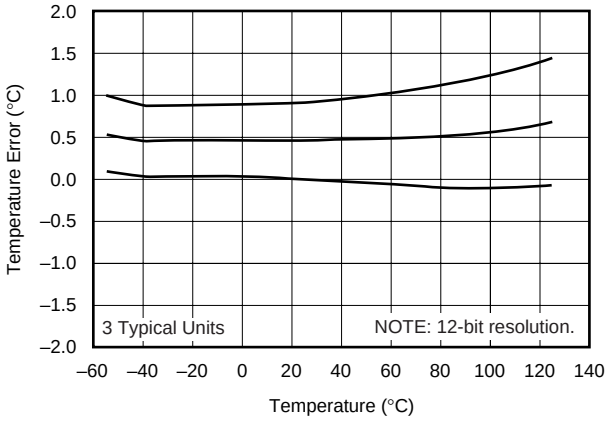
SHUTDOWN CURRENT vs TEMPERATURE



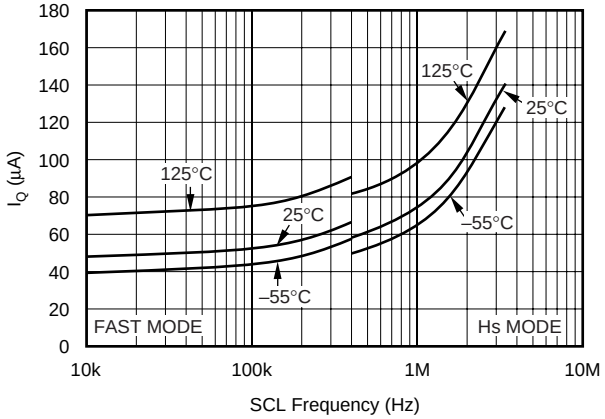
CONVERSION TIME vs TEMPERATURE



TEMPERATURE ACCURACY vs TEMPERATURE



QUIESCENT CURRENT WITH BUS ACTIVITY vs TEMPERATURE



APPLICATIONS INFORMATION

The TMP100 and TMP101 are digital temperature sensors optimal for thermal management and thermal protection applications. The TMP100 and TMP101 are I²C and SMBus interface compatible and are specified over a temperature range of –55°C to +125°C.

The TMP100 and TMP101 require no external components for operation except for pull-up resistors on SCL, SDA, and ALERT, although a 0.1µF bypass capacitor is recommended, as shown in Figure 1 and Figure 2.

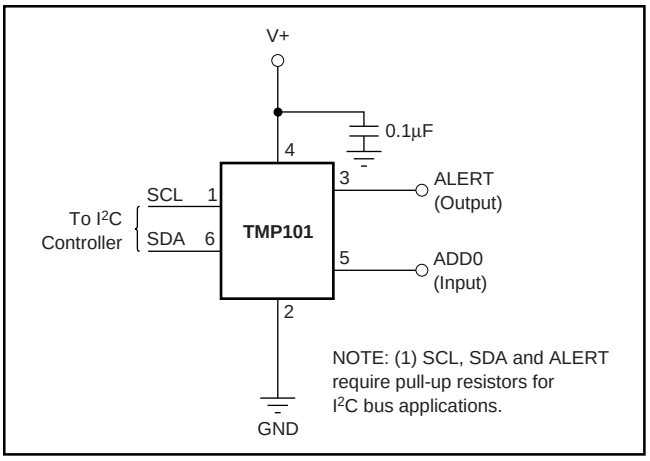


FIGURE 1. Typical Connections of the TMP101.

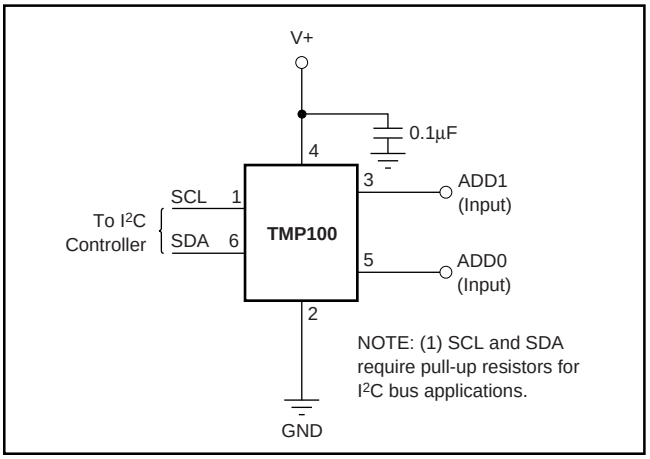


FIGURE 2. Typical Connections of the TMP100.

The die flag of the lead frame is connected to pin 2. The sensing device of the TMP100 and TMP101 is the chip itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path. The GND pin of the TMP100 or TMP101 is directly connected to the metal lead frame, and is the best choice for thermal input.

To maintain the accuracy in applications requiring air or surface temperature measurement, care should be taken to isolate the package and leads from ambient air temperature. A thermally conductive adhesive will assist in achieving accurate surface temperature measurement.

POINTER REGISTER

Figure 3 shows the internal register structure of the TMP100 and TMP101. The 8-bit Pointer Register of the TMP100 and TMP101 is used to address a given data register. The Pointer Register uses the two LSBs to identify which of the data registers should respond to a read or write command. Table I identifies the bits of the Pointer Register byte. Table II describes the pointer address of the registers available in the TMP100 and TMP101. Power-up Reset value of P1/P0 is 00.

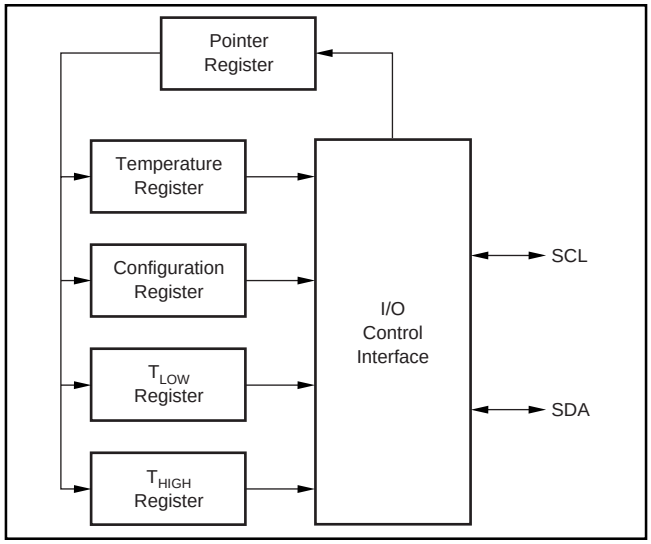


FIGURE 3. Internal Register Structure of TMP100 and TMP101.

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

TABLE I. Pointer Register Byte.

P1	P0	REGISTER
0	0	Temperature Register (READ Only)
0	1	Configuration Register (READ/WRITE)
1	0	T_{LOW} Register (READ/WRITE)
1	1	T_{HIGH} Register (READ/WRITE)

TABLE II. Pointer Addresses of the TMP100 and TMP101 Registers.

TEMPERATURE REGISTER

The Temperature Register of the TMP100 or TMP101 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data and are described in Table III and Table IV. The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is summarized in Table V. Following power-up or reset, the Temperature Register will read 0°C until the first conversion is complete.

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4

TABLE III. Byte 1 of Temperature Register.

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0

TABLE IV. Byte 2 of Temperature Register.

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0.0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90
–128	1000 0000 0000	800

TABLE V. Temperature Data Format.

The user can obtain 9, 10, 11, or 12 bits of resolution by addressing the Configuration Register and setting the resolution bits accordingly. For 9, 10, or 11 bit resolution, the most significant bits in the Temperature Register are used with the unused LSBs set to zero.

CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. The format of the Configuration Register for the TMP100 and TMP101 is shown in Table VI, followed by a breakdown of the register bits. The power-up/reset value of the Configuration Register is all bits equal to 0. The OS/ALERT bit will read as 1 after power-up/reset.

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	OS/ALERT	R1	R0	F1	F0	POL	TM	SD

TABLE VI. Configuration Register Format.

SHUTDOWN MODE (SD)

The Shutdown Mode of the TMP100 and TMP101 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to less than 1μA. For the TMP100 and TMP101, Shutdown Mode is enabled when the SD bit is 1. The device will shutdown once the current conversion is completed. For SD equal to 0, the device will maintain continuous conversion.

THERMOSTAT MODE (TM)

The Thermostat Mode bit of the TMP101 indicates to the device whether to operate in Comparator Mode (TM = 0) or Interrupt Mode (TM = 1). For more information on comparator and interrupt modes, see text “HIGH and LOW Limit Registers.”

POLARITY (POL)

The Polarity Bit of the TMP101 allows the user to adjust the polarity of the ALERT pin output. If POL = 0, the ALERT pin will be active LOW, as shown in Figure 4. For POL = 1 the ALERT Pin will be active HIGH, and the state of the ALERT Pin is inverted.

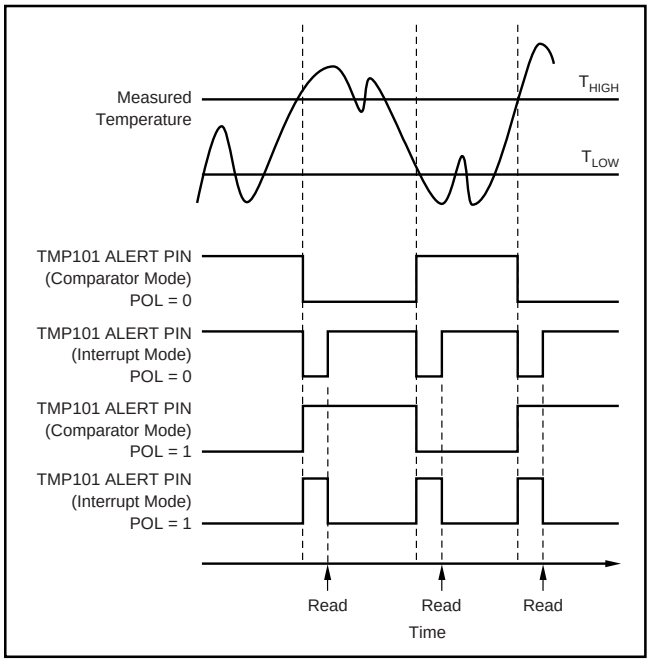


FIGURE 4. Output Transfer Function Diagrams.

FAULT QUEUE (F1/F0)

A fault condition occurs when the measured temperature exceeds the limits set in the T_{HIGH} and T_{LOW} Registers. The Fault Queue is provided to prevent a false alert due to environmental noise and requires consecutive fault measurements to trigger the alert function of the TMP101. Table VII defines the number of measured faults that may be programmed to trigger an alert condition.

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

TABLE VII. Fault Settings of the TMP100 and TMP101.

CONVERTER RESOLUTION (R1/R0)

The Converter Resolution Bits control the resolution of the internal Analog-to-Digital (A/D) converter. This allows the user to maximize efficiency by programming for higher resolution or faster conversion time. Table VIII identifies the Resolution Bits and relationship between resolution and conversion time.

R1	R0	RESOLUTION	CONVERSION TIME (typical)
0	0	9 Bits (0.5°C)	40ms
0	1	10 Bits (0.25°C)	80ms
1	0	11 Bits (0.125°C)	160ms
1	1	12 Bits (0.0625°C)	320ms

TABLE VIII. Resolution of the TMP100 and TMP101.

OS/ALERT (OS)

The TMP100 and TMP101 feature a One-Shot Temperature Measurement Mode. When the device is in Shutdown Mode, writing a 1 to the OS/ALERT bit will start a single temperature conversion. The device will return to the shutdown state at the completion of the single conversion. This is useful to reduce power consumption in the TMP100 and TMP101 when continuous monitoring of temperature is not required.

Reading the OS/ALERT bit will provide information about the Comparator Mode status. The state of the POL bit will invert the polarity of data returned from the OS/ALERT bit. For POL = 0, the OS/ALERT will read as 0 until the temperature equals or exceeds T_{HIGH} for the programmed number of consecutive faults, causing the OS/ALERT bit to read as 1. The OS/ALERT bit will continue to read as 1 until the temperature falls below T_{LOW} for the programmed number of consecutive faults when it will again read as 0. The status of the TM bit does not affect the status of the OS/ALERT bit.

HIGH AND LOW LIMIT REGISTERS

In Comparator Mode (TM = 0), the ALERT Pin of the TMP101 becomes active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin will remain active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In Interrupt Mode (TM = 1) the ALERT Pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. The ALERT pin remains active until a read operation of any register occurs or the device successfully responds to the SMBus Alert Response Address. The ALERT pin will also be cleared if the device is placed in Shutdown Mode. Once the ALERT pin is cleared, it will only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin will become active and remain active until cleared by a read operation of any register or a successful response to the SMBus Alert Response Address. Once the ALERT pin is cleared, the above cycle will repeat with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This will also clear the state of the internal registers in the device returning the device to Comparator Mode (TM = 0).

Both operational modes are represented in the Figure 4. Tables IX and X describe the format for the T_{HIGH} and T_{LOW} registers. Power-up Reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature Register.

All 12 bits for the Temperature, T_{HIGH}, and T_{LOW} registers are used in the comparisons for the ALERT function for all converter resolutions. The three LSBs in T_{HIGH} and T_{LOW} can affect the ALERT output even if the converter is configured for 9-bit resolution.

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4

Byte	D7	D6	D5	D4	D3	D2	D1	D0
2	H3	H2	H1	H0	0	0	0	0

TABLE IX. Bytes 1 and 2 of T_{HIGH} Register.

Byte	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4

Byte	D7	D6	D5	D4	D3	D2	D1	D0
2	L3	L2	L1	L0	0	0	0	0

TABLE X. Bytes 1 and 2 of T_{LOW} Register.

SERIAL INTERFACE

The TMP100 and TMP101 operate only as slave devices on the I^2C bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The TMP100 and TMP101 support the transmission protocol for fast (up to 400kHz) and high-speed (up to 3.4MHz) modes. All data bytes are transmitted most significant bit first.

SERIAL BUS ADDRESS

To program the TMP100 and TMP101, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP100 features two address pins to allow up to eight devices to be addressed on a single I^2C interface. Table XI describes the pin logic levels used to properly connect up to eight devices. 'Float' indicates the pin is left unconnected. The state of pins ADD0 and ADD1 is sampled on the first I^2C bus communication and should be set prior to any activity on the interface.

ADD1	ADD0	SLAVE ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111

TABLE XI. Address Pins and Slave Addresses for TMP100.

The TMP101 features one address pin and an ALERT pin, allowing up to three devices to be connected per bus. Pin logic levels are described in Table XII. The address pins of the TMP100 and TMP101 are read after reset or in response to an I^2C address acquire request. Following reading, the state of the address pins is latched to minimize power dissipation associated with detection.

ADD0	SLAVE ADDRESS
0	1001000
Float	1001001
1	1001010

TABLE XII. Address Pins and Slave Address for TMP101.

BUS OVERVIEW

The device that initiates the transfer is called a “master,” and the devices controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a HIGH to LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge Bit. During data transfer SDA must remain stable while SCL is HIGH, as any change in SDA while SCL is HIGH will be interpreted as a control signal.

Once all data has been transferred, the master generates a STOP condition indicated by pulling SDA from LOW to HIGH, while SCL is HIGH.

WRITING/READING TO THE TMP100 AND TMP101

Accessing a particular register on the TMP100 and TMP101 is accomplished by writing the appropriate value to the Pointer Register. The value for the Pointer Register is the first byte transferred after the I^2C slave address byte with the R/$\overline{W}$ bit LOW. Every write operation to the TMP100 and TMP101 requires a value for the Pointer Register. (Refer to Figure 6.)

When reading from the TMP100 and TMP101, the last value stored in the Pointer Register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer Register. This is accomplished by issuing an I^2C slave address byte with the R/$\overline{W}$ bit LOW, followed by the Pointer Register Byte. No additional data is required. The master can then generate a START condition and send the I^2C slave address byte with the R/$\overline{W}$ bit HIGH to initiatnlthe read command. See Figure 7 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes as the TMP100 and TMP101 will remember the Pointer Register value until it is changed by the next write operation.

SLAVE MODE OPERATIONS

The TMP100 and TMP101 can operate as slave receivers or slave transmitters.

Slave Receiver Mode:

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit LOW. The TMP100 or TMP101 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer Register. The TMP100 or TMP101 then acknowledges reception of the Pointer Register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP100 and TMP101 will acknowledge reception of each data byte. The master may terminate data transfer by generating a START or STOP condition.

Slave Transmitter Mode:

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit HIGH. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer Register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master may terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

SMBus ALERT FUNCTION

The TMP101 supports the SMBus Alert function. When the TMP101 is operating in Interrupt Mode (TM = 1), the ALERT pin of the TMP101 may be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP101 is active, the TMP101 will acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte will indicate if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit will be HIGH if the temperature is greater than or equal to T_{HIGH}. This bit will be LOW if the temperature is less than T_{LOW}. Refer to Figure 8 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus alert command will determine which device will clear its ALERT status. If the TMP101 wins the arbitration, its ALERT pin will become inactive at the completion of the SMBus Alert command. If the TMP101 loses the arbitration, its ALERT pin will remain active.

The TMP100 will also respond to the SMBus ALERT command if its TM bit is set to 1. Since it does not have an ALERT pin, the master needs to periodically poll the device by issuing an SMBus Alert command. If the TMP100 has generated an ALERT, it will acknowledge the SMBus Alert command and return its slave address in the next byte.

GENERAL CALL

The TMP100 and TMP101 respond to the I^2C General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100, the TMP100 and TMP101 will latch the status of their address pins, but will not reset. If the second byte is 00000110, the TMP100 and TMP101 will latch the status of their address pins and reset their internal registers.

HIGH-SPEED MODE

In order for the I²C bus to operate at frequencies above 400kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP100 and TMP101 will not acknowledge this byte as required by the I²C specification, but will switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 3.4MHz. After the Hs-mode master code has been issued, the master will transmit an I²C slave address to initiate a data transfer operation. The bus will continue to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP100 and TMP101 will switch their input and output filters back to fast-mode operation.

TIMING DIAGRAMS

The TMP100 and TMP101 are I²C and SMBus compatible. Figures 5 to 8 describe the various operations on the TMP100 and TMP101. Bus definitions are given below. Parameters for Figure 5 are defined in Table XIII.

Bus Idle: Both SDA and SCL lines remain HIGH.

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCL line is HIGH, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCL line is HIGH defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that has been transmitted by the slave.

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCLK Operating Frequency	$f_{(SCLK)}$		0.4		3.4	MHz
Bus Free Time Between STOP and START Condition	$t_{(BUF)}$	600		160		ns
Hold Time After Repeated START Condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START Condition Setup Time	$t_{(SUSTA)}$	600		160		ns
STOP Condition Setup Time	$t_{(SUSTO)}$	600		160		ns
Data Hold Time	$t_{(HDDAT)}$	0		0		ns
Data Setup Time	$t_{(SUDAT)}$	100		10		ns
SCLK Clock LOW Period	$t_{(LOW)}$	1300		160		ns
SCLK Clock HIGH Period	$t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time	t_F		300		160	ns
Clock/Data Rise Time	t_R		300		160	ns

TABLE XIII. Timing Diagram Definitions.

I²C TIMING DIAGRAMS

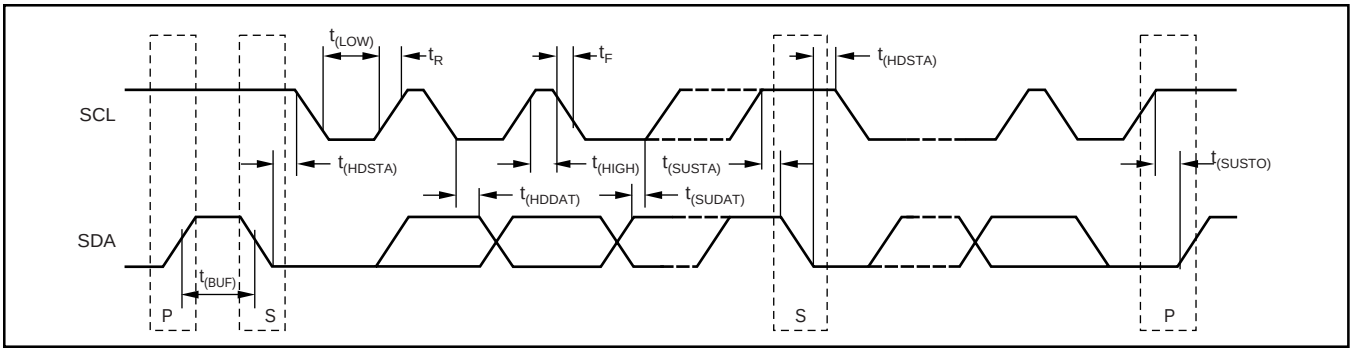


FIGURE 5. I²C Timing Diagram.

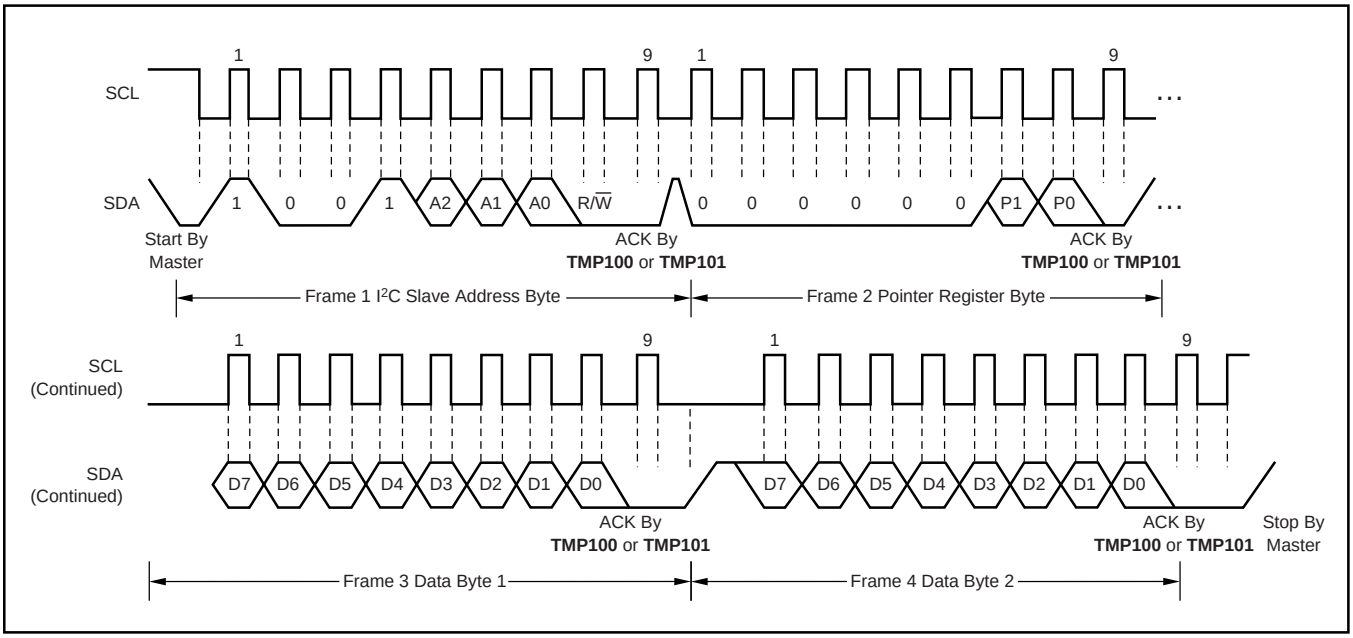


FIGURE 6. I²C Timing Diagram for Write Word Format.

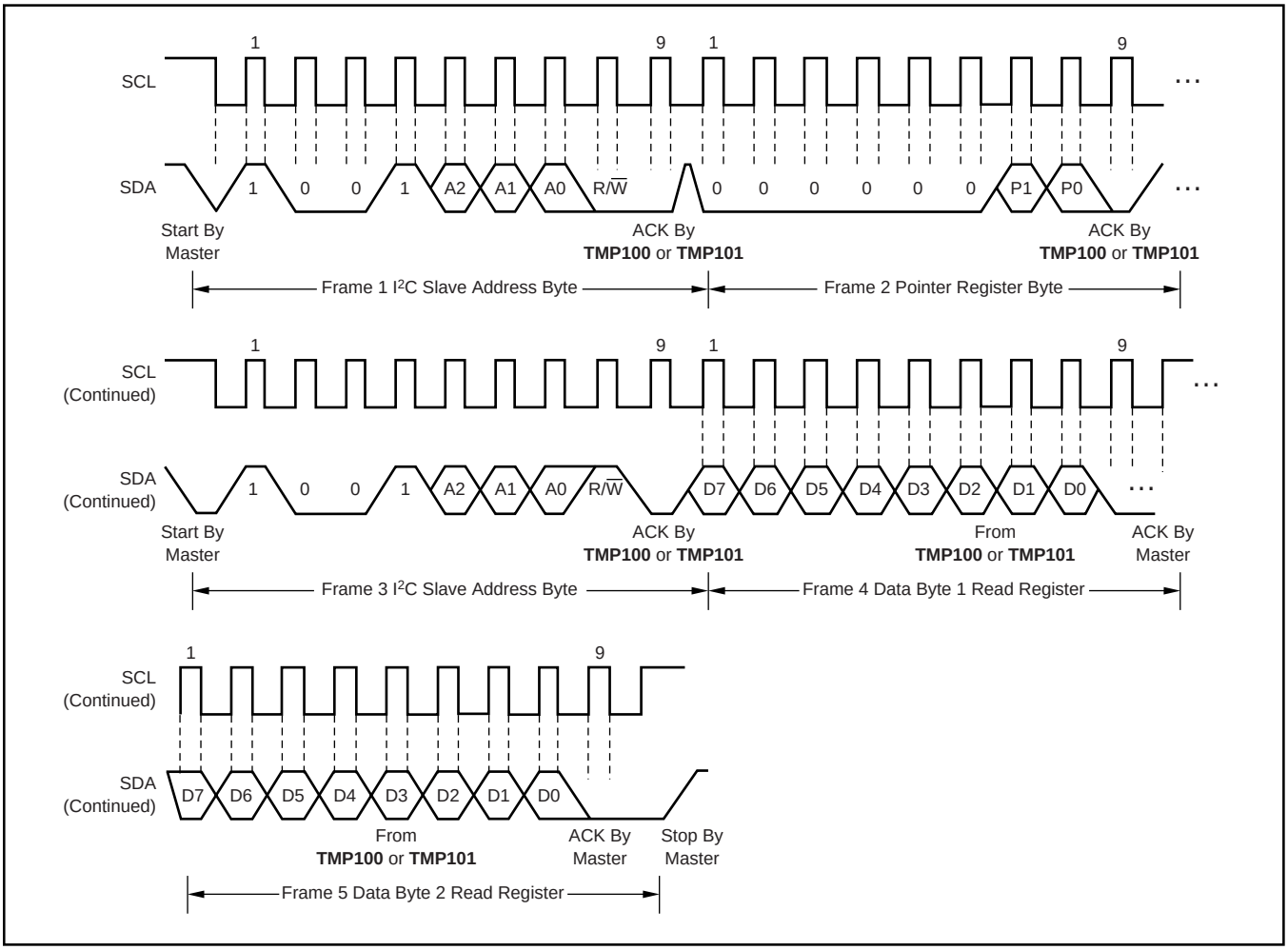


FIGURE 7. I²C Timing Diagram for Read Word Format.

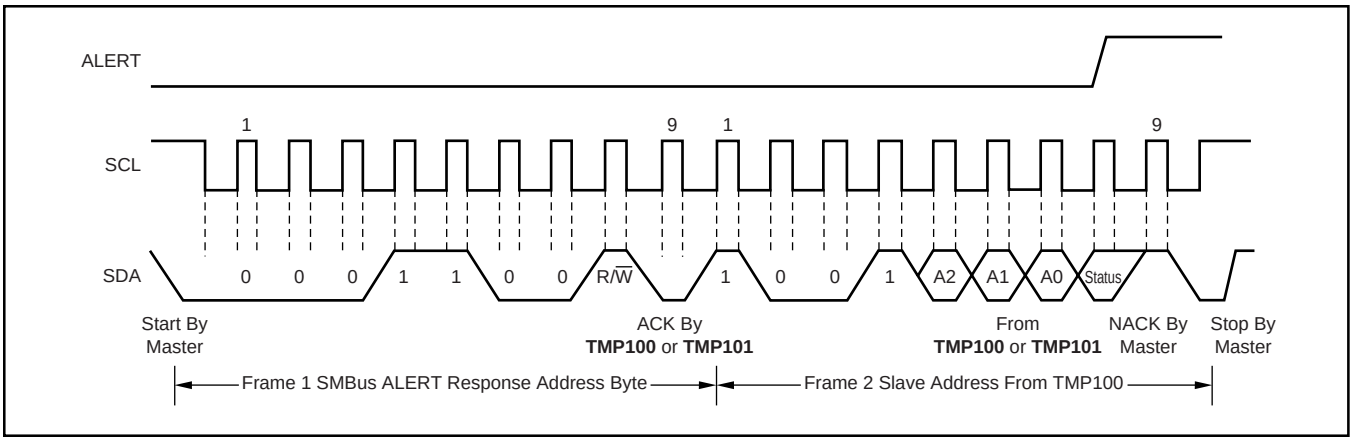


FIGURE 8. Timing Diagram for SMBus ALERT.

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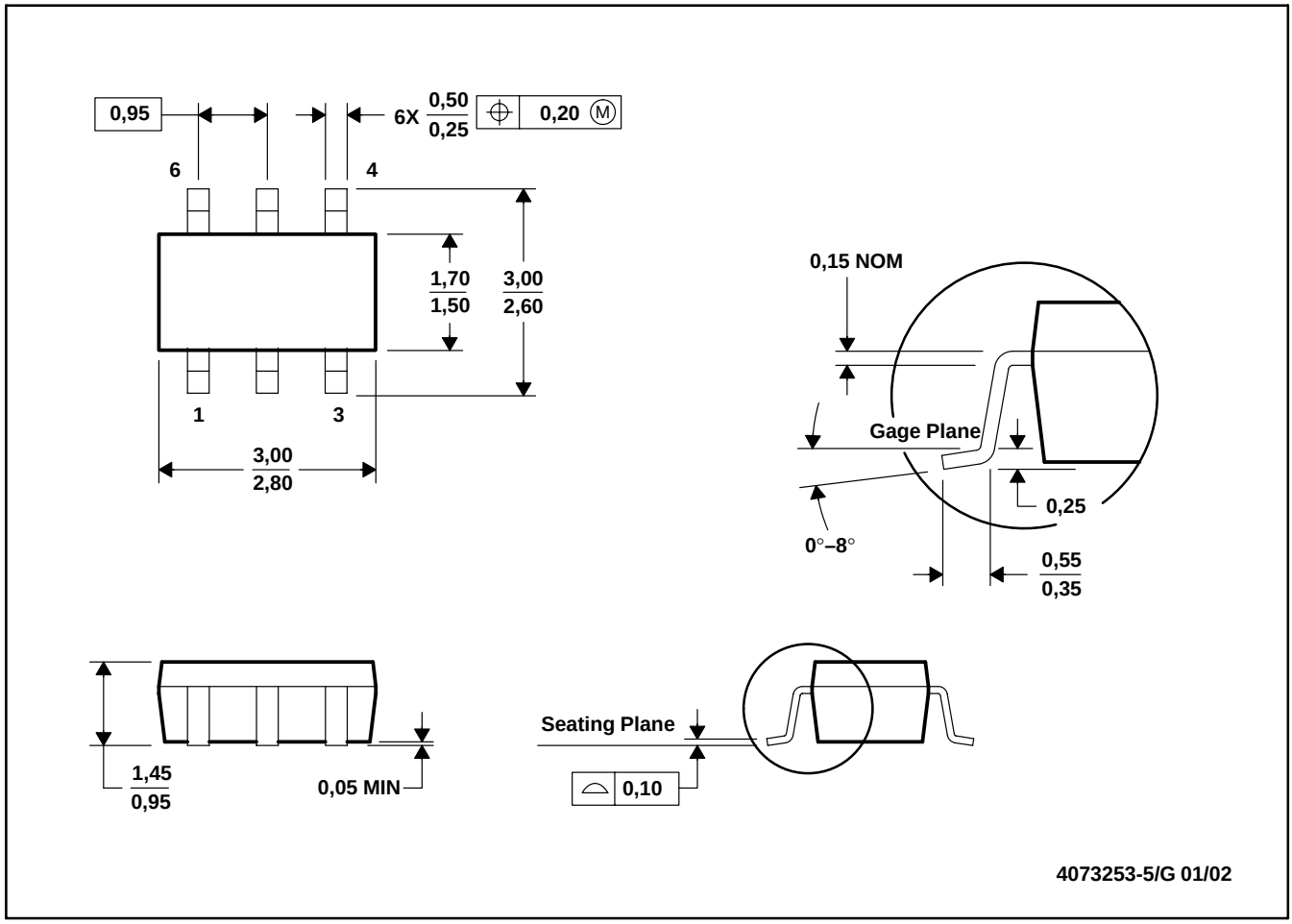
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

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