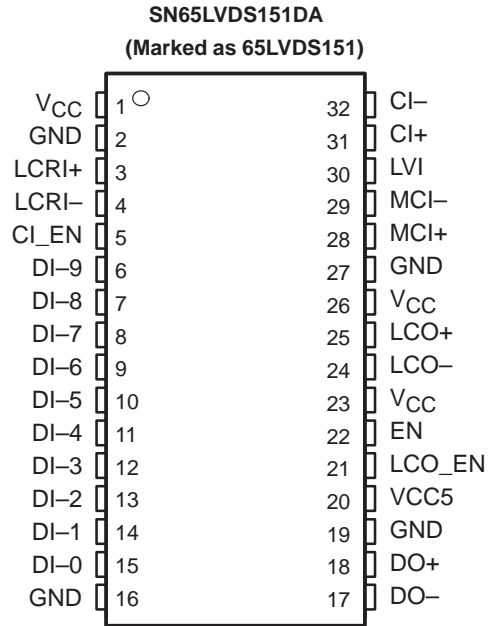


- **A Member of the MuxIt™ Serializer-Deserializer Building-Block Chip Family**
- **Supports Serialization of up to 10 Bits of Parallel Data Input at Rates up to 200 Mbps**
- **PLL Lock/Valid Input Provided to Enable Link Data Transfers**
- **Cascadable With Additional SN65LVDS151 MuxIt Serializer-Transmitters for Wider Parallel Input Data Channel Widths**
- **LVDS Compatible Differential Inputs and Outputs Meet or Exceed the Requirements of ANSI TIA/EIA-644-A**
- **LVDS Inputs and Outputs ESD Protection Exceeds 12 kV HBM**
- **LVTTL Compatible Inputs for Lock/Valid, Enables, and Parallel Data Inputs Are 5-V Tolerant**
- **Operates With 3.3 V Supply**
- **Packaged in 32-Pin DA Thin Shrink Small-Outline Package With 26 Mil Terminal Pitch**



description

MuxIt is a family of general-purpose, multiple-chip building blocks for implementing parallel data serializers and deserializers. The system allows for wide parallel data to be transmitted through a reduced number of transmission lines over distances greater than can be achieved with a single-ended (e.g., LVTTL or LVCMOS) data interface. The number of bits multiplexed per transmission line is user-selectable and allows for higher transmission efficiencies than with existing fixed ratio solutions. MuxIt utilizes the LVDS (TIA/EIA-644-A) low voltage differential signaling technology for communications between the data source and data destination.

The MuxIt family initially includes three devices supporting simplex communications: the SN65LVDS150 phase locked loop frequency multiplier, the SN65LVDS151 serializer-transmitter, and the SN65LVDS152 receiver-deserializer.

The SN65LVDS151 consists of a 10-bit parallel-in/serial-out shift register, three LVDS differential transmission line receivers, a pair of LVDS differential transmission line drivers, plus associated input buffers. It accepts up to 10 bits of user data on parallel data inputs (DI-0 → DI-9) and serializes (multiplexes) the data for transmission over an LVDS transmission line link. Two or more SN65LVDS151 units may be connected in series (cascaded) to accommodate wider parallel data paths for higher serialization values. Data is transmitted over the LVDS serial link at M times the input parallel data clock frequency. The multiplexing ratio M, or number of bits per data clock cycle, is programmed on the companion SN65LVDS150 MuxIt programmable PLL frequency multiplier with configuration pins (M1 → M5). The range of multiplexing ratio M supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier is between 4 and 40. Table 1 shows some of the combinations of LCRI and MCI supported by the SN65LVDS150 MuxIt programmable PLL frequency multiplier.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description (continued)

Data is parallel loaded into the SN65LVDS151 input latches on the first rising edge of the M-clock input (MCI) signal following a rising edge of the link clock reference input (LCRI). The data is read out serially from the SN65LVDS151 shift registers on the rising edges of the M-clock input (MCI). The lowest order bit of parallel input data, DI-0, is output from DO on the third rising edge of MCI following the rising edge of LCRI. The remaining bits of parallel input data, DI-1 → DI-(M-1) are clocked out sequentially, in ascending order, by subsequent MCI rising edges. The link clock output (LCO) signal rising edge is synchronized to the data output (DO) by an internal circuit clocked by MCI. The LCO signal rising edge follows the first rising edge of MCI after the rising edge of LCRI. Examples of operating waveforms for values of M = 4 and M = 10 are provided in Figure 1.

Both the LCRI and MCI signals are intended to be sourced from the SN65LVDS150 MuxIt programmable frequency multiplier. They are carried over LVDS differential connections to minimize skew and jitter. The SN65LVDS151 includes LVDS differential line drivers for both the serialized data output (DO) stream and the link clock output (LCO). The cascade input (CI) is also an LVDS connection, and when it is used it is tied to the DO output of the preceding SN65LVDS151.

An internal power-on reset (POR) and an enable input (EN) control the operation of the SN65LVDS151. When V_{CC} is below 1.5 V, or when EN is low, the device is in a low-power disabled state, and the DO and LCO differential outputs are in a high-impedance state. When V_{CC} is above 3 V and EN is high, the device and the two differential outputs are enabled and operating to specifications. The link clock output enable input (LCO_EN) is used to turn off the LCO output when it is not being used. Cascade input enable (CI_EN) is used to turn off the CI input when it is not being used.

Serialized data bits are output from the DO output, starting in ascending order, from parallel input bit DI-0. The number of serialized data bits output per data clock cycle is determined by the multiplexing ratio M. For values of M less than or equal to 10, the cascade input (CI±) is not used, and only the first M parallel input bits (DI-0 though DI-[M-1]) are used. For values of M greater than 10, all ten parallel input bits (DI-0 though DI-9) are used, and the cascade input is used to shift in the remaining data bits from additional SN65LVDS151 serializers. Table 2 shows which input data bits are used as a function of the multiplier M.

Table 1. Example Combinations of LCRI and MCI Supported by the SN65LVDS150 MuxIt Programmable PLL Frequency Multiplier

M	LCRI, MHz		MCI, MHz	
	MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
4	5	50	20	200
10	5	20	50	200
20	5	10	100	200
40	5	5	200	200

description (continued)

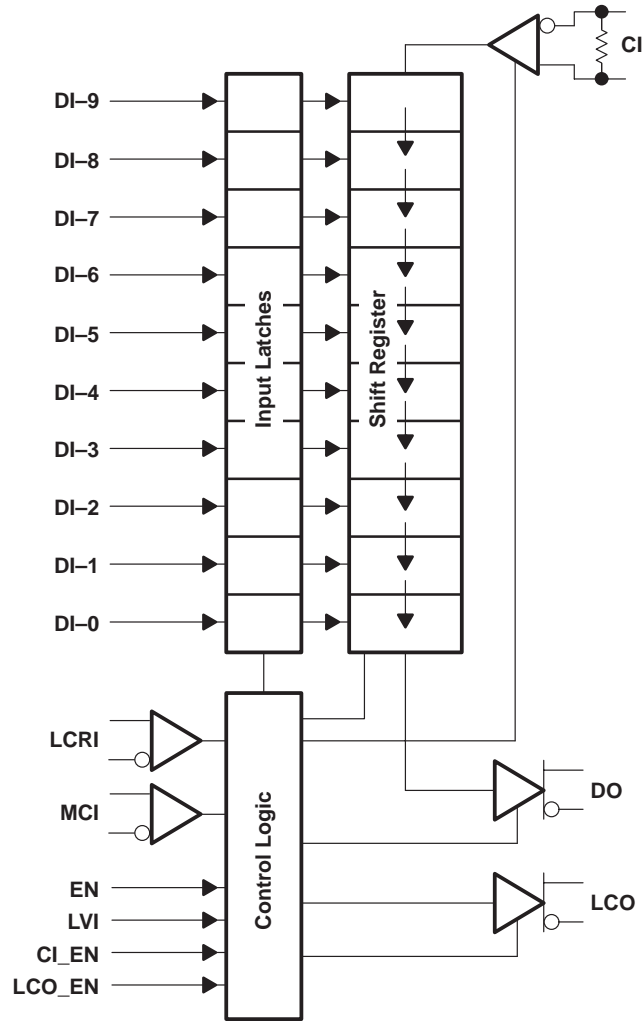
Table 2. Input Data Bits Used as a Function of the Multiplier M

	M = 4	M = 5	M = 6	M = 7	M = 8	M = 9	M = 10	M >10
1 st bit output	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0	DI-0
2 nd bit output	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1	DI-1
3 rd bit output	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2	DI-2
4 th bit output	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3	DI-3
5 th bit output	Invalid	DI-4	DI-4	DI-4	DI-4	DI-4	DI-4	DI-4
6 th bit output	Invalid	Invalid	DI-5	DI-5	DI-5	DI-5	DI-5	DI-5
7 th bit output	Invalid	Invalid	Invalid	DI-6	DI-6	DI-6	DI-6	DI-6
8 th bit output	Invalid	Invalid	Invalid	Invalid	DI-7	DI-7	DI-7	DI-7
9 th bit output	Invalid	Invalid	Invalid	Invalid	Invalid	DI-8	DI-8	DI-8
10 th bit output	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	DI-9	DI-9
11 th + bits output	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	CI bits

SN65LVDS151 MuxIt™ SERIALIZER-TRANSMITTER

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block diagram



† The CI input includes a 110 Ω termination resistor.

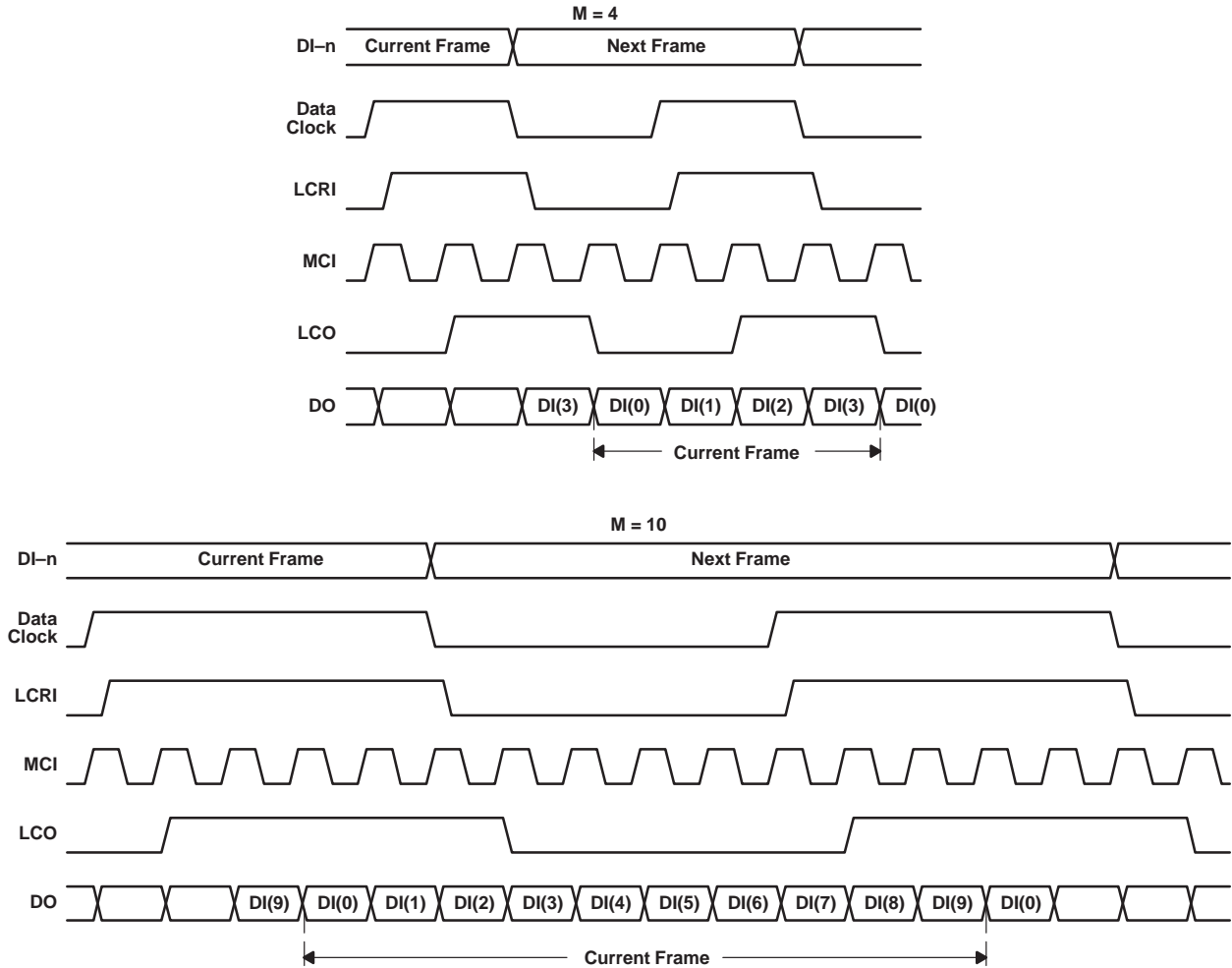
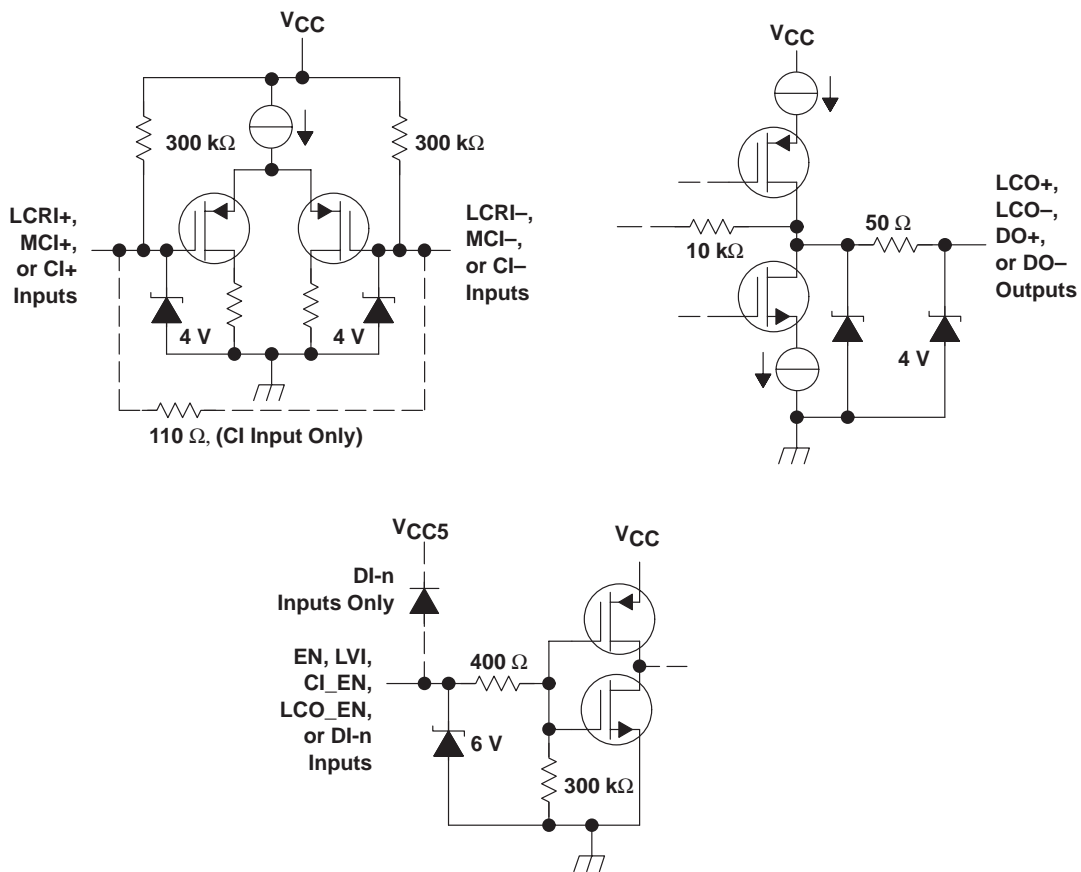


Figure 1. Operating Waveform Examples

SN65LVDS151 MuxIt™ SERIALIZER-TRANSMITTER

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equivalent input and output schematic diagrams



Terminal Functions

TERMINAL NAME	NO.	I/O	TYPE	DESCRIPTION
CI+, CI-	31, 32	I	LVDS	Cascade input. This may be used to connect additional SN65LVDS151 units when the multiplexing ratio M value is greater than 10. This input has an internal 110-Ω nominal termination resistor.
CI_EN	5	I	LVTTTL	Cascade input enable. Used to enable or disable the cascade input differential receiver. A high-level input enables the CI input, a low-level input disables the CI input.
DO-, DO+	17, 18	O	LVDS	Data output. This is the data being transmitted to the destination end of the serial link, or being supplied to another SN65LVDS151 unit in cascade.
EN	22	I	LVTTTL	Enable. Controls device operation. A high-level input enables the device; a low-level input disables and resets the device. When initially enabled, all outputs are in a low-level condition.
GND	2, 16, 19, 27		NA	Circuit ground
LCO+, LCO-	25, 24	O	LVDS	Link clock output This is the data block synchronization clock being transmitted to the destination end of the serial link.
LCO_EN	21	I	LVTTTL	Link clock output enable. Used to disable the link clock output when it is not being used. A high-level input enables the LCO output; a low-level input disables the LCO output.
LCRI+, LCRI-	3, 4	I	LVDS	Link clock reference input. This is the clock for latching in the parallel data; it comes from the PLL frequency multiplier.
LVI	30	I	LVTTTL	Lock/valid input. This is a signal required for proper MuxIt system operation. It is directly connected to the LVO output of a SN65LVDS150. It is used to inhibit the operation of this device until after the PLL has stabilized. A low level input forces a reset of the internal latches and shift registers, and forces the DO and LCO outputs to a low level. A high level input enables operation.
MCI+, MCI-	28, 29	I	LVDS	M-clock input. This is the high frequency multiplied clock input from the local PLL frequency multiplier. It synchronizes the transmission of the link data
DI-9–DI-0	6-15	I	LVTTTL	Parallel data inputs. Data is latched into the device on the first rising edge of MCI following a rising edge of LCRI.
V _{CC}	1, 23, 26		NA	Supply voltage
VCC5	20		NA	5-V V _{CC} tolerance bias. Tied to 5 V nominal when the LVTTTL inputs are being driven by a device powered from a 5-V supply, otherwise tied to local V _{CC}

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	–0.5 V to 4 V
Voltage range: DI-0 through DI-9 inputs	–0.5 V to VCC5 +0.5 V
EN, CI_EN, LCO_EN, LVI inputs, VCC5	–0.5 V to 5.5 V
CI±, LCRI±, or MCI± Inputs, DO±, or LCO± outputs	–0.5 to 4 V
Electrostatic discharge, human body model (see Note 2):	
MCI±, LCRI±, CI±, DO±, LCO±, and GND	±12 kV
All pins	±2 kV
Charged-device model (see Note 3): All pins	
Charged-device model (see Note 3): All pins	±500 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
 2. Tested in accordance with JEDEC Standard 22, Test Method A114–B.
 3. Tested in accordance with JEDEC Standard 22, Test Method C101.



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DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING
DA	1453 mW	11.6 mW/°C	756 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	3	3.3	3.6	V
High-level input voltage, V _{IH}	2			V
Low-level input voltage, V _{IL}	0.8			V
Magnitude of differential input voltage, V _{ID}	0.1	0.6		V
Common-mode input voltage, V _{IC}	LCRI, MCI, CI		$\frac{ V_{ID} }{2}$	V
			$2.4 - \frac{ V_{ID} }{2}$	V
			V _{CC} -0.8	V
Operating free-air temperature, T _A	-40	85		°C

timing requirements

PARAMETERS	TEST CONDITIONS	MIN	MAX	UNIT
t _{su(1)} LCRI↑ setup time before MCI↑	See Figure 2	0.5		ns
t _{h(1)} LCRI hold time after MCI↑		0.3		ns
t _{su(2)} Data setup time, DI-0 – DI-9 before MCI↑ after LCRI↑	See Figure 3	0		ns
t _{h(2)} Data hold time, DI-0 – DI-9 valid after MCI↑ after LCRI↑		2		ns
t _{su(3)} CI setup time before MCI↑	T _A ≤ 25°C	-0.8		ns
	T _A = 85°C	-1.1		
t _{h(3)} CI hold time after MCI↑		2.5		ns
t _c Clock cycle time	LCRI	20	200	ns
	MCI	5	50	
t _w High-level clock pulse width duration	MCI, LCRI	0.4 t _c	0.6 t _c	ns

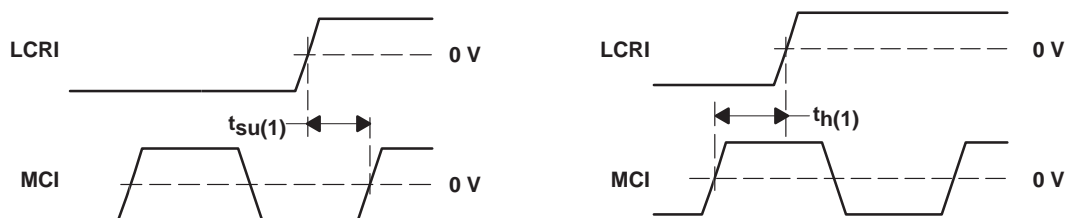


Figure 2. Clock Input Timing Requirements

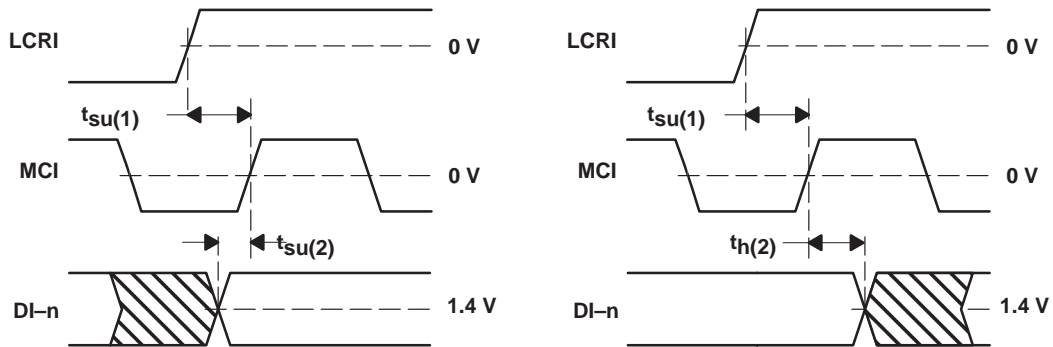


Figure 3. Data Input Timing Requirements

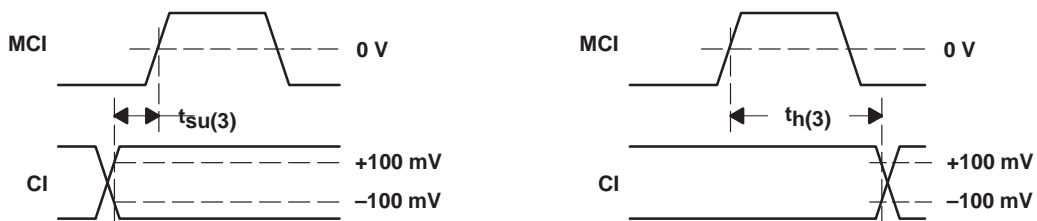


Figure 4. Cascade Input Timing Requirements

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electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{ITH+}	Positive-going differential input voltage threshold	See Figure 5			100	mV
V _{ITH-}	Negative-going differential input voltage threshold				-100	mV
V _{OD(SS)}	Steady-state differential output voltage magnitude	R _L = 100 Ω, V _{ID} = ±100 mV, See Figures 6 and 7	247	340	454	mV
Δ V _{OD(SS)}	Change in steady-state differential output voltage magnitude between logic states			-50	50	mV
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 8	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states			-50	50	mV
V _{OC(PP)}	Peak-to-peak change common-mode output voltage			50	150	mV
I _{CC}	Supply current	Enabled, R _L = 100 Ω,		22	30	mA
		Disabled		0.5	1	
		f(MCI) = 200 MHz, f(LCRI) = 20 MHz, R _L = 100 Ω, DI-n = 1010101010		35	65	
I _{ID}	Differential input current	(I _{I+} - I _{I-}) (CI input)	V _{ID} = 0.4 V, V _{IC} = 2.2 V or 0.2 V	3	4.4	mA
		(I _{I+} - I _{I-}) (LCRI, MCI inputs)	V _{IC} = 0.05 V to 2.35 V, V _{ID} = ±0.1 V	-2	2	μA
I _I	Input current	LCRI, MCI inputs	V _I = 0 V	-2	-20	μA
			V _I = 2.4 V	-1.2		
		CI input	V _I = 0 V	-4	-40	μA
			V _I = 2.4 V	-2.4		
I _{I(OFF)}	Power-off output current	LCRI, MCI inputs	V _{CC} = 0 V, V _I = 3.6 V		20	μA
		CI input			40	
I _{IH}	High-level input current	EN, LVI, DI-n, LCO_EN	V _{IH} = 2 V		20	μA
I _{IL}	Low-level input current	EN, LVI, DI-n, LCO_EN	V _{IL} = 0.8 V		10	μA
I _{OS}	Short-circuit output current	DO, LCO	V _{O+} or V _{O-} = 0 V	-10	10	mA
			V _{OD} = 0 V	-10	10	
I _{OZ}	High-impedance output current		V _O = 0 V or V _{CC}	-5	5	μA
I _{O(OFF)}	Power-off output current		V _{CC} = 1.5 V, V _I = 3.6 V	-5	5	μA
C _I	Input capacitance	LCRI, MCI inputs	V _{ID} = (0.4sin(4E6πt) + 0.5) V	3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.



switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d(1)}	Propagation delay time, MCI↑ to DO↑	T _A ≤ 25°C	3	5	5.8	ns
		T _A = 85°C	3	5	6.1	
t _{d(2)}	Propagation delay time, MCI↑ to DO↓	T _A ≤ 25°C	3	5	5.8	ns
		T _A = 85°C	3	5	6.1	
t _{d(3)}	Propagation delay time, MCI↑ to LCO↑	T _A ≤ 25°C	3	5	5.8	ns
		T _A = 85°C	3	5	6.1	
t _r	Differential output signal rise time	R _L = 100 Ω, C _L = 10 pF, See Figure 9	0.3	0.8	1.5	ns
t _f	Differential output signal fall time		0.3	0.8	1.5	ns
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH}), DO		-250	0	250	ps
t _{sk(pp)}	Part-to-part output skew, Do			0	2.3	ns
t _{sk(ω)}	Multiple-frequency skew, LCO↑ to DO↑ or DO↓	See Figure 11	-250	0	250	ps
t _{PZL}	Propagation delay time, high-impedance to low-level	EN input to DO, LCO output, See Figure 12		3	20	ns
t _{PLZ}	Propagation delay time, low-level to high-impedance			3	10	ns
t _{PHZ}	Propagation delay time, high-level to high-impedance			4	10	ns

PARAMETER MEASUREMENT INFORMATION

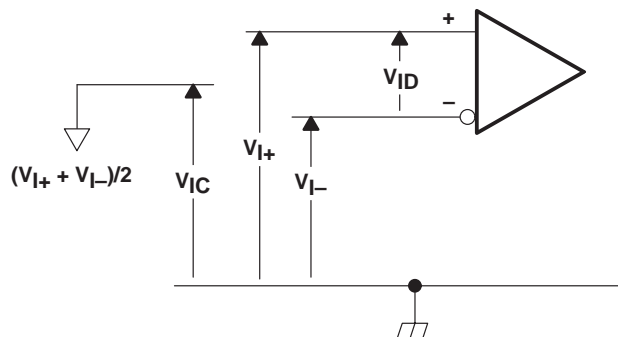


Figure 5. Receiver Voltage Definitions

Table 3. Receiver Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V _{I+}	V _{I-}	V _{ID}	V _{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	-100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	-100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	-100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	-600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	-600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	-600 mV	0.3 V

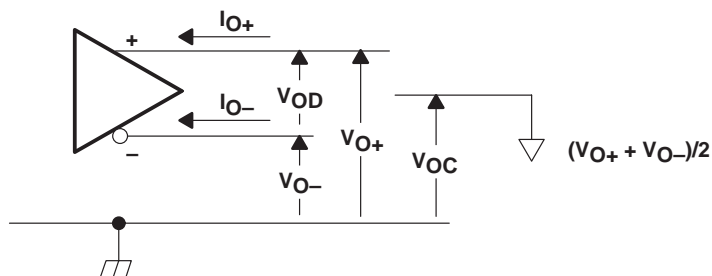


Figure 6. Driver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION

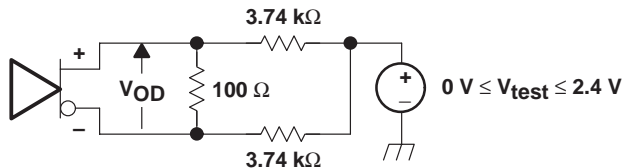
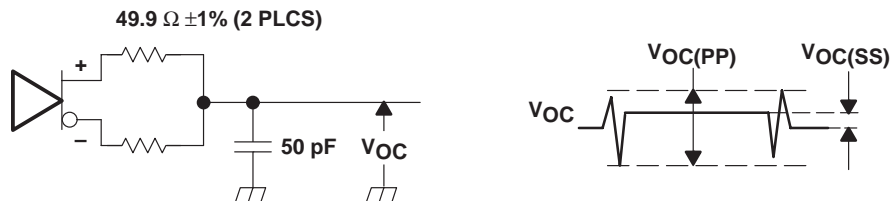


Figure 7. V_{OD} Test Circuit



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 5 GHz.

Figure 8. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

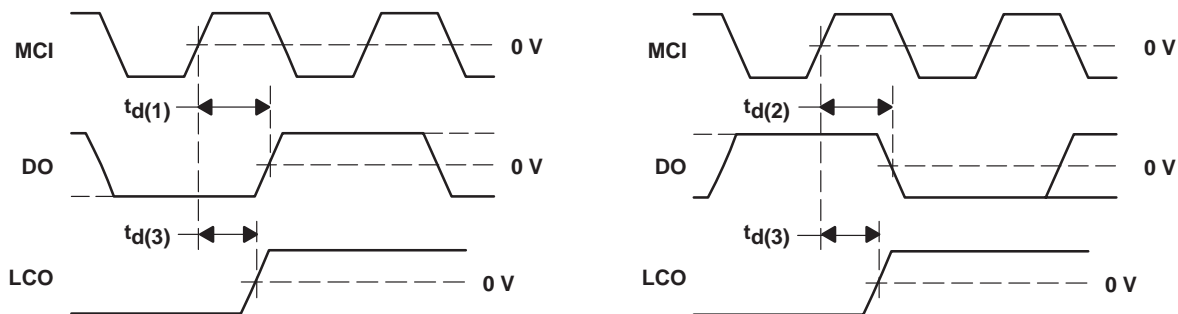
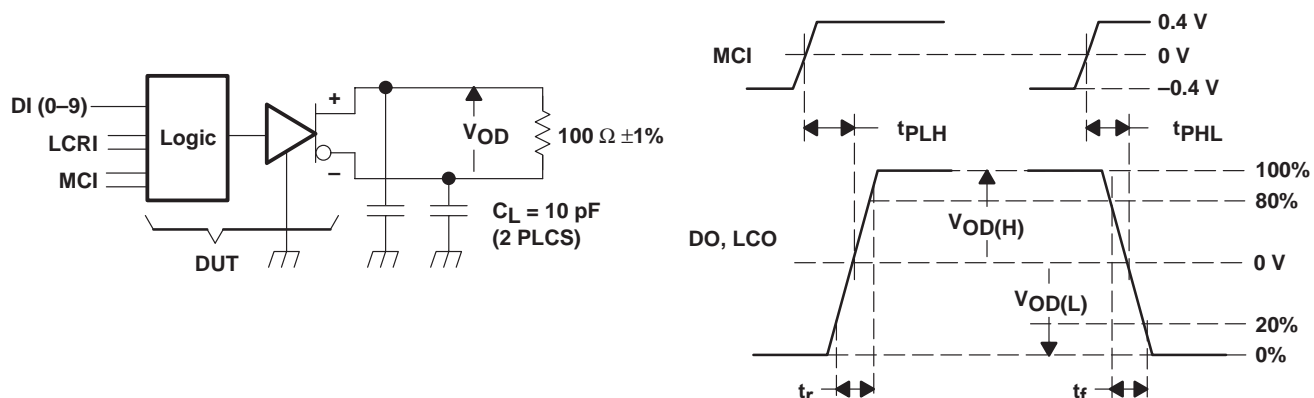


Figure 9. Output Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: All input pulses are supplied by generators having the following characteristics: t_r or $t_f \leq 1\ \text{ns}$, MCI pulse repetition rate (PRR) = 50 Mpps, MCI Pulse width = $10 \pm 0.2\ \text{ns}$, LCRI pulse repetition rate (PRR) = 5 Mpps, LCRI pulse width = $100 \pm 20\ \text{ns}$. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 10. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

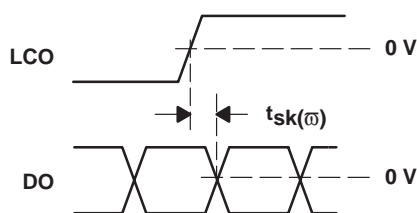


Figure 11. LCO to DO Multiple-Frequency Skew Waveforms

PARAMETER MEASUREMENT INFORMATION

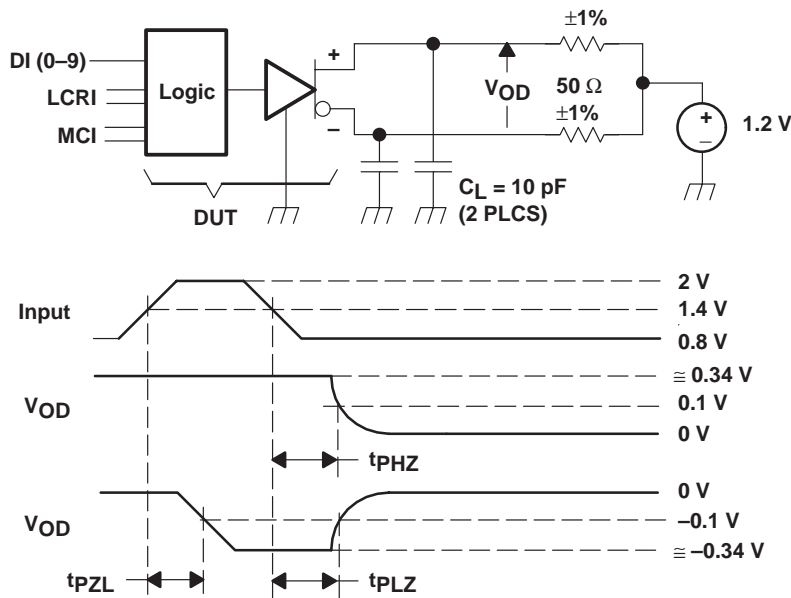


Figure 12. Enable/Disable Time Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

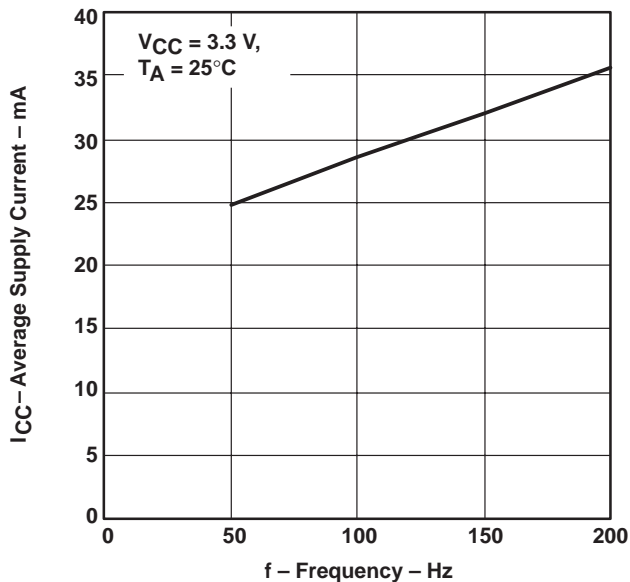


Figure 13. Average Supply Current vs Frequency

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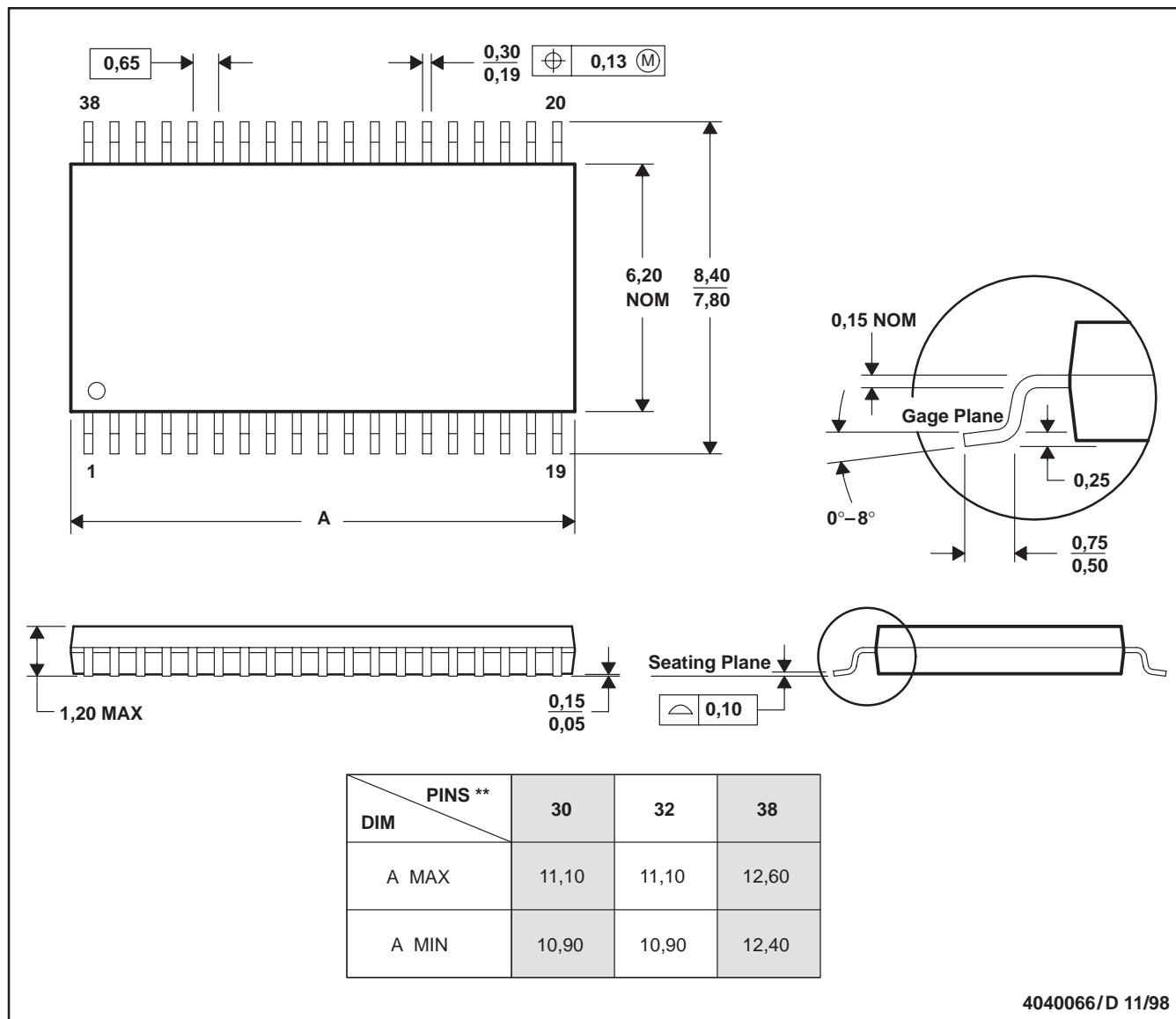
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MECHANICAL INFORMATION

DA (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

38 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC MO-153

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