CD54HC194, CD74HC194, CD74HCT194

Data sheet acquired from Harris Semiconductor
SCHS164F

September 1997 - Revised October 2003

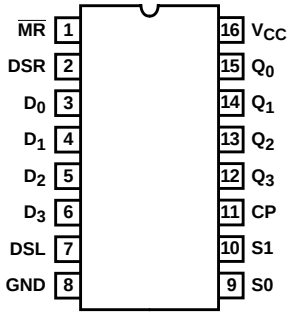
High-Speed CMOS Logic 4-Bit Bidirectional Universal Shift Register

Features

- **Four Operating Modes**
  - **Shift Right, Shift Left, Hold and Reset**
- **Synchronous Parallel or Serial Operation**
- **Typical f_{MAX} = 60MHz at V_{CC} = 5V, C_L = 15pF, $T_A = 25^oC$**
- **Asynchronous Master Reset**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Pinout

CD54HC194 (CERDIP)
CD74HC194 (PDIP, SOIC, SOP, TSSOP)
CD74HCT194 (PDIP)
TOP VIEW



Description

The ’HC194 and CD74HCT194 are 4-bit shift registers with Asynchronous Master Reset ($\overline{MR}$). In the parallel mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift right mode, and at the shift right (DSR) serial input for the shift left mode. Clearing the register is accomplished by a Low applied to the Master Reset ($\overline{MR}$) pin.

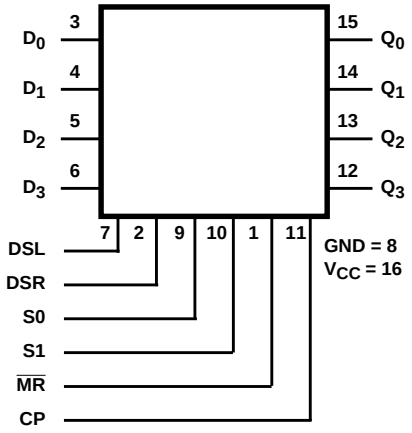
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC194F3A	-55 to 125	16 Ld CERDIP
CD74HC194E	-55 to 125	16 Ld PDIP
CD74HC194M	-55 to 125	16 Ld SOIC
CD74HC194MT	-55 to 125	16 Ld SOIC
CD74HC194M96	-55 to 125	16 Ld SOIC
CD74HC194NSR	-55 to 125	16 Ld SOP
CD74HC194PW	-55 to 125	16 Ld TSSOP
CD74HC194PWR	-55 to 125	16 Ld TSSOP
CD74HC194PWT	-55 to 125	16 Ld TSSOP
CD74HCT194E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS							OUTPUT			
	CP	$\overline{MR}$	S1	S0	DSR	DSL	D_n	Q_0	Q_1	Q_2	Q_3
Reset (Clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (Do Nothing)	X	H	l (Note 1)	l (Note 1)	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l (Note 1)	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l (Note 1)	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l (Note 1)	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l (Note 1)	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	q_2	d_3

H = High Voltage Level,
h = High Voltage Level One Set-up Time Prior To The Low to High Clock Transition,
L = Low Voltage Level,
l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition,
d_n (q_n) = Lower Case Letters Indicate the State of the Referenced Input (or output) One Set-up Time Prior to the Low To High Clock Transition,
X = Don't Care,
↑ = Transition from Low to High Level
NOTE:

1. The High-to-Low transition of the S0 and S1 Inputs on the 'HC194 and CD74HCT194 should take place only while CP is High for Conventional Operation.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 2):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 3)	V_{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
CP	0.6
$\overline{MR}$	0.55
DSL, DSR, D_n	0.25
Sn	1.10

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

Prerequisite For Switching Function

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Max. Clock Frequency (Figure 1)	f_{MAX}	-	2	6	-	5	-	4	-	MHz
			4.5	30	-	24	-	20	-	MHz
			6	35	-	28	-	23	-	MHz
$\overline{MR}$ Pulse Width (Figure 2)	t_W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Clock Pulse Width (Figure 1)	t_W	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time Data to Clock (Figure 3)	t_{SU}	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	19	-	ns
Removal Time, $\overline{MR}$ to Clock (Figure 2)	t_{REM}	-	2	60	-	75	-	90	-	ns
			4.5	12	-	15	-	18	-	ns
			6	10	-	13	-	15	-	ns
Set-Up Time S1, S0 to Clock (Figure 4)	t_{SU}	-	2	80	-	100	-	120	-	ns
			4.5	16	-	20	-	24	-	ns
			6	14	-	17	-	20	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t_{SU}	-	2	70	-	90	-	105	-	ns
			4.5	14	-	18	-	21	-	ns
			6	12	-	15	-	18	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t_H	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t_H	-	2	0	-	0	-	0	-	ns
			4.5	0	-	0	-	0	-	ns
			6	0	-	0	-	0	-	ns
HCT TYPES										
Max. Clock Frequency (Figure 1)	f_{MAX}	-	4.5	27	-	22	-	18	-	MHz
$\overline{MR}$ Pulse Width (Figure 2)	t_W	-	4.5	16	-	20	-	24	-	ns
Clock Pulse Width (Figure 1)	t_W	-	4.5	16	-	20	-	24	-	ns
Set-up Time, Data to Clock (Figure 3)	t_{SU}	-	4.5	14	-	18	-	21	-	ns
Removal Time $\overline{MR}$ to Clock (Figure 2)	t_{REM}	-	4.5	12	-	15	-	18	-	ns

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	
Set-up Time S1, S0 to Clock (Figure 4)	t_{SU}	-	4.5	20	-	25	-	30	-	ns
Set-up Time DSL, DSR to Clock (Figure 4)	t_{SU}	-	4.5	14	-	18	-	21	-	ns
Hold Time S1, S0 to Clock (Figure 4)	t_H	-	4.5	0	-	0	-	0	-	ns
Hold Time Data to Clock (Figure 3)	t_H	-	4.5	0	-	0	-	0	-	ns

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
HC TYPES								
Propagation Delay, Clock to Output (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
Propagation Delay, Clock to Q	t_{PLH}, t_{PHL}	-	5	14	-	-	-	ns
Output Transition Time (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Propagation Delay, $\overline{MR}$ to Output (Figure 2)	t_{PHL}	C_L = 50pF	2	-	140	175	210	ns
			4.5	-	28	35	42	ns
			6	-	24	30	36	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
Maximum Clock Frequency	f_{MAX}	-	5	60	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	55	-	-	-	pF
HCT TYPES								
Propagation Delay, Clock to Output (Figure 1)	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	37	46	56	ns
Propagation Delay, Clock to Q	t_{PLH}, t_{PHL}	-	5	15	-	-	-	ns
Output Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	15	19	22	ns
Propagation Delay, $\overline{MR}$ to Output (Figure 2)	t_{PHL}	C_L = 50pF	4.5	-	40	50	60	ns
Input Capacitance	C_{IN}	-	-	-	10	10	10	pF
Maximum Clock Frequency	f_{MAX}	-	5	50	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C_{PD}	-	5	60	-	-	-	pF

NOTES:

4. C_{PD} is used to determine the dynamic power consumption, per gate.
5. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

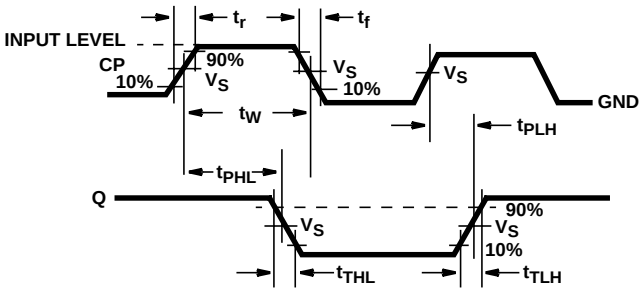


FIGURE 1. CLOCK PREREQUISITE TIMES AND PROPAGATION AND OUTPUT TRANSITION TIMES

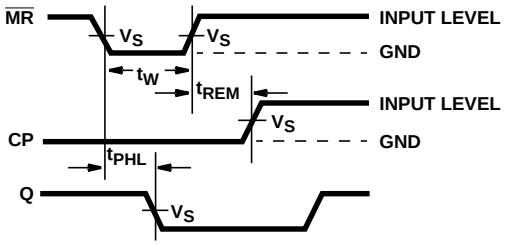


FIGURE 2. MASTER RESET PREREQUISITE TIMES AND PROPAGATION DELAYS

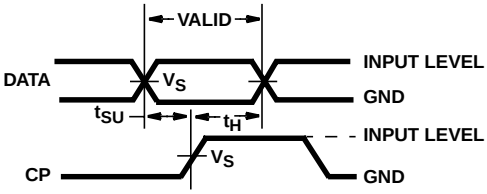


FIGURE 3. DATA PREREQUISITE TIMES

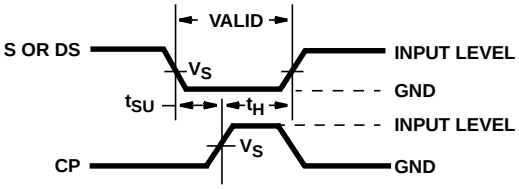
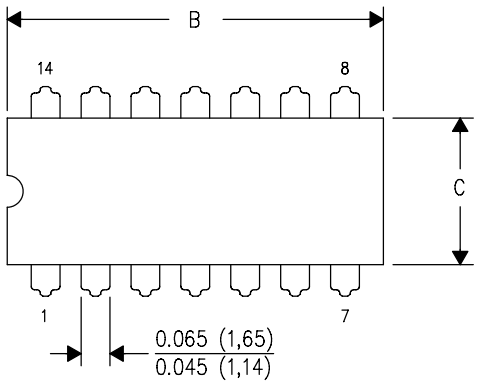


FIGURE 4. PARALLEL LOAD OR SHIFT-LEFT/SHIFT-RIGHT PREREQUISITE TIMES

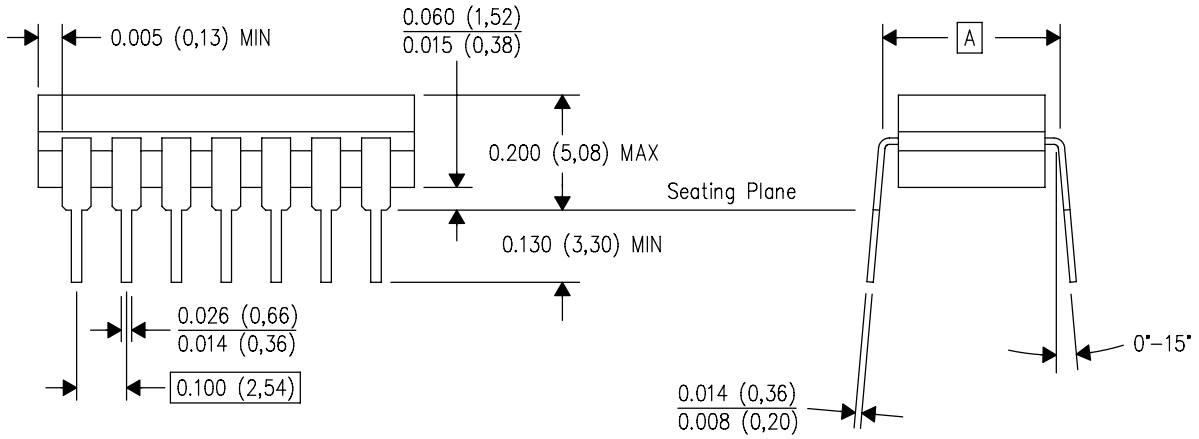
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



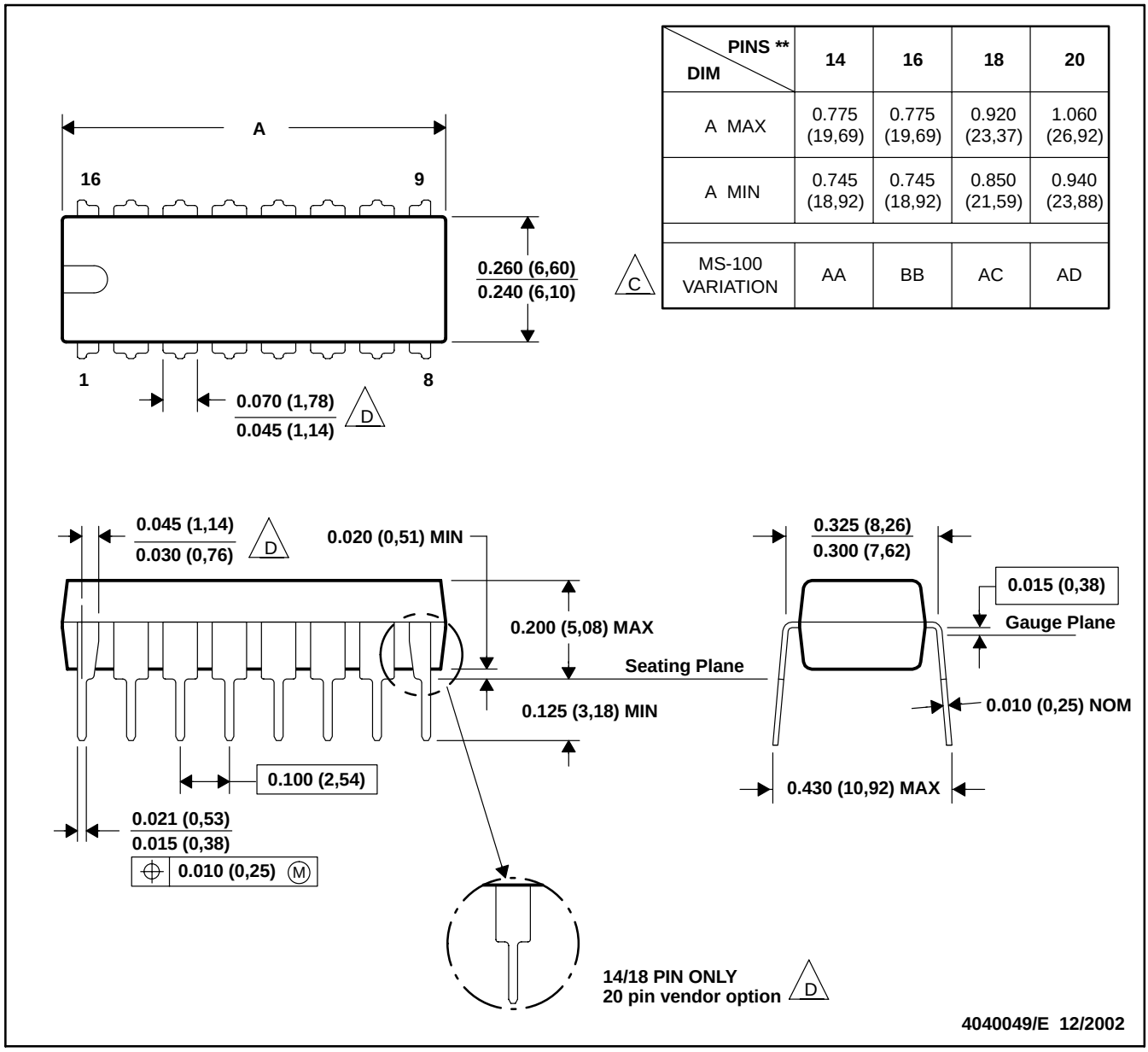
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

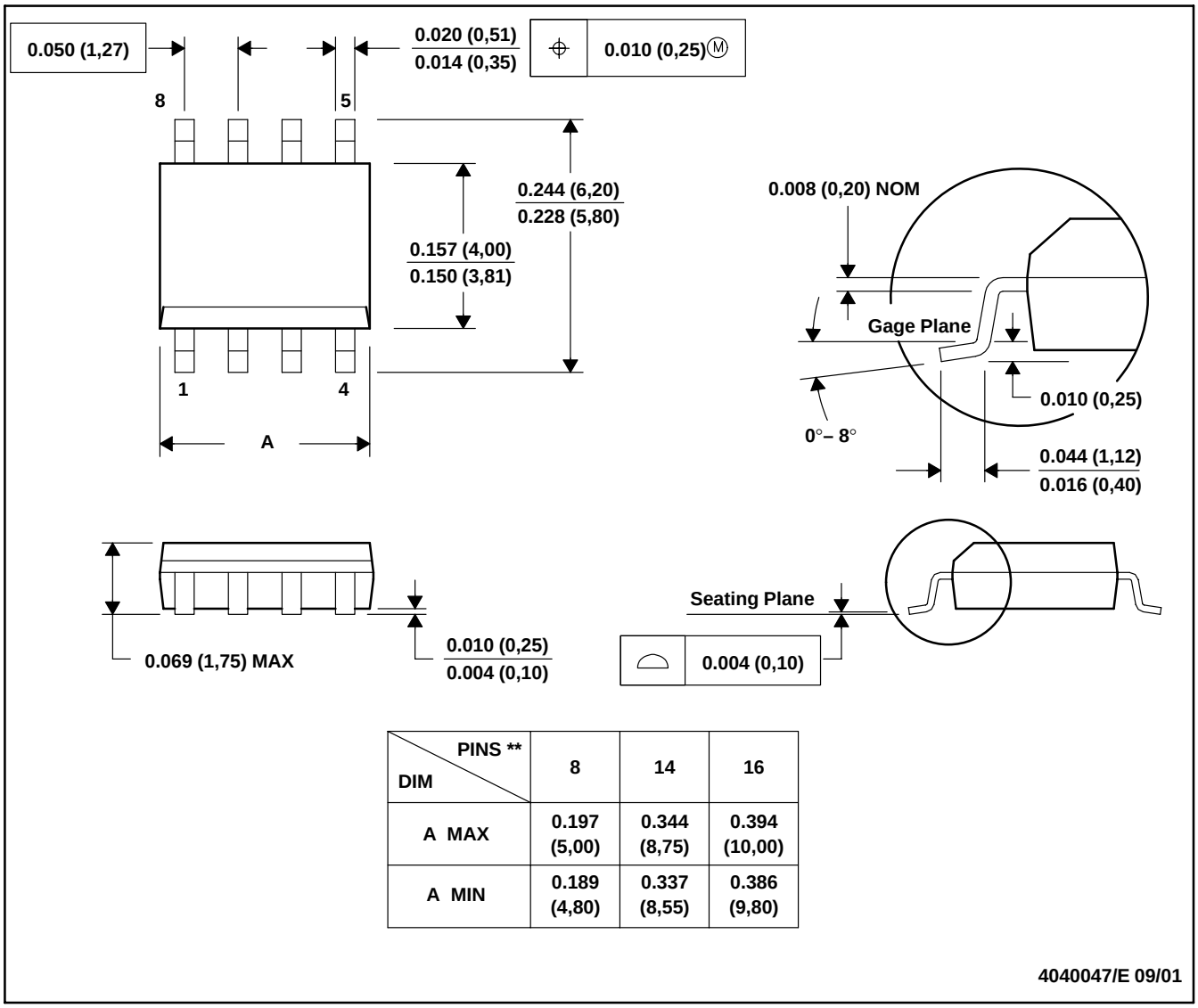
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

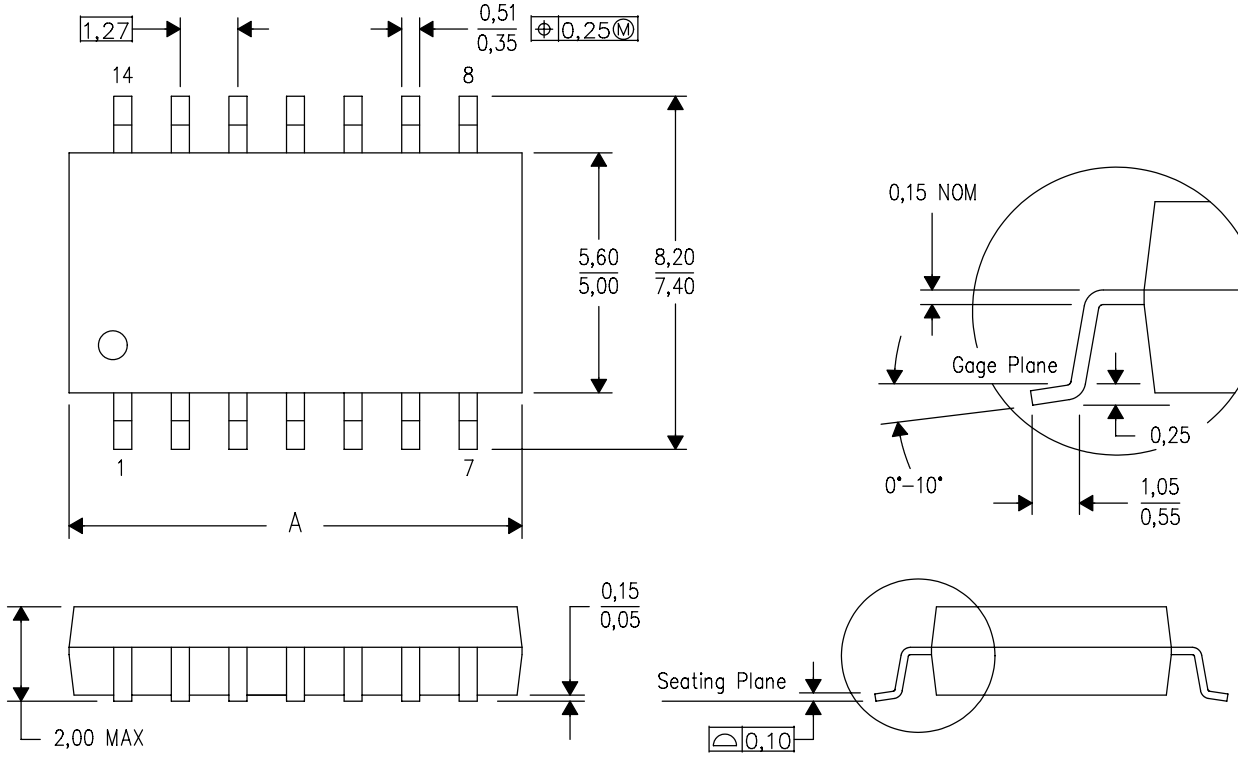
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



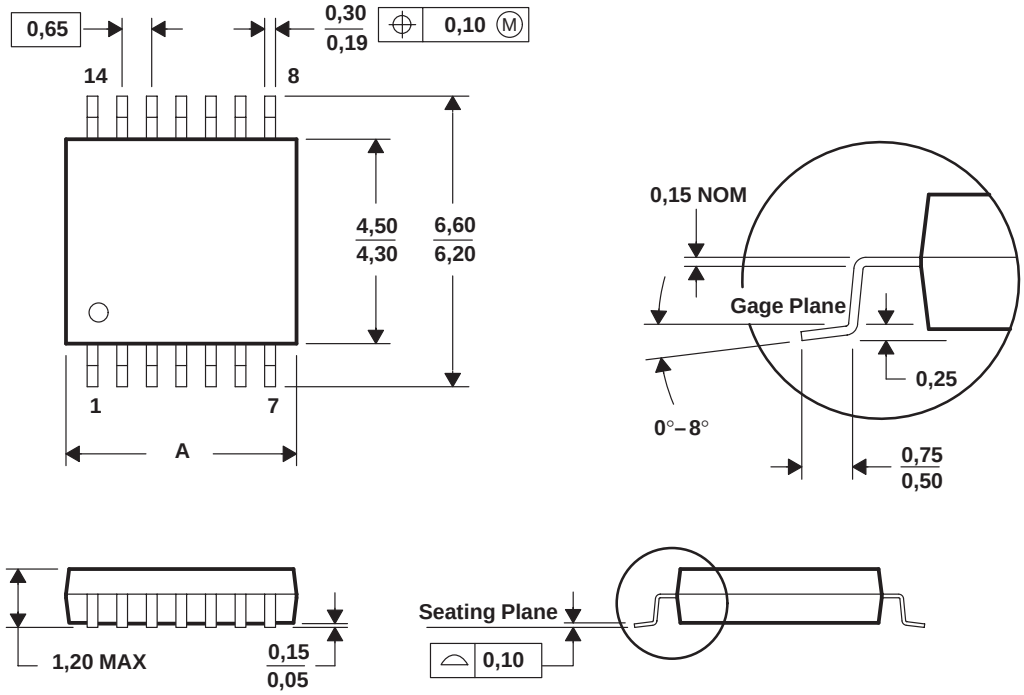
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

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