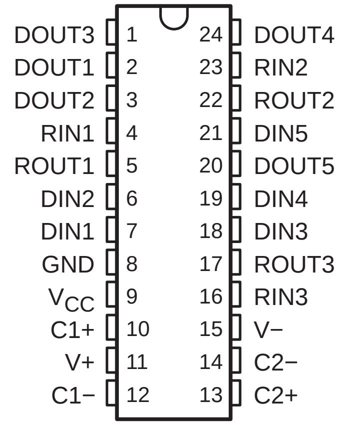
- **ESD Protection for RS-232 I/O Pins**
  - **±15 kV − Human-Body Model**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates at 5-V V_{CC} Supply**
- **Operates Up To 120 kbit/s**
- **External Capacitors . . . 4 × 0.1 μF**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

DB OR DW PACKAGE
(TOP VIEW)



description/ordering information

The MAX207 consists of five line drivers, three line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The devices operate at data signaling rates up to 120 kbit/s and a maximum of 30-V/μs driver output slew rate.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC (DW)	Tube of 25	MAX207CDW	MAX207C
		Reel of 2000	MAX207CDWR	
	SSOP (DB)	Reel of 2000	MAX207CDBR	MA207C
−40°C to 85°C	SOIC (DW)	Tube of 25	MAX207IDW	MAX207I
		Reel of 2000	MAX207IDWR	
	SSOP (DB)	Reel of 2000	MAX207IDBR	MB207I

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Function Tables

EACH DRIVER

INPUT D_{IN}	OUTPUT D_{OUT}
L	H
H	L

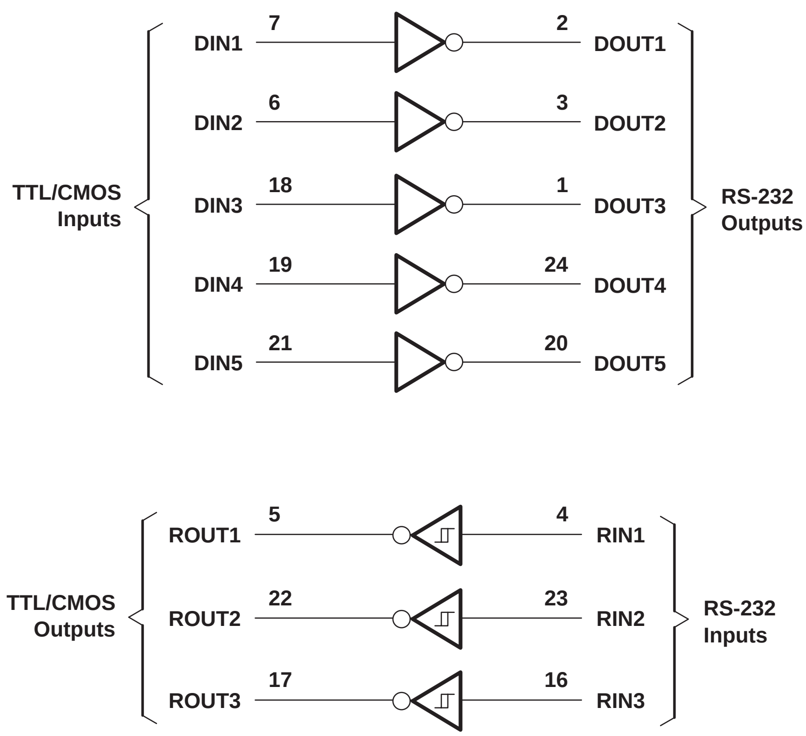
H = high level, L = low level

EACH RECEIVER

INPUT R_{IN}	OUTPUT R_{OUT}
L	H
H	L
Open	H

H = high level, L = low level, Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.3 V to 6 V
Positive charge pump voltage range, V+ (see Note 1) . . . . V_{CC} − 0.3 V to 14 V
Negative charge pump voltage range, V− (see Note 1) . . . . −14 V to 0.3 V
Input voltage range, V_I: Drivers . . . . −0.3 V to V+ + 0.3 V
Receivers . . . . ±30 V
Output voltage range, V_O: Drivers . . . . V− − 0.3 V to V+ + 0.3 V
Receivers . . . . −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: D_{OUT} . . . . Continuous
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package . . . . 63°C/W
DW package . . . . 46°C/W
Operating virtual junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 4)

			MIN	NOM	MAX	UNIT
	Supply voltage		4.5	5	5.5	V
V_{IH}	Driver high-level input voltage	D_{IN}	2			V
V_{IL}	Driver low-level input voltage	D_{IN}			0.8	V
V_I	Driver input voltage	D_{IN}	0		5.5	V
V_I	Receiver input voltage		−30		30	V
T_A	Operating free-air temperature	MAX207C	0		70	°C
T_A	Operating free-air temperature	MAX207I	−40		85	°C

NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5 V, T_A = 25°C		11	20	mA

NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = GND	5	9		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3 kΩ to GND,	D_{IN} = V_{CC}	−5	−9		V
I_{IH}	High-level input current	V_I = V_{CC}			15	200	μA
I_{IL}	Low-level input current	V_I at 0 V			−15	−200	μA
I_{OS}‡	Short-circuit output current	V_{CC} = 5.5 V,	V_O = 0 V		±10	±60	mA
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300			Ω

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate	C_L = 50 to 1000 pF, One D_{OUT} switching,	R_L = 3 kΩ to 7 kΩ, See Figure 1	120			kbit/s
t_{PLH} (D)	Propagation delay time, low- to high-level output	C_L = 2500 pF, all drivers loaded,	R_L = 3 kΩ, See Figure 1		2		μs
t_{PHL} (D)	Propagation delay time, high- to low-level output	C_L = 2500 pF, all drivers loaded,	R_L = 3 kΩ, See Figure 1		2		μs
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	C_L = 50 pF to 1000 pF V_{CC} = 5 V	R_L = 3 kΩ to 7 kΩ,	3	6	30	V/μs

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 μF at V_{CC} = 5 V ± 0.5 V.

ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
D_{OUT}, R_{IN}	Human-Body Model	±15	kV

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	3.5	V_{CC}−0.4 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

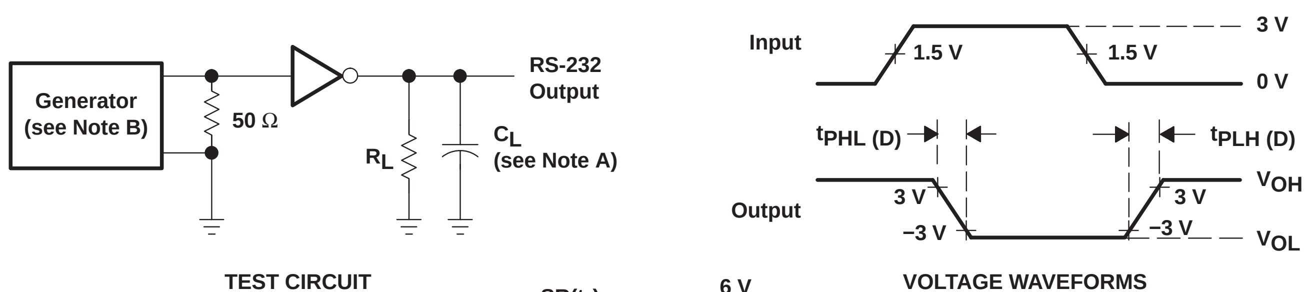
† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF		0.5	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF		0.5	10	µs
$t_{sk(p)}$	Pulse skew‡			300		ns

† All typical values are at V_{CC} = 5 V, and T_A = 25°C.
‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.1 µF, at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION

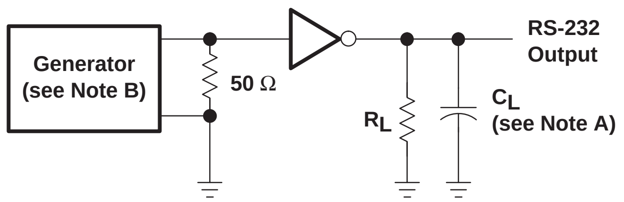


$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)}\ or\ t_{PLH\ (D)}}$$

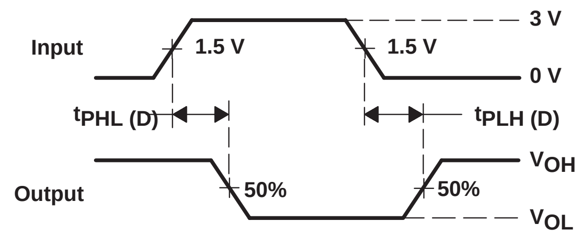
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 1. Driver Slew Rate

PARAMETER MEASUREMENT INFORMATION



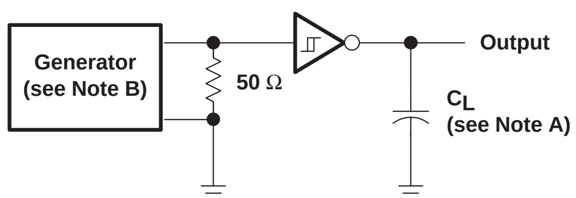
TEST CIRCUIT



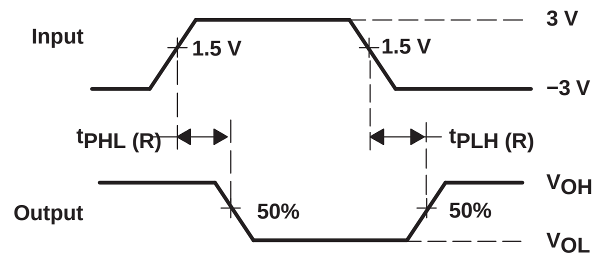
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 2. Driver Pulse Skew



TEST CIRCUIT

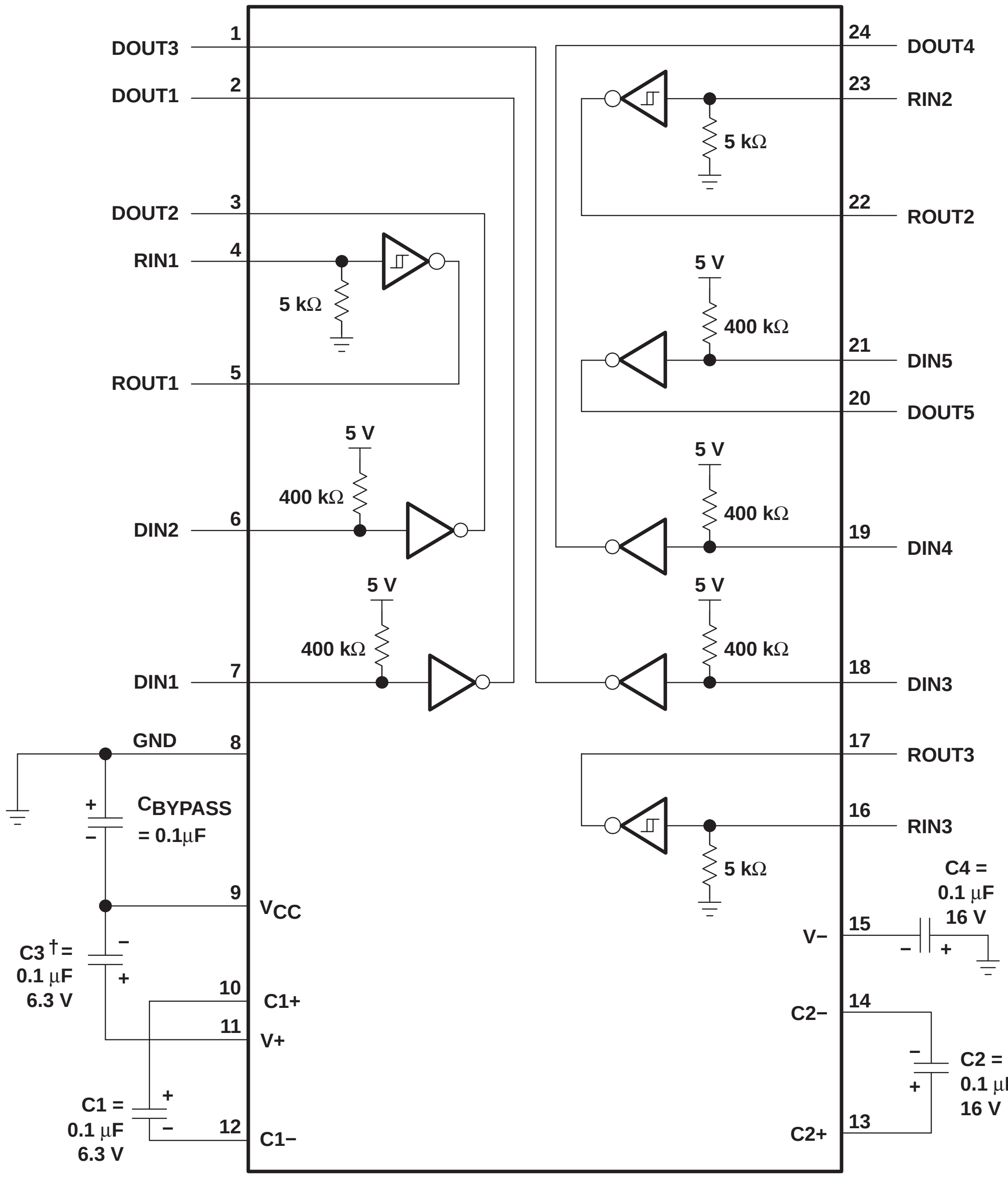


VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

capacitor selection

The capacitor type used for C1−C4 is not critical for proper operation. The MAX207 requires 0.1-μF capacitors, although capacitors up to 10 μF can be used without harm. Ceramic dielectrics are suggested for the 0.1-μF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V−.

Use larger capacitors (up to 10 μF) to reduce the output impedance at V+ and V−.

Bypass V_{CC} to ground with at least 0.1 μF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1−C4).

ESD protection

TI MAX207 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV when powered down.

ESD test conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

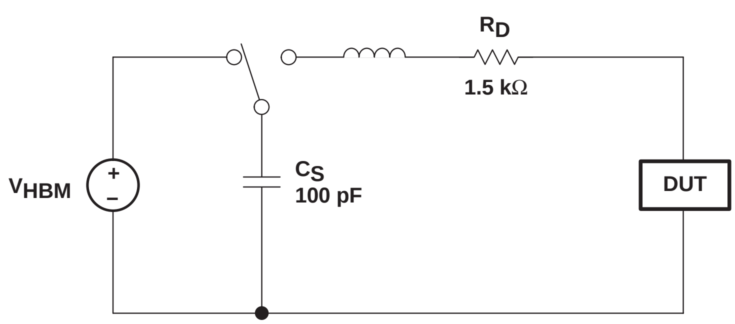


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION

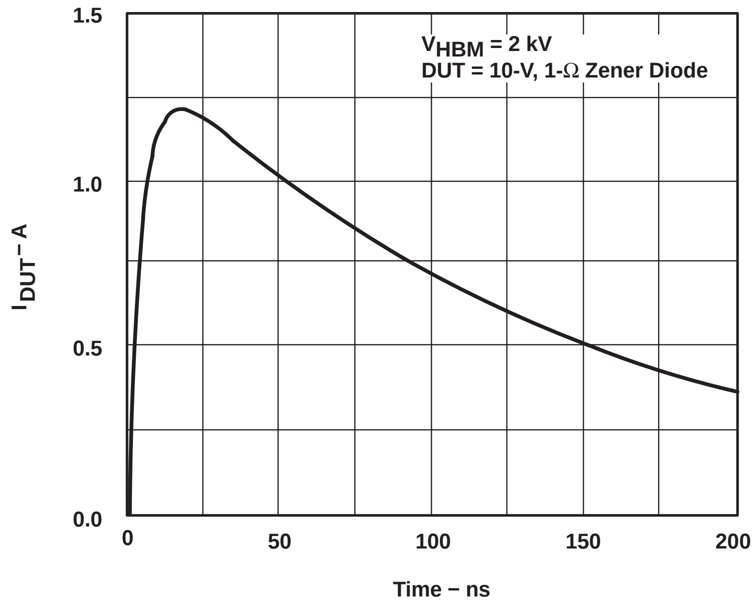


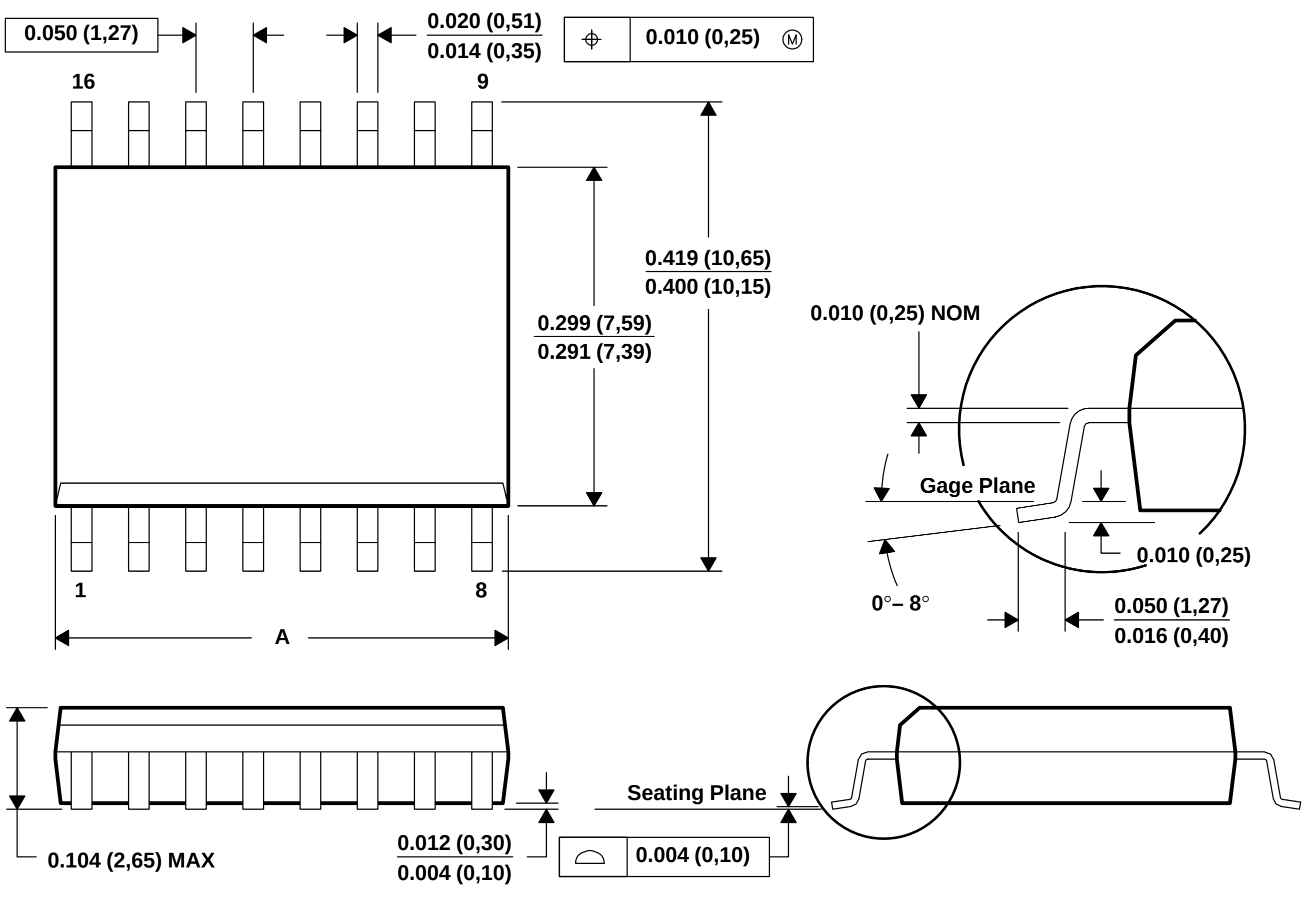
Figure 6. Typical HBM Current Waveform

Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



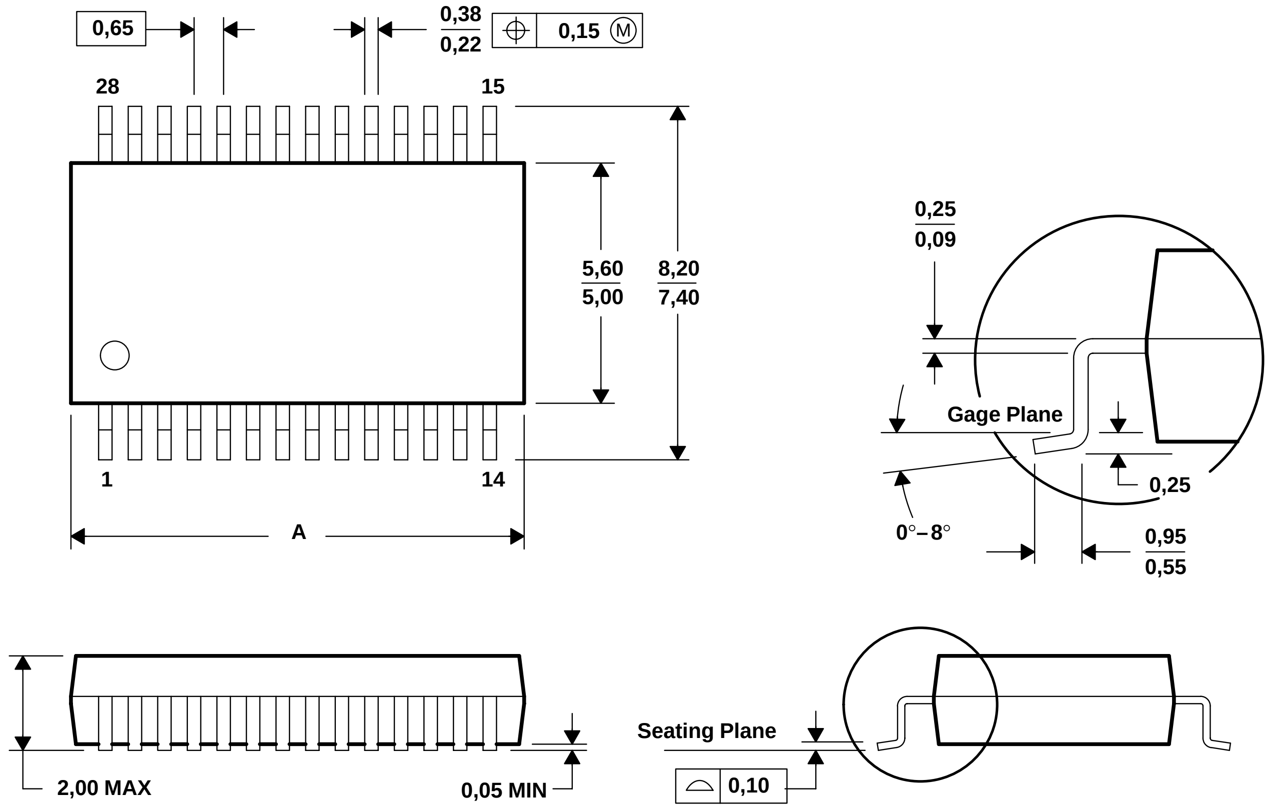
DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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