6-A Output, D-CAP+™ Mode, Synchronous Step-Down, Integrated-FET Converter for DDR Memory Termination

Check for Samples: TPS53317

FEATURES

- **TI proprietary Integrated MOSFET and Packaging Technology**
- **Supports DDR Memory Termination with up to 6-A Continuous Output Source or Sink Current**
- **External Tracking**
- **Minimum External Components Count**
- **1-V to 6-V Conversion Voltage**
- **D-CAP+™ Mode Architecture**
- **Supports All MLCC Output Capacitors and SP/POSCAP**
- **Selectable SKIP Mode or Forced CCM**
- **Optimized Efficiency at Light and Heavy Loads**
- **Selectable 600-kHz or 1-MHz Switching Frequency**
- **Selectable Overcurrent Limit (OCL)**
- **Overvoltage, Over-Temperature and Hiccup Undervoltage Protection**
- **Adjustable Output Voltage from 0.6 V to 2 V**
- **3.5 mm × 4 mm, 20-Pin QFN Package**

APPLICATIONS

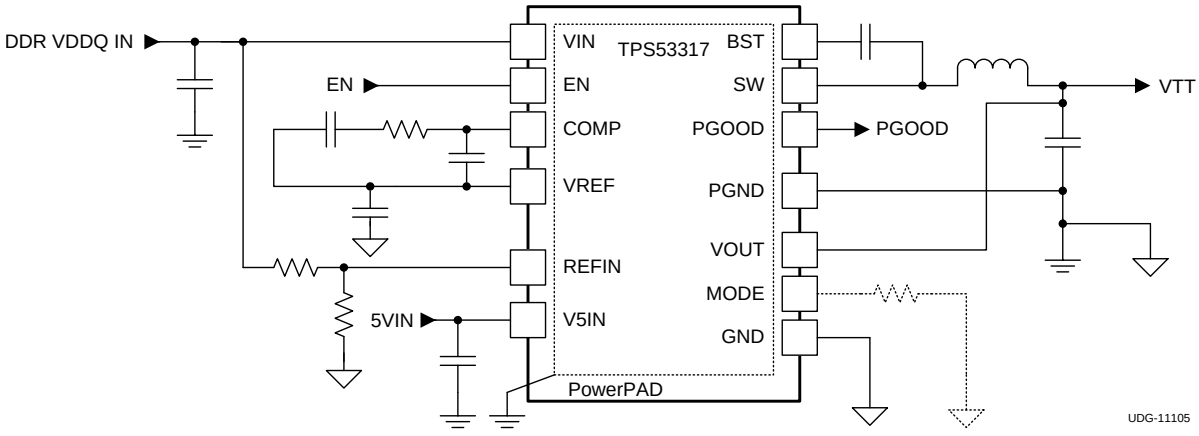
- **Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, and DDR4**
- **VTT Termination**
- **Low-Voltage Applications for 1-V to 6-V Input Rails**

DESCRIPTION

The TPS53317 is a FET-integrated synchronous buck regulator designed mainly for DDR termination. It can provide a regulated output at ½ V_{DDQ} with both sink and source capability. The TPS53317 employs D-CAP+™ mode operation that provides ease of use, low external component count and fast transient response. It can also be used for other POL regulation applications requiring up to 6 A. In addition, the TPS53317 supports full, 6-A, output sinking current capability with tight voltage regulation.

The TPS53317 features two switching frequency settings (600 kHz and 1 MHz), integrated droop support, external tracking capability, pre-bias startup, output soft discharge, integrated bootstrap switch, power good function, V5IN pin UVLO protection, and supports both ceramic and SP/POSCAP capacitors. It supports input voltages up to 6.0 V, and output voltages adjustable from 0.6 V to 2.0 V.

The TPS53317 is available in the 3.5 mm by 4 mm, 20-pin QFN package (Green RoHs compliant and Pb free) with TI proprietary Integrated MOSFET and packaging technology and is specified from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP+ is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERING NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
-40°C to 85°C	Plastic QFN (RGB)	TPS53317RGBR	20	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS53317RGBT	20	Mini reel	250	

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53317 RGB 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	35.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	39.6	
θ_{JB}	Junction-to-board thermal resistance(4)	12.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	12.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	3.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage range	VIN, V5IN, BST (with respect to SW)	–0.3	7.0	V
	BST	–0.3	14.0	
	SW	–2	7	
	EN	–0.3	7	
	MODE, REFIN	–0.3	3.6	
	VOUT	–1	3.6	
Output voltage range	COMP, VREF	–0.3	3.6	V
	PGOOD	–0.3	7.0	
	PGND	–0.3	0.3	
Junction temperature	T_J	–40	150	
Storage temperature	T_{stg}	–55	150	˚C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	˚C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		VALUE			UNIT
		MIN	NOM	MAX	
Input voltage range	VIN, EN, BST (with respect to SW)	–0.1		6.5	V
	V5IN	4.5		6.5	
	BST	–0.1		13.5	
	SW	–1.0		6.5	
	VOUT, MODE, REFIN	–0.1		3.5	
Output voltage range	COMP	–0.1		3.5	
	VREF		2		V
	PGOOD	–0.1		6.5	
	PGND	–0.1		0.1	
Operating temperature range, T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V_{V5IN} = 5.0 V, PGND = GND (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY: VOLTAGE, CURRENTS AND 5 V UVLO						
I_{VINSD}	VIN shutdown current	EN = 'LO'		0.02	5	µA
V_{V5IN}	V5IN supply voltage	V5IN voltage range	4.5	5.0	6.5	V
I_{V5IN}	V5IN supply current	EN ='HI', V5IN supply current, f_{SW} = 600 kHz		1.1	2	mA
I_{V5INSD}	V5IN shutdown current	EN = 'LO', V5IN shutdown current		0.2	7.0	µA
V_{V5UVLO}	V5IN UVLO	Ramp up; EN = 'HI'	4.20	4.37	4.50	V
$V_{V5UVHYS}$	V5IN UVLO hysteresis	Falling hysteresis		440		mV
$V_{VREFUVLO}$	REF UVLO(1)	Rising edge of VREF, EN = 'HI'		1.8		V
$V_{VREFUVHYS}$	REF UVLO hysteresis(1)			100		mV
$V_{POR5VFILT}$	Reset	OVP latch is reset by V5IN falling below the reset threshold	1.5	2.3	3.1	V
VOLTAGE FEEDBACK LOOP: VREF, VOUT, AND VOLTAGE GM AMPLIFIER						
V_{OUTTOL}	Output voltage accuracy	V_{REFIN} = 1 V, No droop	–1%	0%	1%	
		V_{REFIN} = 0.6 V, No droop	–1%	0%	1%	
V_{VREF}	VREF	I_{VREF} = 0 µA	1.98	2.00	2.02	V
		I_{VREF} = 50 µA	1.975	2.000	2.025	
I_{REFSNK}	VREF sink current	V_{VREF} = 2.05 V		2.5		mA
g_M	Transconductance			1.00		mS
V_{CM}	Common mode input voltage range(1)		0		2	V
V_{DM}	Differential mode input voltage		0		80	mV
$I_{COMPSNK}$	COMP pin maximum sinking current	V_{COMP} = 2 V, (V_{REFIN} - V_{OUT}) = 80 mV		80		µA
$I_{COMPSRC}$	COMP pin maximum sourcing current	V_{COMP} = 2 V		-80		µA
V_{OFFSET}	Input offset voltage	T_A = 25°C		0		mV
R_{DSCH}	Output voltage discharge resistance			42		Ω
f_{-3dbVL}	–3dB Frequency(1)		4.5	6.0	7.5	MHz
CURRENT SENSE: CURRENT SENSE AMPLIFIER, OVERCURRENT AND ZERO CROSSING						
A_{CSINT}	Internal current sense gain	Gain from the current of the low-side FET to PWM comparator when PWM = "OFF"	43	53	57	mV/A
I_{OCL}	Positive overcurrent limit (valley)			7.6		A
$I_{OCL(neg)}$	Negative overcurrent limit (valley)			–9.3		A
V_{ZXOFF}	Zero crossing comp internal offset			0		mV
PROTECTION: OVP, UVP, PGOOD, and THERMAL SHUTDOWN						
V_{PGDLL}	PGOOD deassert to lower (PGOOD → Low)	Measured at the VOUT pin wrt/ V_{REFIN}		84%		
$V_{PGHYSHL}$	PGOOD high hysteresis			8%		
V_{PGDLH}	PGOOD de-assert to higher (PGOOD → Low)	Measured at the VOUT pin wrt/ V_{REFIN}		116%		
$V_{PGHYSHH}$	PGOOD high hysteresis			-8%		
$V_{INMINPG}$	Minimum VIN voltage for valid PGOOD	Measured at the VIN pin with a 2-mA sink current on PGOOD pin. V5IN is grounded here.(2)	0.9	1.3	1.5	V
V_{OVP}	OVP threshold	Measured at the VOUT pin wrt/ V_{REFIN}	117%	120%	123%	
V_{UVP}	UVP threshold	Measured at the VOUT pin wrt/ V_{REFIN}, device latches OFF, begins soft-stop	65%	68%	71%	
TH_{SD}	Thermal shutdown(1)	Latch off controller, attempt soft-stop.		145		°C
$TH_{SD(hys)}$	Thermal Shutdown hysteresis(1)	Controller re-starts after temperature has dropped		10		°C

(1) Ensured by design, not production tested.
(2) If V5IN is higher than 1.5 V, PGOOD is valid regardless of the voltage applied at VIN. This is based on bench testing.

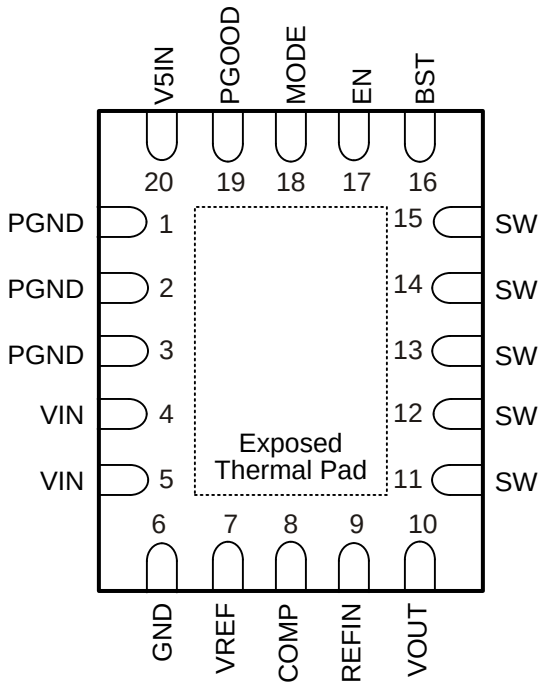
ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V_{V5IN} = 5.0 V, PGND = GND (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DRIVERS: BOOT STRAP SWITCH						
$R_{DSONBST}$	Internal BST switch on-resistance	I_{BST} = 10 mA, T_A = 25°C			10	Ω
I_{BSTLK}	Internal BST switch leakage current	V_{BST} = 14 V, V_{SW} = 7 V			1	µA
TIMERS: ON-TIME, MINIMUM OFF-TIME, SS, AND I/O TIMINGS						
$t_{ONESHOTC}$	PWM one-shot (3)	V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 1 MHz		210		ns
		V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 600 kHz		310		
$t_{MIN(off)}$	Minimum OFF time	V_{VIN} = 5 V, V_{VOUT} = 1.05 V, f_{SW} = 1 MHz, DRVL on, SW = PGND, V_{VOUT} < V_{REFIN}		270		ns
$t_{INT(SS)}$	Soft-start time	From V_{OUT} ramp starting to V_{OUT} =95%, default setting		1.6		ms
$t_{INT(SSDLY)}$	Internal soft-start delay time	From V_{VREF} = 2 V to V_{OUT} ramp starting		260		µs
t_{PGDDLY}	PGOOD startup delay time	External tracking		8		ms
$t_{PGDPDLYH}$	PGOOD high propagation delay time	50 mV over drive, rising edge	0.8	1	1.2	ms
$t_{PGDPDLYL}$	PGOOD low propagation delay time	50 mV over drive, falling edge		10		µs
t_{OVPDLY}	OVP delay time	Time from the VOUT pin out of +20% of REFIN to OVP fault		10		µs
$t_{UVDLYEN}$	Undervoltage fault enable delay	Time from EN_INT going high to undervoltage fault is ready		2		ms
		External tracking from VOUT ramp starts		8		
t_{UVPDLY}	UVP delay time	Time from the VOUT pin out of –32% of REFIN to UVP fault		256		µs
LOGIC PINS: I/O VOLTAGE AND CURRENT						
V_{PGDPD}	PGOOD pull-down voltage	PGOOD low impedance, I_{SINK} = 4 mA, V_{V5IN} = 4.5 V			0.3	V
I_{PGDLKG}	PGOOD leakage current	PGOOD high impedance, forced to 5.5 V	–1	0	1	µA
V_{ENH}	EN logic high	EN, VCCP logic	2			V
V_{ENL}	EN logic low	EN, VCCP logic			0.5	V
I_{EN}	EN input current				1	µA
V_{MODETH}	MODE threshold voltage (4)	Threshold 1	80	130	180	mV
		Threshold 2	200	250	300	
		Threshold 3	370	420	470	
		Threshold 4	1.765	1.800	1.850	V
I_{MODE}	MODE current			15		µA

(3) Ensured by design, not production tested.
(4) See Table 1 for descriptions of MODE parameters.

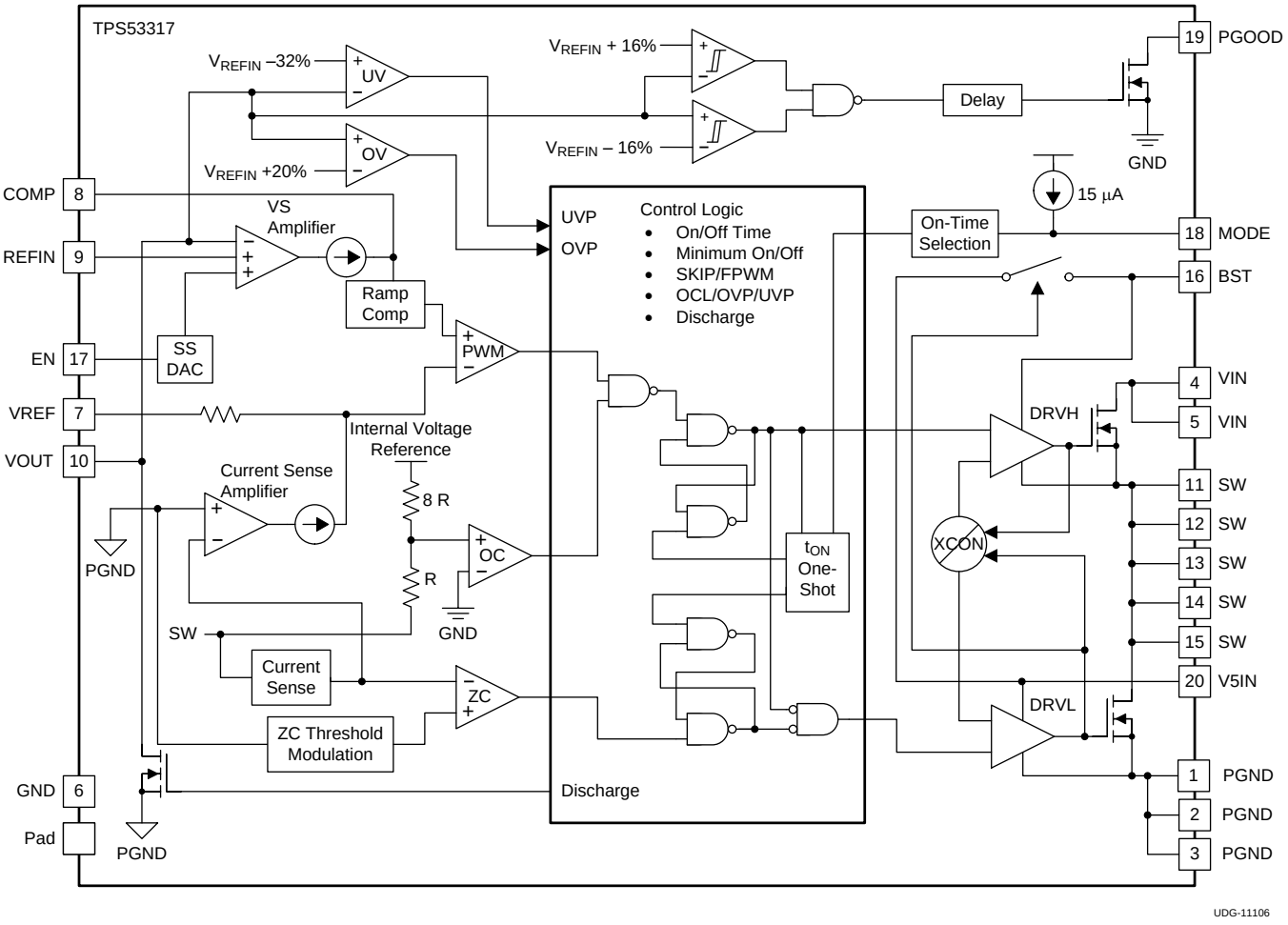
TPS53317
RGB PACKAGE
(Top View)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BST	16	I	Power supply for internal high-side gate driver. Connect a 0.1-µF bootstrap capacitor between this pin and the SW pin. A series boot resistor is optional.
COMP	8	O	Connect an R-C-C network between this pin and VREF for loop compensation.
EN	17	I	Enable pin (3.3-V logic compatible).
GND	6	–	Analog ground.
MODE	18	I	Allows selection of different operation modes. (See Table 1)
PGND	1	G	Power ground.
	2		
	3		
PGOOD	19	O	Open drain power good output. Connect pull-up resistor.
REFIN	9	I	External tracking reference input. Apply voltage between 0.6 V to 2.0 V. For non-tracking mode, connect REFIN to VREF via resistor divider.
SW	11	I/O	Switching node output.
	12		
	13		
	14		
	15		
V5IN	20	I	5-V power supply for analog circuits and gate drive.
VIN	4	I	Power supply input pin.
	5		
VOUT	10	I	Output voltage monitor input pin.
VREF	7	O	2.0-V reference output. Connect a 0.22-µF ceramic capacitor to GND.

FUNCTIONAL BLOCK DIAGRAM



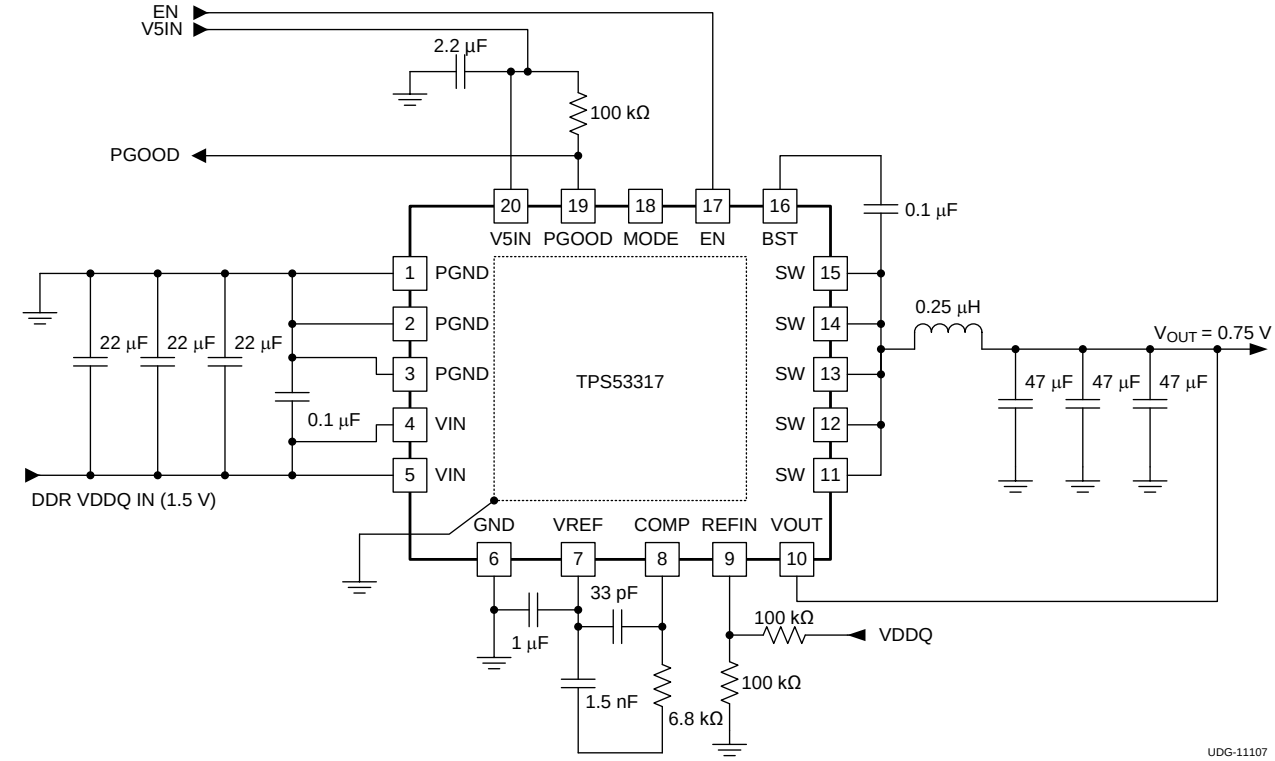


Figure 1. Typical DDR Memory Termination Regulator Circuit (Non-droop Configuration)

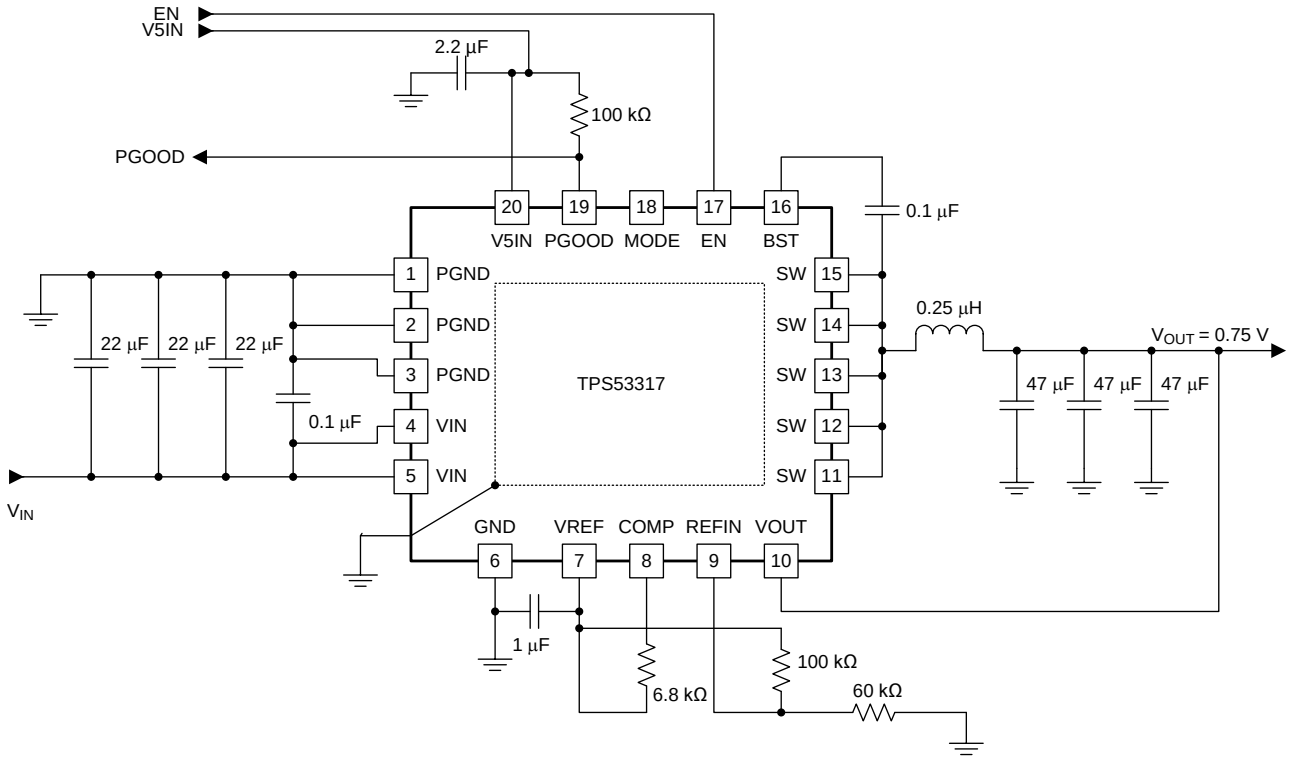


Figure 2. Application Using Droop Configuration

APPLICATION INFORMATION

Functional Overview

The TPS53317 is a D-CAP+™ mode adaptive on-time converter. Integrated high-side and low-side FET supports a maximum of 6-A DC output current. The converter automatically runs in discontinuous conduction mode (DCM) to optimize light-load efficiency. Multiple switching frequencies are provided to enable optimization of the power train for the cost, size and efficiency requirements of the design (see Table 1).

In adaptive on-time converters, the controller varies the on-time as a function of input and output voltage to maintain a nearly constant frequency during steady-state conditions. In conventional constant on-time converters, each cycle begins when the output voltage crosses to a fixed reference level. However, in the TPS53317, the cycle begins when the current feedback reaches an error voltage level which is the amplified difference between the reference voltage and the feedback voltage.

PWM Operation

Referring to Figure 3, in steady state, continuous conduction mode, the converter operates in the following way.

Starting with the condition that the top FET is off and the bottom FET is on, the current feedback (V_{CS}) is higher than the error amplifier output (V_{COMP}). V_{CS} falls until it hits V_{COMP}, which contains a component of the output ripple voltage. V_{CS} is not directly accessible by measuring signals on pins of TPS53317. The PWM comparator senses where the two waveforms cross and triggers the on-time generator.

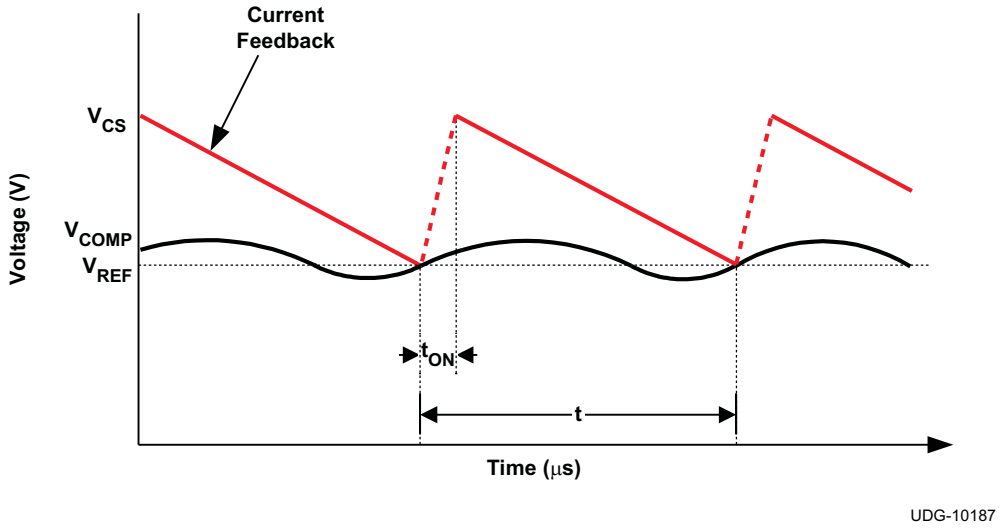


Figure 3. D-CAP+™ Mode Basic Waveforms

The current feedback is an amplified and filtered version of the voltage between PGND and SW during low-side FET on-time. The TPS53317 also provides a single-ended differential voltage (V_{OUT}) feedback to increase the system accuracy and reduce the dependence of circuit performance on layout.

PWM Frequency and Adaptive on Time Control

In general, the on-time (at the SW node) can be estimated by Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (1)$$

where

- f_{SW} is the frequency selected by the connection of the MODE pin

The on-time pulse is sent to the top FET. The inductor current and the current feedback rises to peak value. Each ON pulse is latched to prevent double pulsing. Switching frequency settings are shown in Table 1.

Non-Droop Configuration

The TPS53317 can be configured as a non-droop solution. The benefit of a non-droop approach is that load regulation is flat, therefore, in a system where tight DC tolerance is desired, the non-droop approach is recommended. For the Intel system agent application, non-droop is recommended as the standard configuration.

The non-droop approach can be implemented by connecting a resistor and a capacitor between the COMP and the VREF pins. The purpose of the type II compensation is to obtain high DC feedback gain while minimizing the phase delay at unity gain cross over frequency of the converter.

The value of the resistor (R_C) can be calculated using the desired unity gain bandwidth of the converter, and the value of the capacitor (C_C) can be calculated by knowing where the zero location is desired. The capacitor C_P is optional, but recommended. Its appropriate capacitance value can be calculated using the desired pole location.

Figure 4 shows the basic implementation of the non-droop mode using the TPS53317.

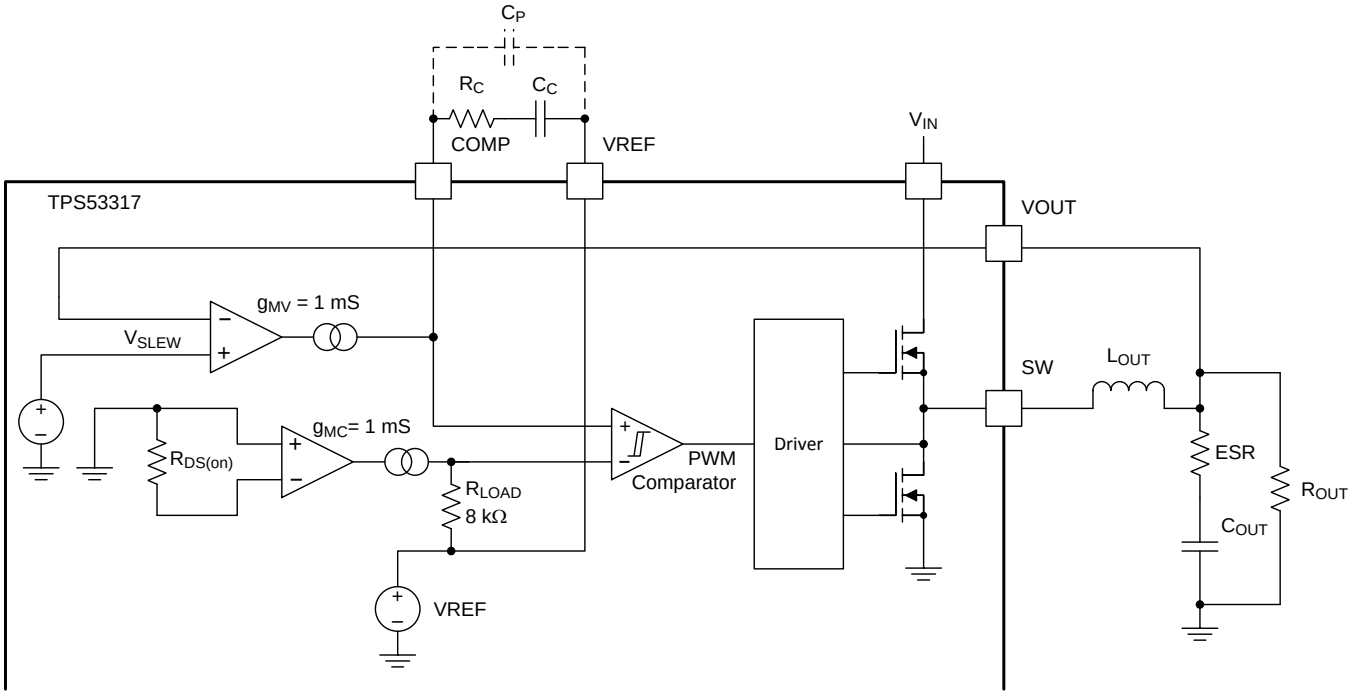


Figure 4. Non-Droop Mode Basic Implementation

Figure 5 shows shows the load regulation using non-droop configuration.

Figure 6 shows the transient response of TPS53317 using non-droop configuration, where C_{OUT} = 3 x 47 µF. The applied step load is from 0 A to 2 A.

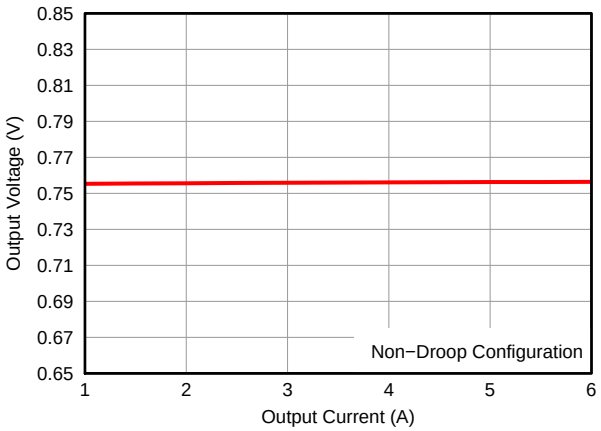


Figure 5. Load Regulation for 1.5-V Input, 0.75-V Output (Non-Droop Configuration)

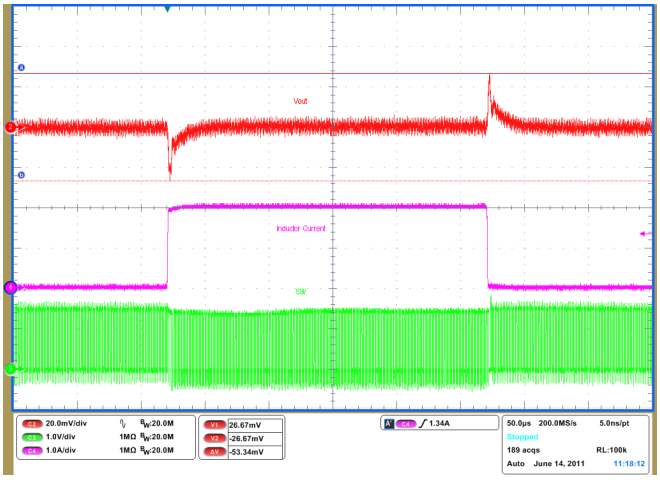


Figure 6. Non-Droop Configuration Transient Response
CH 2: V_{OUT} (20 mV/div)
CH 4: I_{OUT} (1 A/div)
CH 3: SW (1 V/div)

Droop Configuration

The terminology for droop is the same as *load line* or *voltage positioning* as defined in the Intel CPU V_{CORE} specification. Based on the actual tolerance requirement of the application, load-line set points can be defined to maximize either cost savings (by reducing output capacitors) or power reduction benefits.

Accurate droop voltage response is provided by the finite gain of the droop amplifier. The equation for droop voltage is shown in Equation 2.

$$V_{DROOP} = \frac{A_{CSINT} \times I_{OUT}}{R_{DROOP} \times g_M} \quad (2)$$

where

- low-side on-resistance is used as the current sensing element
- A_{CSINT} is a constant, which nominally is 53 mV/A.
- I_{OUT} is the DC current of the inductor, or the load current
- R_{DROOP} is the value of resistor from the COMP pin to the VREF pin
- g_M is the transconductance of the droop amplifier with nominal value of 1 mS

Equation 3 can be used to easily derive R_{DROOP} for any load line slope/droop design target.

$$R_{LOAD\_LINE} = \frac{V_{DROOP}}{I_{OUT}} = \frac{A_{CSINT}}{R_{DROOP} \times g_M} \quad \therefore \quad R_{DROOP} = \frac{A_{CSINT}}{R_{LOAD\_LINE} \times g_M} \quad (3)$$

Figure 7 shows the basic implementation of the droop mode using the TPS53317.

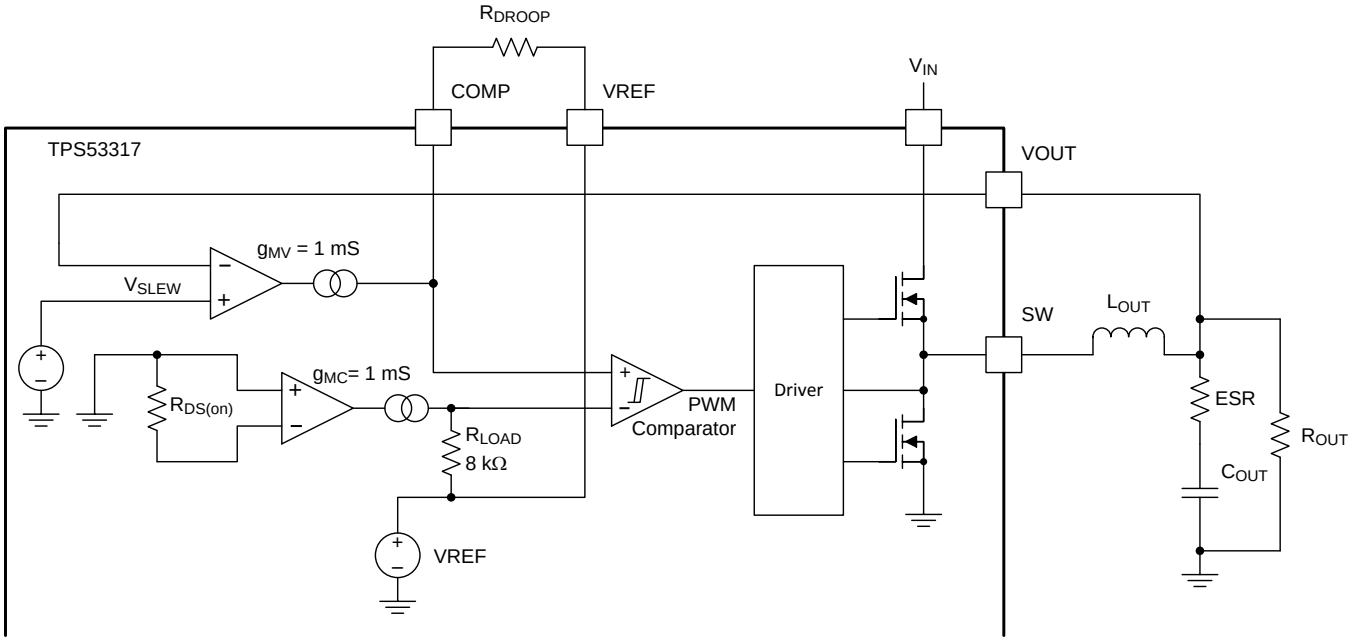


Figure 7. DROOP Mode Basic Implementation

The droop (voltage positioning) method was originally recommended to reduce the number of external output capacitors required. The effective transient voltage range is increased because of the active voltage positioning (see Figure 8).

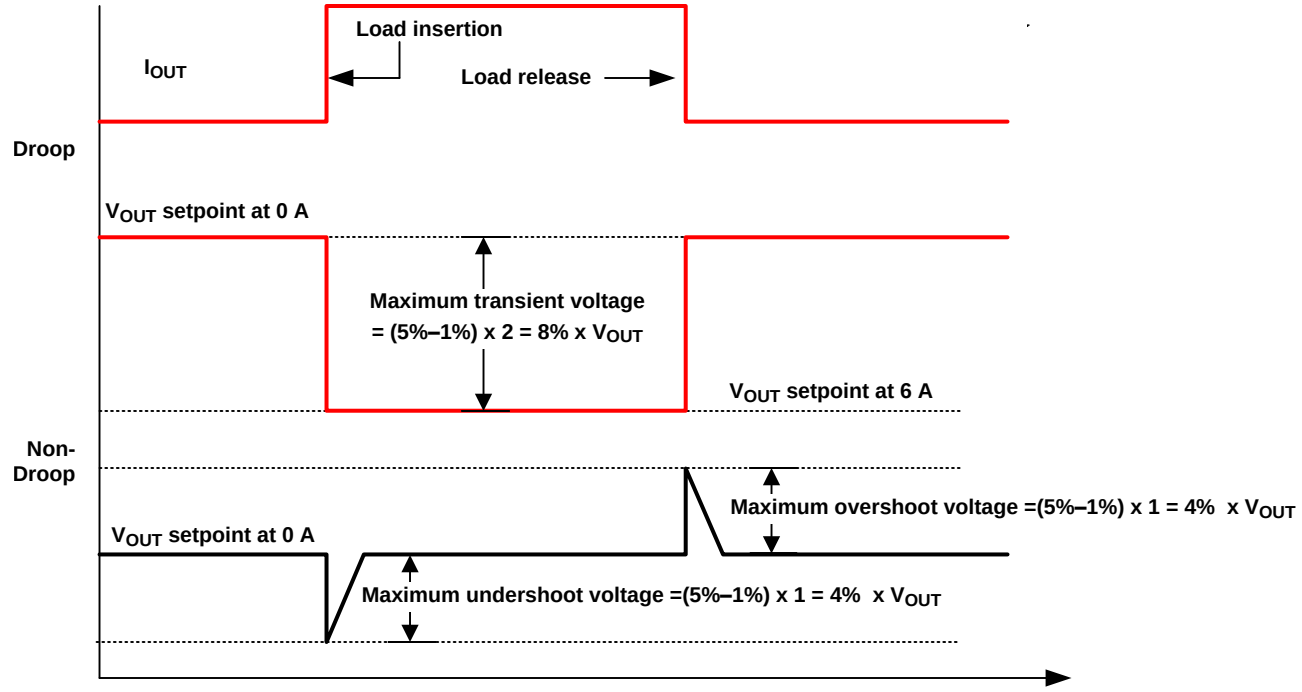


Figure 8. DROOP vs Non-DROOP in Transient Voltage Window

In applications where the DC and the AC tolerances are not separated, (meaning that there is no strict DC tolerance requirement) the droop method can be used.

Table 1. Mode Definitions

MODE	MODE RESISTANCE (kΩ)	LIGHT-LOAD POWER SAVING MODE	SWITCHING FREQUENCY (f_{SW})	OVERCURRENT LIMIT (OCL) VALLEY (A)
1	0	SKIP	600 kHz	7.6
2	12		600 kHz	5.4
3	22		1 MHz	5.4
4	33		1 MHz	7.6
5	47	PWM	600 kHz	7.6
6	68		600 kHz	5.4
7	100		1 MHz	5.4
8	OPEN		1 MHz	7.6

Figure 9 shows the load regulation of the 1.5-V rail using an R_{DROOP} value of 6.8 kΩ.

Figure 10 shows the transient response of the TPS53317 using droop configuration and C_{OUT} = 3 × 47 µF. The applied step load is from 0 A to 2 A.

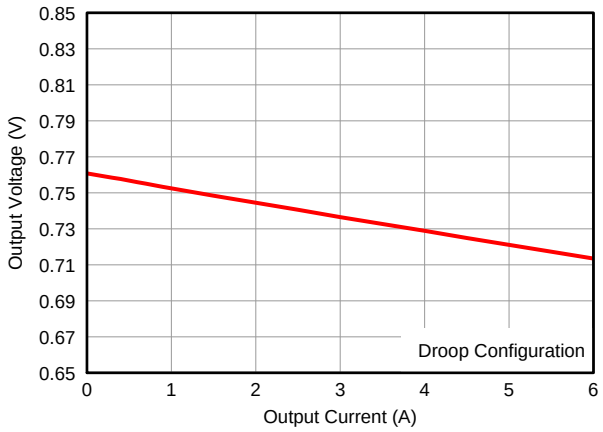


Figure 9. Load Regulation for 1.5-V Input, 0.75-V Output (Droop Configuration)

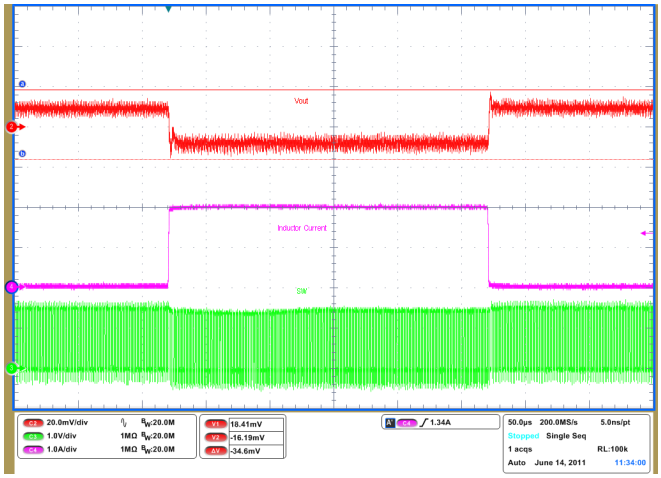


Figure 10. Droop Configuration Transient Response
CH 2: V_{OUT} (20 mV/div)
CH 4: I_{OUT} (1 A/div)
CH 3: SW (1 V/div)

Light-Load Power Saving Features

The TPS53317 has an automatic pulse-skipping mode to provide excellent efficiency over a wide load range. The converter senses inductor current and prevents negative flow by shutting off the low-side gate driver. This saves power by eliminating re-circulation of the inductor current. Further, when the bottom FET shuts off, the converter enters discontinuous mode, and the switching frequency decreases, thus reducing switching losses as well.

TPS53317 also provides a special light-load power saving feature, called ripple reduction. Essentially, it reduces the on-time in SKIP mode to effectively reduce the output voltage ripple associated with using an all MLCC capacitor output power stage design.

Power Sequences

Non-Tracking Startup

The TPS53317 can be configured for non-tracking application. When non-tracking is configured, output voltage is regulated to the REFIN voltage which taps off the voltage dividers from the 2-V reference voltage. Either the EN pin or the V5IN pin can be used to start up the device. The TPS53317 uses internal voltage servo DAC to provide a 1.6-ms soft-start time during soft-start initialization. (See Figure 12)

In a non-tracking application, the output voltage is determined by the resistive divider between the VREF pin and the REFIN pin.

$$V_{OUT} = V_{REF} \times \frac{R2}{R1 + R2} \quad (4)$$

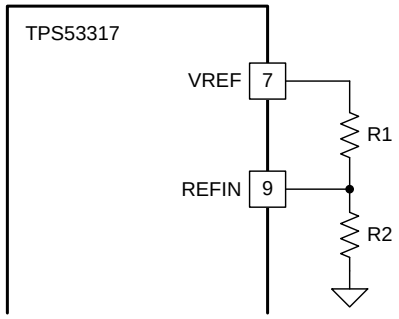


Figure 11. Non-Tracking Configuration

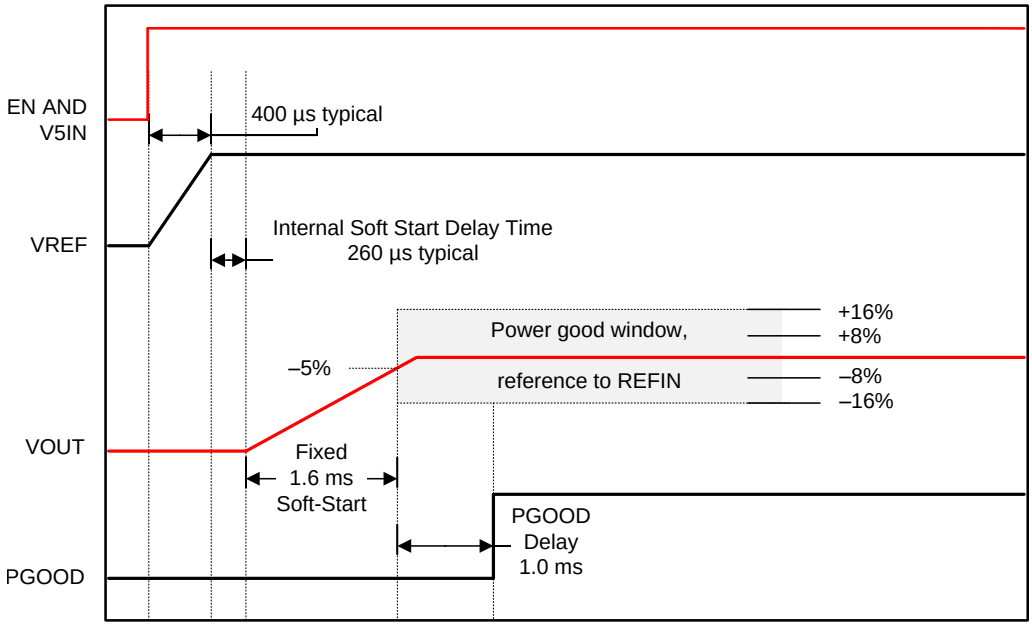


Figure 12. Non-Tracking Startup Timing

Tracking Startup

TPS53317 can also be configured for tracking application. When tracking configuration is desired, output voltage is also regulated to the REFIN voltage which comes from an external power source. In order for TPS53317 to differentiate between a non-tracking configuration or a tracking configuration, there is a minimum delay time of 260 µs required between the time when the EN pin or the V5IN pin is validated to the time when the REFIN pin voltage can be applied, in order for the TPS53317 to track properly (see Figure 15). The valid REFIN voltage range is between 0.6 V to 2 V.

In a tracking application, the output voltage should be one half of the VDDQ voltage. VDDQ can be VIN or it can be an additional voltage rail. Thus, R1= R2 both in Figure 13 and Figure 14.

$$V_{OUT} = ½ \times V_{VDDQ} \quad (5)$$

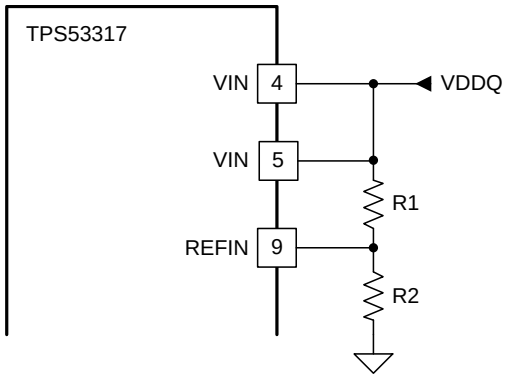


Figure 13. Tracking Configuration 1

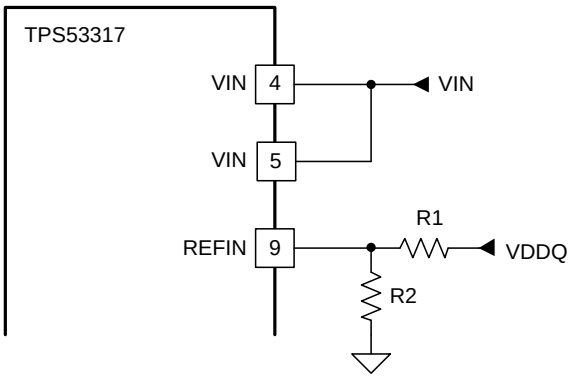


Figure 14. Tracking Configuration 2

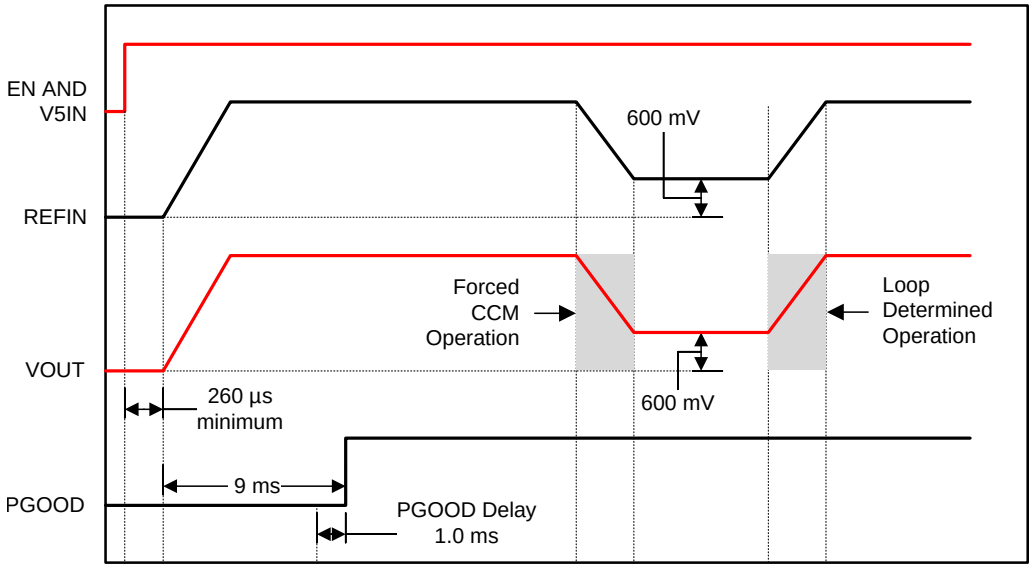


Figure 15. Tracking Startup Timing

Protection Features

The TPS53317 offers many features to protect the converter power train as well as the system electronics.

5-V Undervoltage Protection (UVLO)

The TPS53317 continuously monitors the voltage on the V5IN pin to ensure that the voltage level is high enough to bias the device properly and to provide sufficient gate drive potential to maintain high efficiency. The converter starts with approximately 4.3 V and has a nominal 440 mV of hysteresis. If the 5-V UVLO limit is reached, the converter transitions the phase node into an off function, and the converter remains in the off state until the device is reset by cycling 5 V until the 5-V POR is reached (2.3-V nominal). The power input does not have a UVLO function.

Power Good Signals

The TPS53317 has one open-drain *power good* (PGOOD) pin. During startup, there is a 1-ms power good high propagation delay. The PGOOD pin de-asserts as soon as the EN pin is pulled low or an undervoltage condition on V5IN or any other fault is detected.

Output Overvoltage Protection (OVP)

In addition to the power good function described above, the TPS53317 has additional OVP and UVP thresholds and protection circuits.

An OVP condition is detected when the output voltage is approximately 120% × V_{REFIN}. In this case, the converter de-asserts the PGOOD signals and performs the overvoltage protection function. During OVP, the low-side FET is always on before triggering a negative overcurrent. When a negative OC is also tripped, the low-side FET is no longer continuously on, and pulsed signals are generated to limit the negative inductor current. When the VOUT pin voltage drops below 400 mV, the low-side FET turns off and the converter latches off. The converter remains in the off state until the device is reset by cycling 5 V until the 5-V POR is reached (2.3-V nominal) or when the EN pin is toggled off and on.

Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the Overcurrent Protection and Overcurrent Limit sections. If the output voltage drops below 68% of V_{REFIN}, after approximately a 250 µs delay, the device stops switching and enters hiccup mode. After a hiccup waiting time, a restart is attempted. If the fault condition is not cleared, hiccup mode operation may continue indefinitely.

Overcurrent Protection

Both positive and negative overcurrent protection are provided in the TPS53317.

- Overcurrent Limit (OCL)
- Negative OCL

Overcurrent Limit

If the sensed current value is above the OCL setting, the converter delays the next ON pulse until the current drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. The TPS53317 uses a valley current limiting scheme where the DC OCL trip point is the OCL limit plus half of the inductor ripple current. The typical valley OCL threshold is 7.6 A or 5.4 A (depending on mode selection). The average output current limit calculation is shown in Equation 6.

During the overcurrent protection event, the output voltage droops if the duty cycle cannot satisfy output voltage requirements and continues to droop until the UVP limit is reached. Then, the converter de-asserts the PGOOD pin, and then enters hiccup mode after a 250-µs delay. The converter remains in hiccup mode until the fault is cleared.

$$I_{OCL(dc)} = I_{OCL(valley)} + \frac{1}{2} \times I_{P-P} \quad (6)$$

Negative OCL

The negative OCL circuit acts when the converter is sinking current from the output capacitor(s). The converter continues to act in a *valley* mode, the typical value of the negative OCL set point is –9.3 A or –6.5 A (depending on mode selection) .

Thermal Protection

The TPS53317 has an internal temperature sensor. When the temperature reaches a nominal 145°C, the device shuts down until the temperature decreases by approximately 10°C, when the converter restarts.

TYPICAL CHARACTERISTICS

Characterization data tested using the TPS53317EVM-750 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUU642 for detailed configuration.

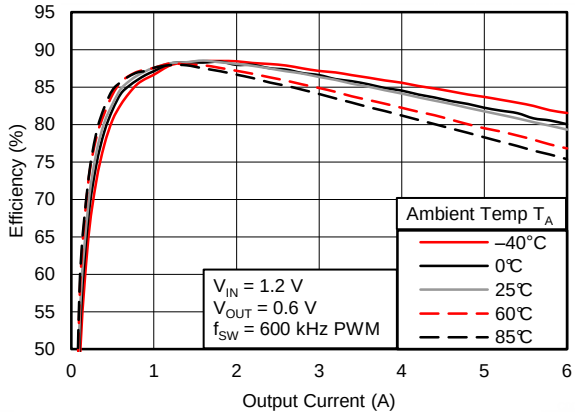


Figure 16. Efficiency vs. Output Current, V_{IN} = 1.2 V

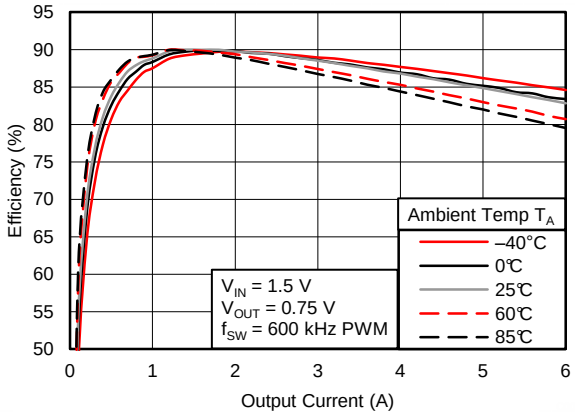


Figure 17. Efficiency vs. Output Current, V_{IN} = 1.5 V

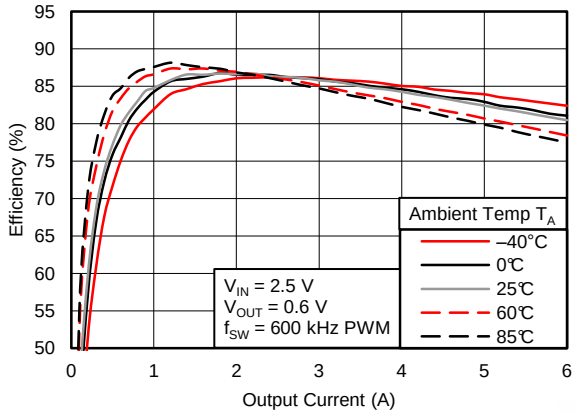


Figure 18. Efficiency vs. Output Current, V_{IN} = 2.5 V

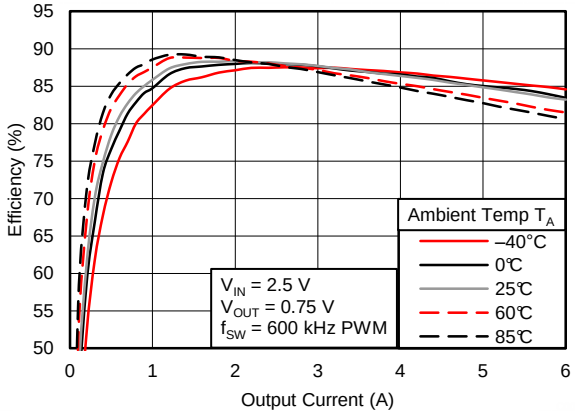


Figure 19. Efficiency vs. Output Current, V_{IN} = 2.5 V

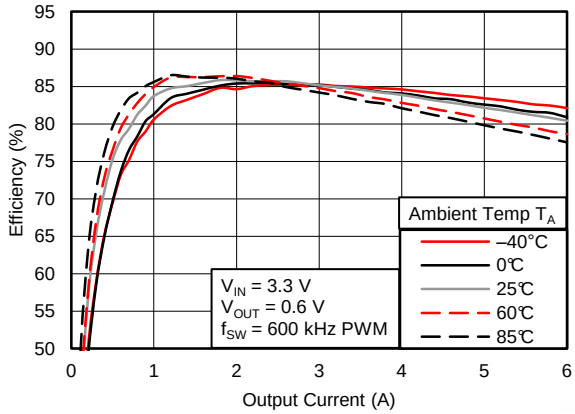


Figure 20. Efficiency vs. Output Current, V_{IN} = 3.3 V

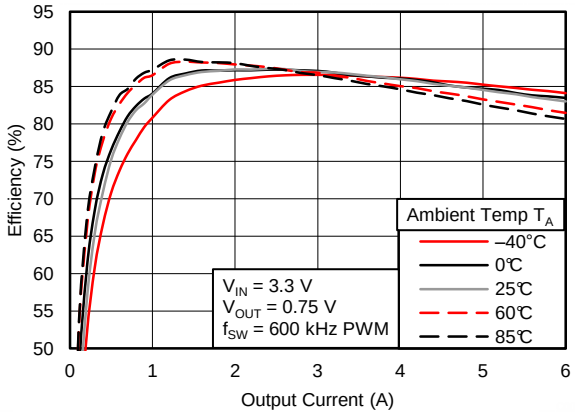


Figure 21. Efficiency vs. Output Current, V_{IN} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

Characterization data tested using the TPS53317EVM-750 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUU642 for detailed configuration.

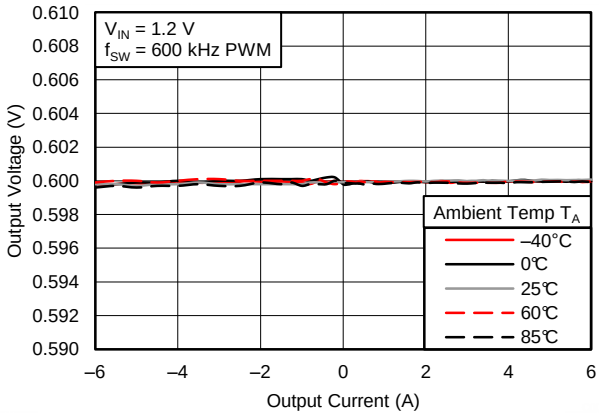


Figure 22. Load Regulation, V_{IN} = 1.2 V

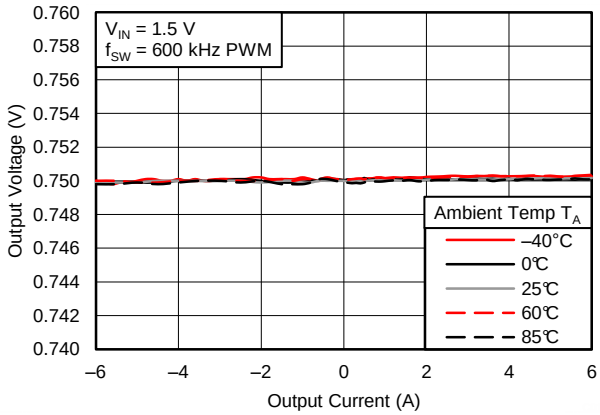


Figure 23. Load Regulation, V_{IN} = 1.5 V

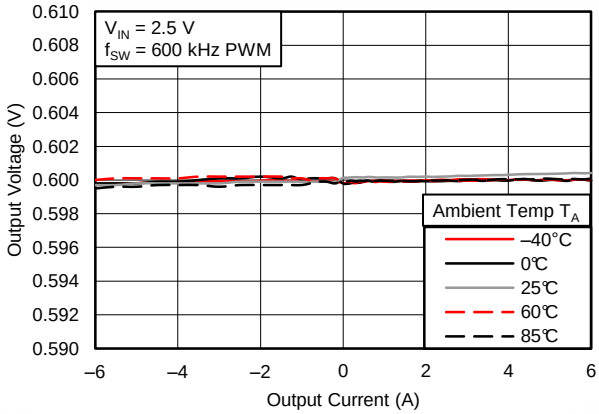


Figure 24. Load Regulation, V_{IN} = 2.5 V

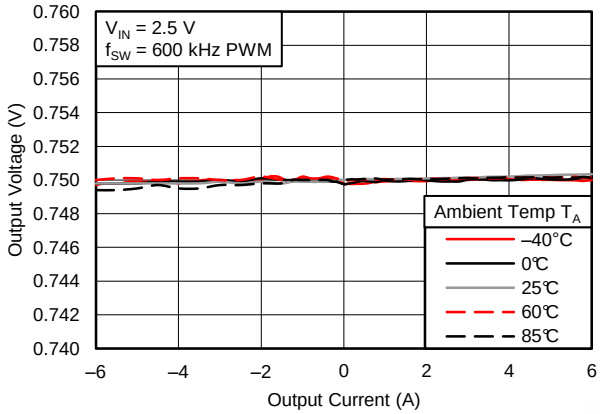


Figure 25. Load Regulation, V_{IN} = 2.5 V

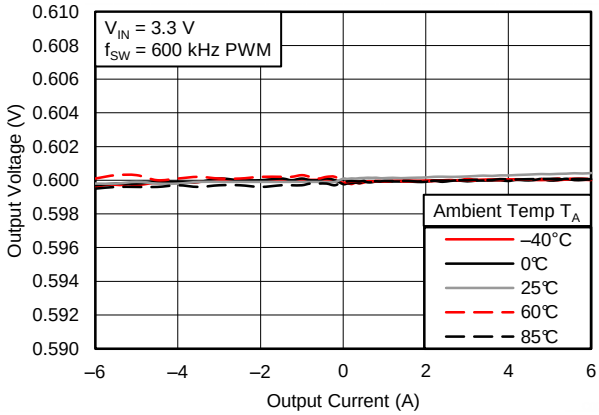


Figure 26. Load Regulation, V_{IN} = 3.3 V

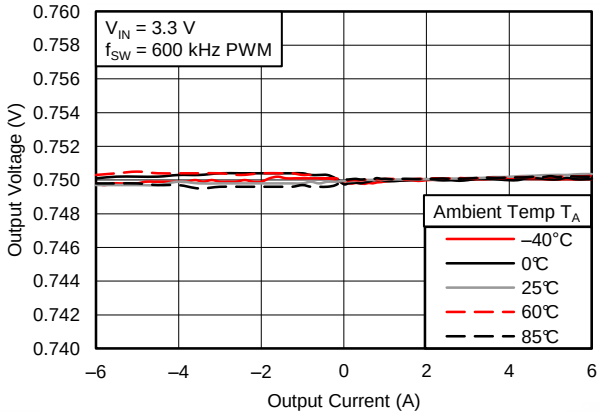


Figure 27. Load Regulation, V_{IN} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

Characterization data tested using the TPS53317EVM-750 where the external tracking input sets the output voltage and operates in non-droop mode. See SLUU642 for detailed configuration.

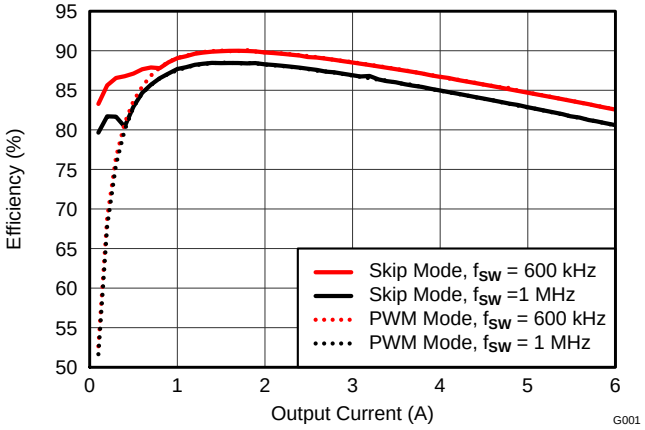


Figure 28. Efficiency vs Output Current
V_{IN} = 1.5 V, V_{OUT} = 0.75 V

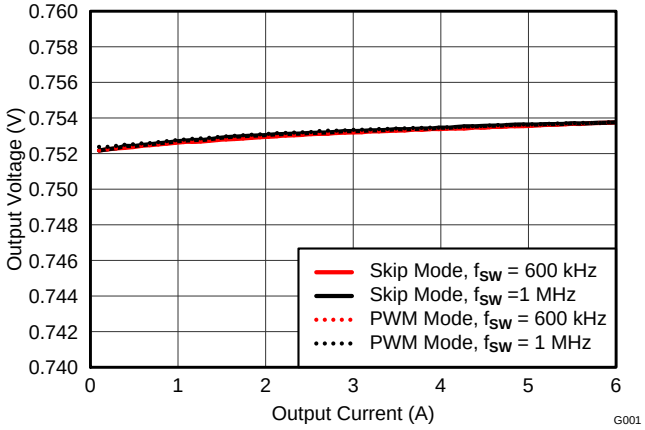


Figure 29. Load Regulation,
V_{IN} = 1.5 V, V_{OUT} = 0.75 V

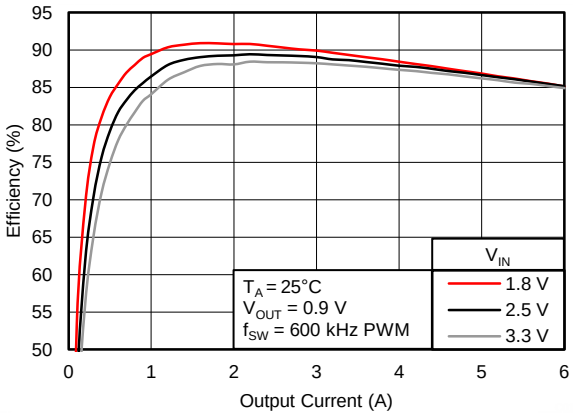


Figure 30. Efficiency vs. Output Current, V_{OUT} = 0.9 V

LAYOUT CONSIDERATIONS

Good layout is essential for stable power supply operation. Follow these guidelines for an optimized PCB layout.

- Connect PGND pins to the thermal pad underneath the device. Use four vias to connect the thermal pad to internal ground planes.
- Place VIN, V5IN and VREF decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, PGND and SW pins. These nodes carry high current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Place COMP and VOUT analog signal traces away from noisy signals (SW, BST).
- The GND pin should connect to the PGND in only one place, through a via or a 0-Ω resistor.

DESIGN EXAMPLES

Design Example 1, DDR4 Application

Step 1. Determine Requirements

- V_{IN} = 1.2 V
- V_{OUT} = 0.6 V
- Maximum load step size of 3 A @ slew rate 7 A/µs (–1.5 A to 1.5 A)
- DC +AC + Ripple voltage regulation limit at sense point: ±42 mV (0.642 V overshoot/ 0.558 V undershoot)
- Maximum Load: I_{MAX} = 2.5 A

Step 2. Determine Configuration

Because this DDR4 application requires a tight load tolerance, fast transient response, and sinking current capability, the design uses a non-droop PWM configuration. Choose 600-kHz switching frequency due to the duty cycle and minimim off-time of the device, and set an overcurrent (OC) valley limit of 5.4 A due to the maximum load requirement of 2.5 A. Referring to Table 1 select an R_{MODE} value of 68 kΩ.

Step 3. Select Inductor

Smaller inductor values have better transient performance but higher ripple and lower efficiency. High values have the opposite characteristics. It is common practice to limit the ripple current to 30% to 50% of the maximum current. Choose 50% to allow use of a smaller inductor for faster transient performance.

$$\Delta I_{P-P} = 2.5\ A \times 0.5 = 1.25\ A \tag{7}$$

$$L = \frac{1}{f_{SW} \times \Delta I_{P-P}} \times V_{OUT} \times (1 - D)$$

where

- D = duty cycle (8)

Because this device operates in DCAP+ mode, the frequency and duty cycle vary based on the input voltage, the output voltage and load. With a 2.5-A load, a 1.2-V input voltage and 0.60 V output voltage, f_{SW} is experimentally measured at approximately 800 kHz and duty cycle of 0.55. Therefore L is calculated as shown in Equation 10.

$$L = \frac{1}{(800\ kHz \times 1.25\ A)} \times 0.6V \times 0.45 = 0.270\ \mu H \tag{9}$$

Choose the closest standard value, 0.25 µH.

Step 4. Determine Output Capacitance

Use Equation 10 to calculate the output capacitance for a desired maximum overshoot.

$$C_{OUT(min),OS} = \frac{\Delta I_{OUT}^2 \times L}{2 \times V_{OUT} \times V_{OS}}$$

where

- $C_{OUT(min),OS}$ is the minimum output capacitance for a desired overshoot
- ΔI_{OUT} is the maximum output current change in the application
- V_{OUT} = desired output voltage
- V_{OS} is the desired output voltage change due to overshoot (10)

Choose a value of 30 mV to account for normal output voltage ripple.

$$C_{OUT(min),OS} = \frac{(3\ \text{A})^2 \times 0.25\ \mu H}{2 \times 0.6\ V \times 0.03\ V} = 62.5\ \mu F \tag{11}$$

Use Equation 12 to calculate the necessary output capacitance for a desired maximum undershoot.

$$C_{OUT(min),US} = \frac{\Delta I_{OUT}^2 \times L \times \left(\frac{V_{OUT}}{V_{IN}} \times t_{SW} + t_{MIN(off)}\right)}{2 \times V_{OUT} \times V_{US} \times \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \times t_{SW} - t_{MIN(off)}\right)}$$

where

- $C_{OUT(min),US}$ is the minimum output capacitance for a desired undershoot
- V_{US} is the desired output voltage change due to overshoot
- t_{SW} is the period of switch node
- $t_{MIN(off)}$ is the minimum off-time (270 ns) (12)

Again, choose 30 mV to account for normal output voltage ripple.

$$C_{OUT(min),US} = \frac{(3\ \text{A})^2 \times 0.25\ \mu H \times \left(\frac{0.6\ V}{1.2\ V} \times \frac{1}{800\ kHz} + 270\ ns\right)}{2 \times 0.6\ V \times 0.03\ V \times \left(\frac{1.2\ V - 0.6\ V}{1.2\ V} \times \frac{1}{800\ kHz} - 270\ ns\right)} = 157.6\ \mu F \quad (13)$$

The undershoot requirements determine, so there must be a minimum of 157.6 µF. Because this is a DDR application where size is also a consideration, this design uses only ceramic capacitors. To account for voltage de-rating of capacitors and provide additional margin, this design includes eleven 22-µF output capacitors.

Step 5. Input Capacitance

This design requires sufficient input capacitance to filter the input current from the host source. Use Equation 14 to calculate the necessary input capacitance.

$$C_{IN(min)} = I_{out} \times \frac{D \times (1 - D)}{\Delta V_{IN(P-P)} \times f_{SW}}$$

where

- $\Delta V_{IN(P-P)}$ is the desired input voltage ripple (typically 1% of the input voltage) (14)

$$C_{IN(min)} = 2.5\ A \times \frac{0.55 \times (1 - 0.55)}{12\ \text{mV} \times 800\ kHz} = 64.45\ \mu F \quad (15)$$

As with the output capacitance selection, this design accounts for voltage de-rating of capacitors and provides additional margin, using four 22 µF input capacitors.

Step 6. Compensation Network

In order to achieve stable operation, the crossover frequency should be less than 1/5 of the switching frequency.

$$f_{CO} = \frac{1}{2\pi} \times \frac{g_M}{C_{OUT}} \times \frac{R_C}{R_S} = 80\ kHz$$

where

- R_S = 53 mΩ (16)

Account for capacitor de-rating here and set the value of C_{OUT} to 160 µF, so that Equation 17 is true.

$$R_C = \frac{f_{CO} \times R_S \times 2\pi \times C_{OUT}}{g_M} = \frac{80\ kHz \times 53\ m\Omega \times 2\pi \times 160\ \mu F}{1\ mS} = 4.26\ k\Omega \quad (17)$$

Choose an R_C value of 3.9 kΩ. Determine C_C by choosing the value of the zero created by R_C and C_C. Using the relationship described in Equation 18.

$$f_z = \frac{f_{CO}}{5} = \frac{1}{2\pi \times R_C \times C_C} \quad (18)$$

Equation 18 yields a C_C value of 2.55 nF. Choose the closest common capacitor value of 2.2 nF. To determine a value for C_P, first consider the relationship described in Equation 19.

$$f_p = \frac{1}{2\pi \times R_C \times \frac{C_C \times C_P}{C_C + C_P}} \approx \frac{1}{2\pi \times R_C \times C_P} \quad (19)$$

- $C_C >> C_P$

Because $C_C >> C_P$, set the pole to be two times the switching frequency as described in Equation 20.

$$C_P \cong \frac{1}{2\pi \times R_C \times 2f_{SW}} = \frac{1}{2\pi \times 3.9\ k\Omega \times 2 \times 800\ kHz} = 25.5\ pF \quad (20)$$

To boost the gain margin, set C_P to 33 pF.

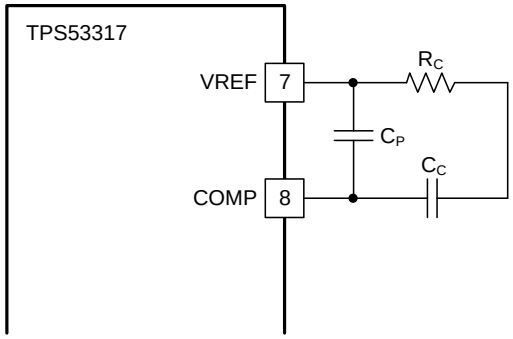


Figure 31. Compensation Network Circuit

Peripheral Component Selection

As described in the table , connect a 0.22-µF capacitor from the VREF pin to GND and connect a 0.1-µF bootstrap capacitor from the SW pin to the BST pin. Because the PGOOD pin is open drain, connect a pull-up resistor between it and the 5-V rail.

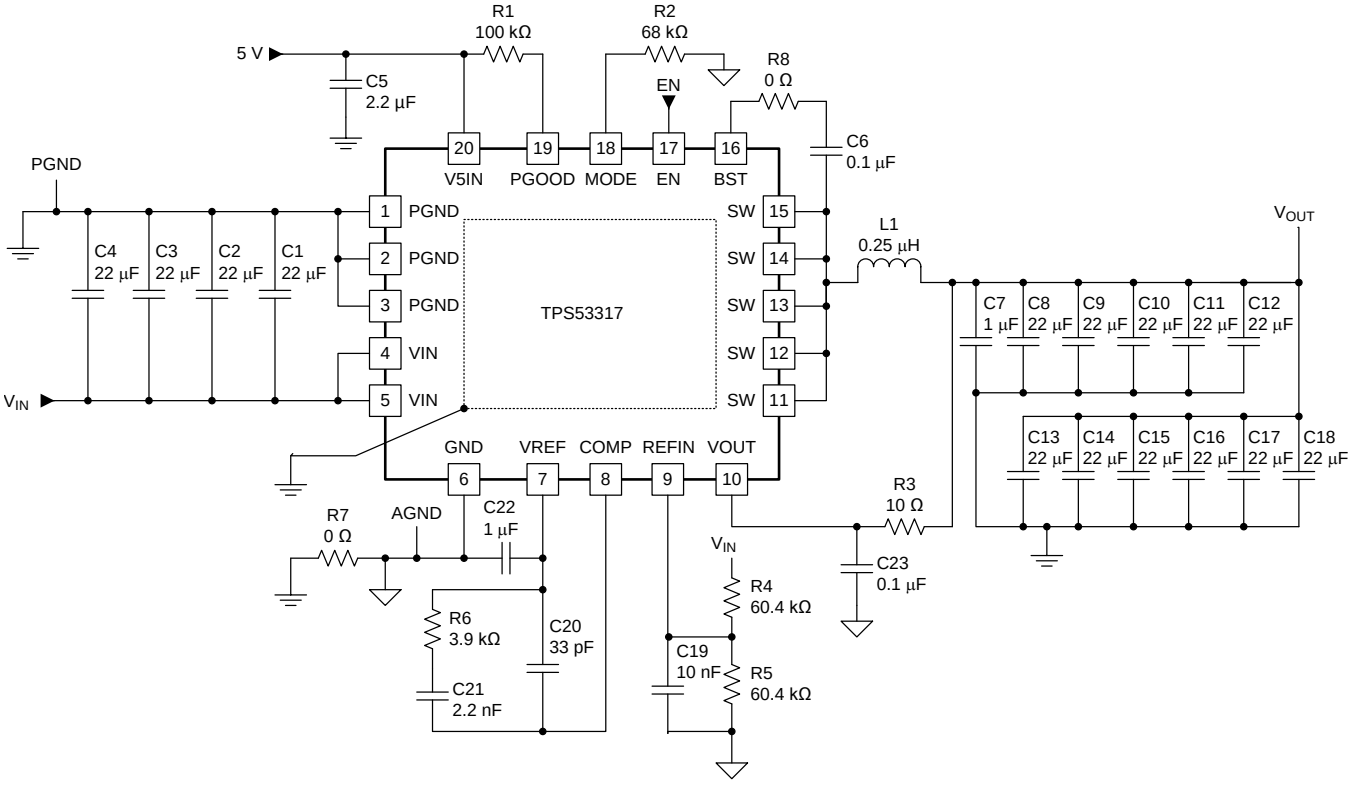


Figure 32. Design Example 1: DDR4 Application Schematic

Test Results

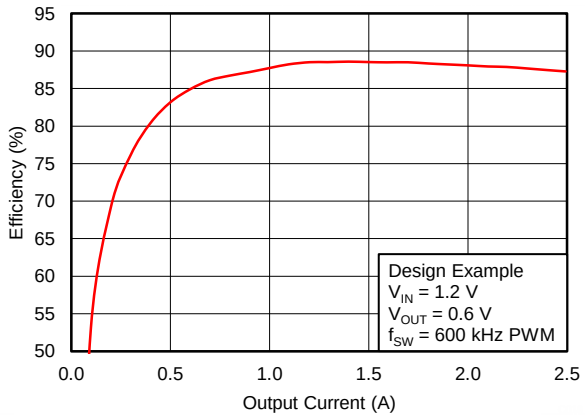


Figure 33. Efficiency

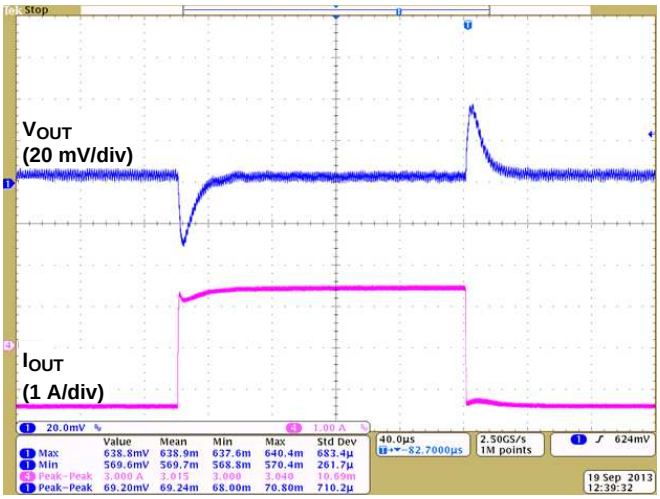


Figure 34. Load Transient

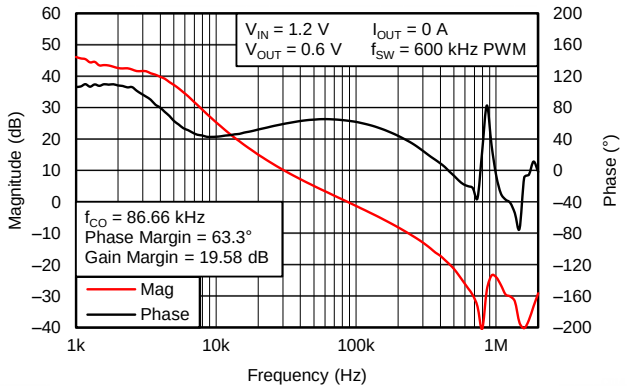


Figure 35. Bode Plot, No Load

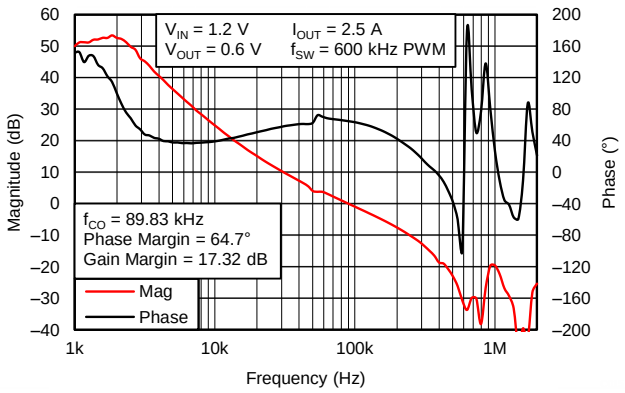


Figure 36. Bode Plot, Full Load

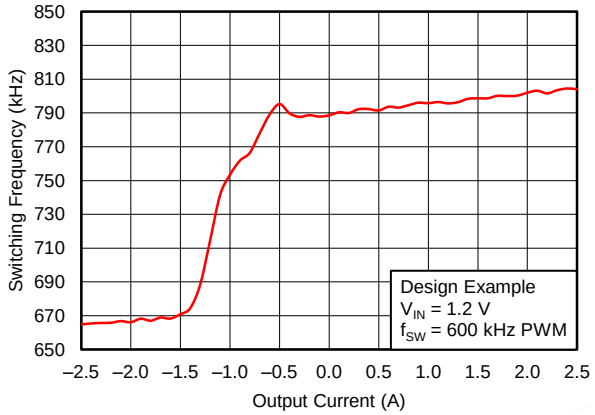


Figure 37. Switching Frequency vs. Load

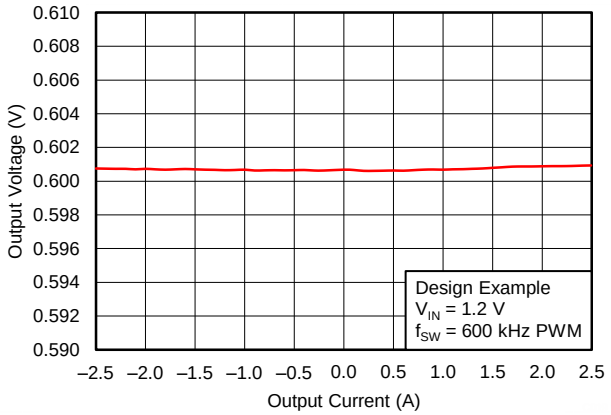


Figure 38. Load Regulation

Design Example 2 Summary: DDR3 Application

Requirements

- V_{IN} = 1.5 V
- V_{OUT} = 0.75 V

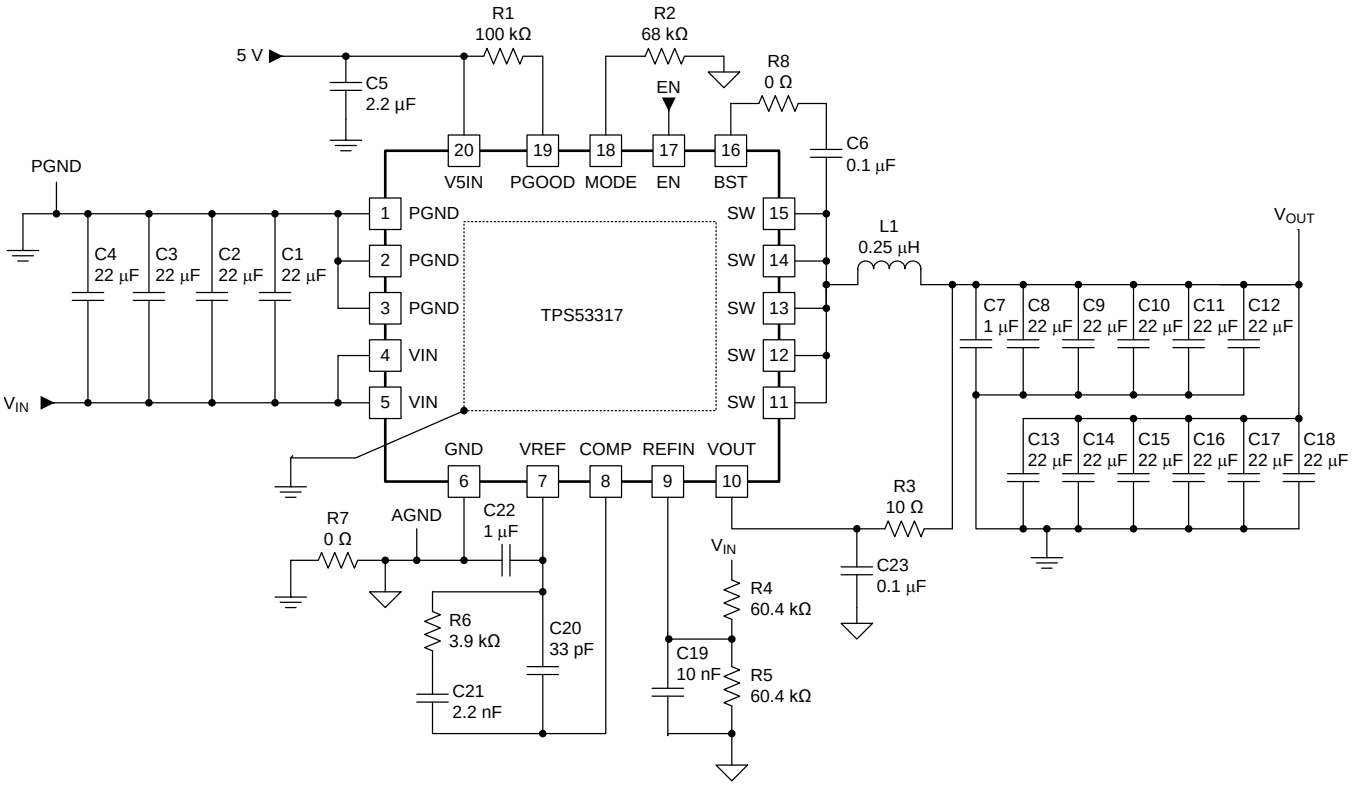


Figure 39. Design Example 2 Schematic: DDR3 Application

Design Example 3 Summary: Non-Tracking Point-of-Load (POL)Application

Requirements

- V_{IN} = 3.3 V
- V_{OUT} = 1.2 V

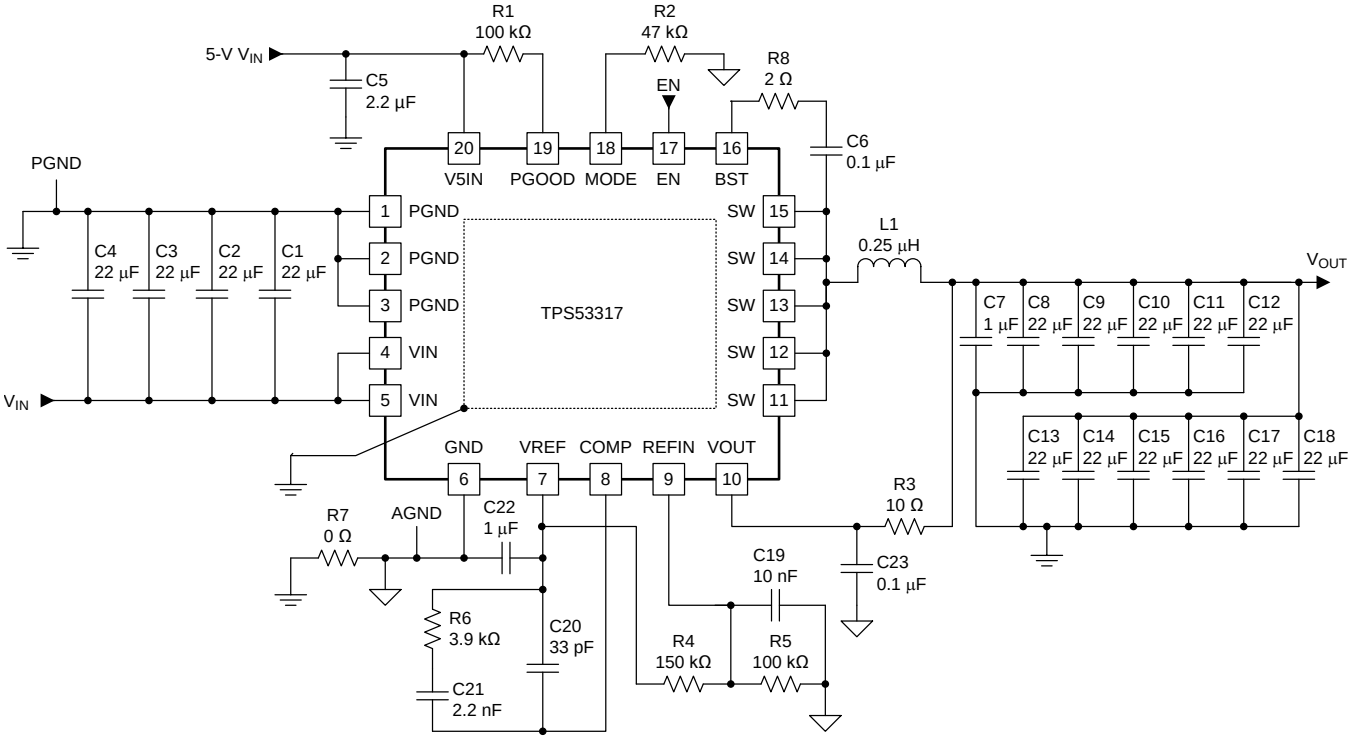


Figure 40. Design Example 3 Schematic: Non-Tracking POL Application

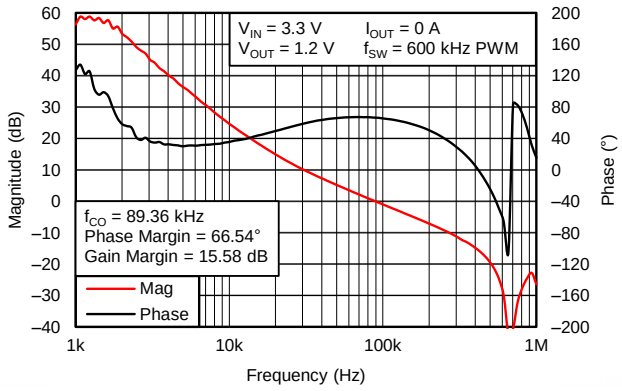


Figure 41. Bode Plot No Load

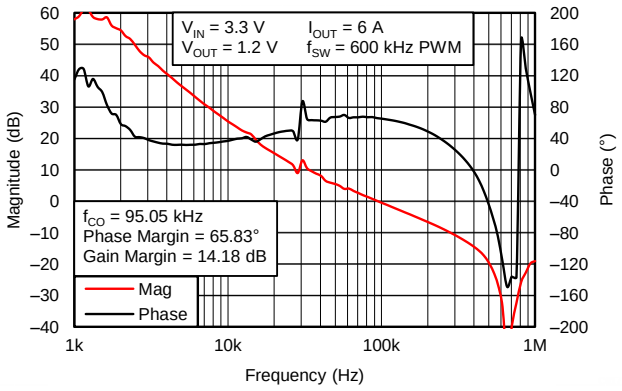


Figure 42. Bode Plot Full Load

REVISION HISTORY

Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (MAY 2012) to Revision C — **Page**

- Added clarity to Internal soft-start delay time and soft-start time test conditions in Electrical Characteristics table 5
- Added clarity to PIN FUNCTIONS table 6
- Deleted typographical errors in FUNCTIONAL BLOCK DIAGRAM 7
- Added Figure 11, Figure 13 and Figure 14 in Power Sequences section. 14
- Added clarity to Output Overvoltage Protection (OVP) section. 16
- Changed minimum valley OCL from "is 6 A or 4 A" to "is 7.6 A or 5.4 A" in Overcurrent Limit section. 16
- Changed "the absolute value of the negative OCL set point is typically -6.5 A or -4.5 A" to "the typical value of the negative OCL set point is –9.3 A or –6.5 A" in Negative OCL section. 17
- Added clarity to LAYOUT CONSIDERATIONS section. 20
- Added DESIGN EXAMPLES 21

Changes from Revision A (JULY 2011) to Revision B — **Page**

- Added Memory Termination bullet in APPLICATIONS 1
- Added clarity to DESCRIPTION 1
- Changed title of Figure 1 8
- Added updates to Table 1 13

Changes from Original (JUNE 2011) to Revision A — **Page**

- Changed from "SKIP and Forced CCM" to "SKIP or Forced CCM" in FEATURES 1
- Changed from "600-kHz and 1-MHz Switching" to "600-kHz or 1-MHz Switching" in FEATURES 1
- Added clarity to Simplified Application drawing 1
- Changed from "f_{SW} = 600 kHz" to " f_{SW} = 1 MHz" for $t_{ON(min)}$ in EC table 5
- Added clarity to FUNCTIONAL BLOCK DIAGRAM 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DPA02257RGBR	ACTIVE	VQFN	RGB	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53317	Samples
TPS53317RGBR	ACTIVE	VQFN	RGB	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53317	Samples
TPS53317RGBT	ACTIVE	VQFN	RGB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	53317	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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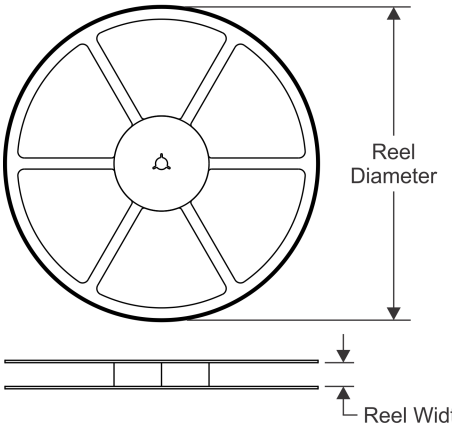
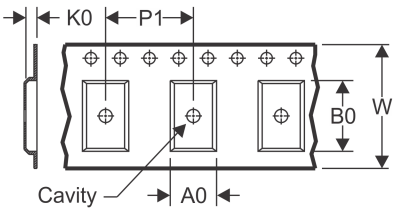
TAPE AND REEL INFORMATION

REEL DIMENSIONS

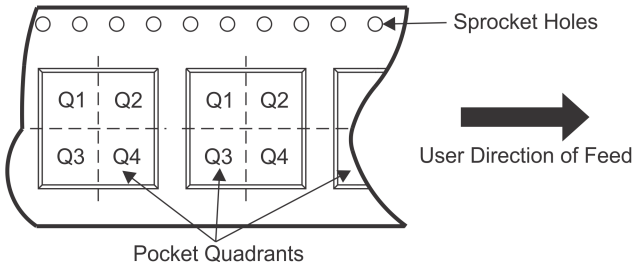


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

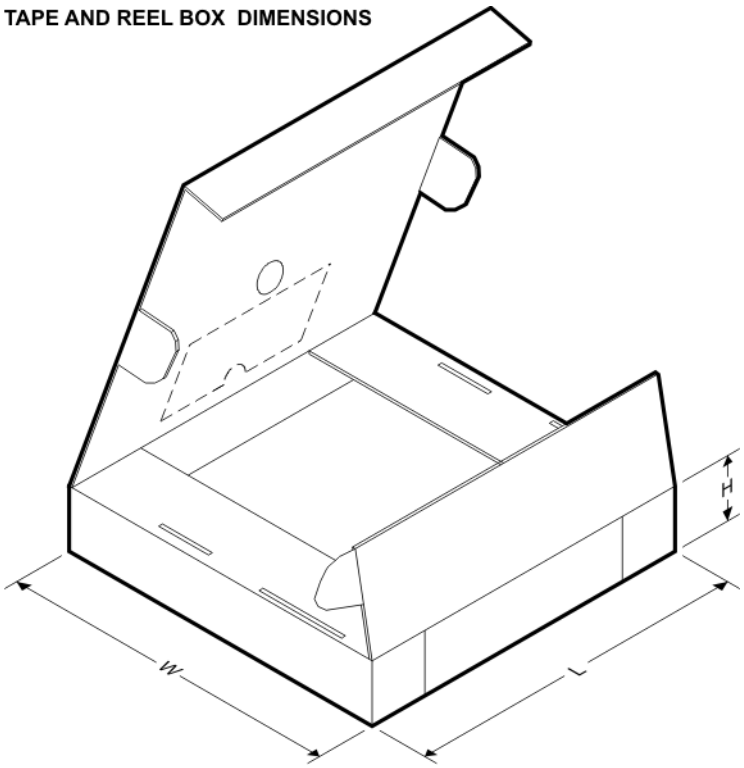
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53317RGBR	VQFN	RGB	20	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS53317RGBR	VQFN	RGB	20	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS53317RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TPS53317RGBT	VQFN	RGB	20	250	180.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

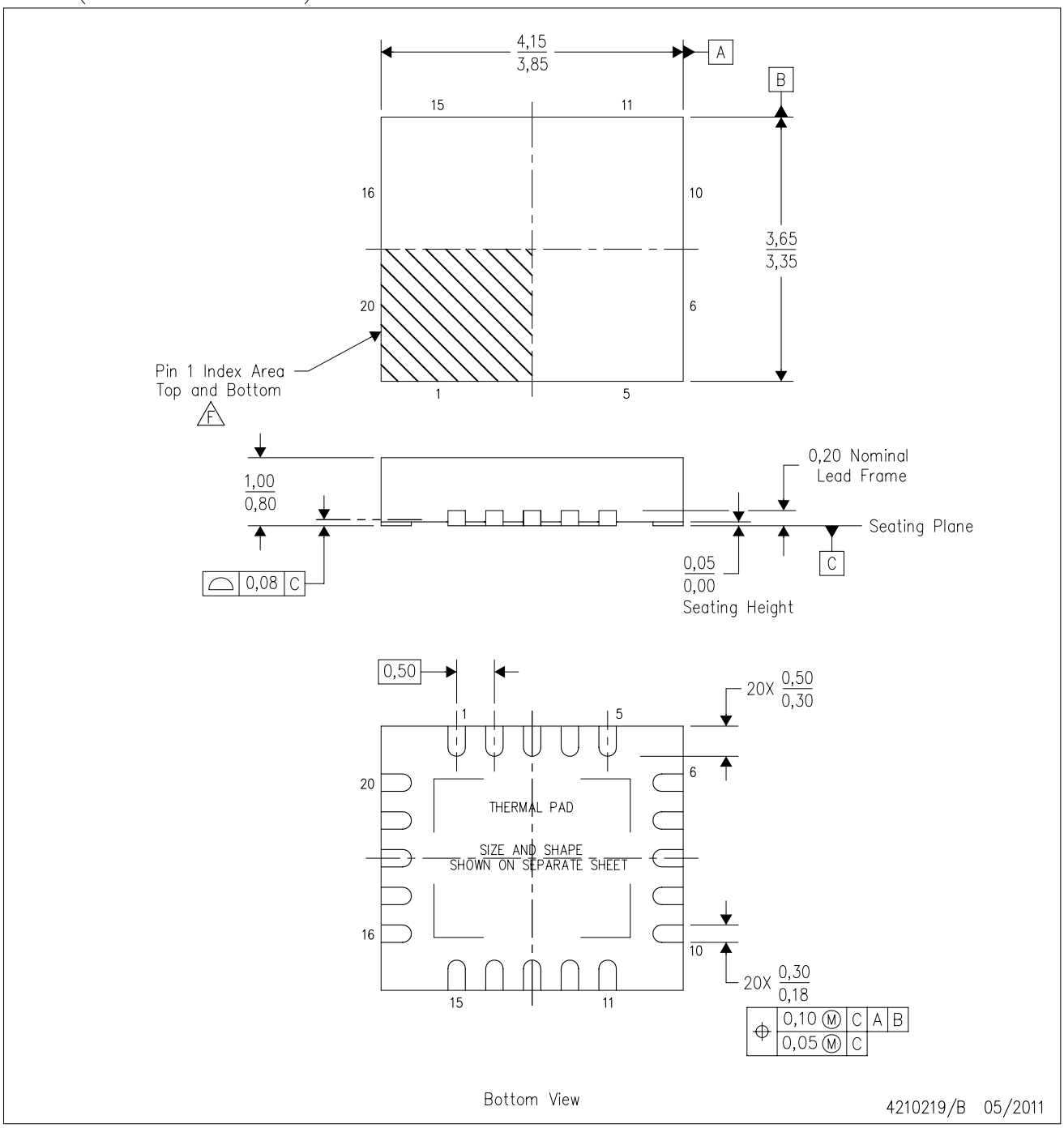
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53317RGBR	VQFN	RGB	20	3000	367.0	367.0	35.0
TPS53317RGBR	VQFN	RGB	20	3000	367.0	367.0	35.0
TPS53317RGBT	VQFN	RGB	20	250	210.0	185.0	35.0
TPS53317RGBT	VQFN	RGB	20	250	210.0	185.0	35.0

RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

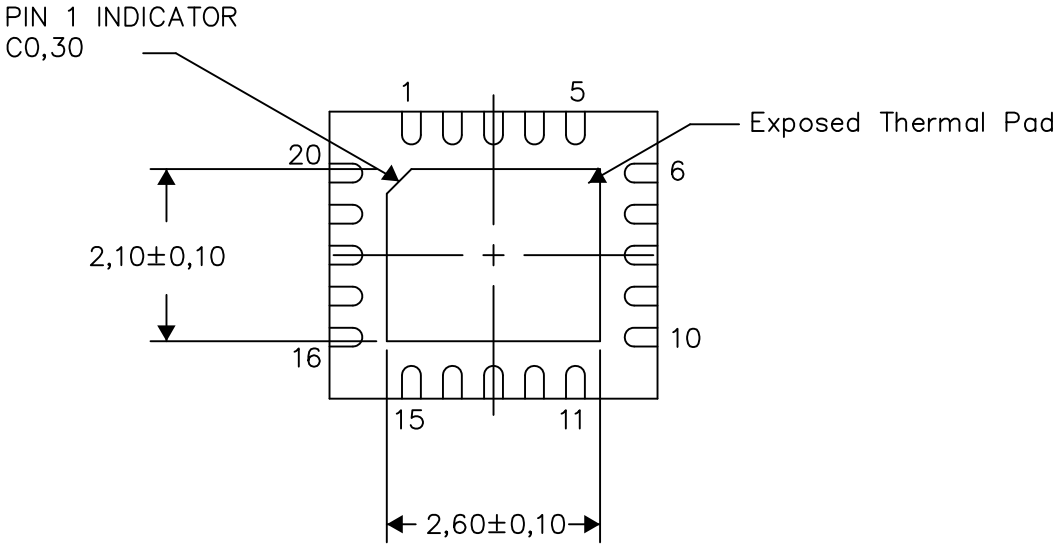
RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



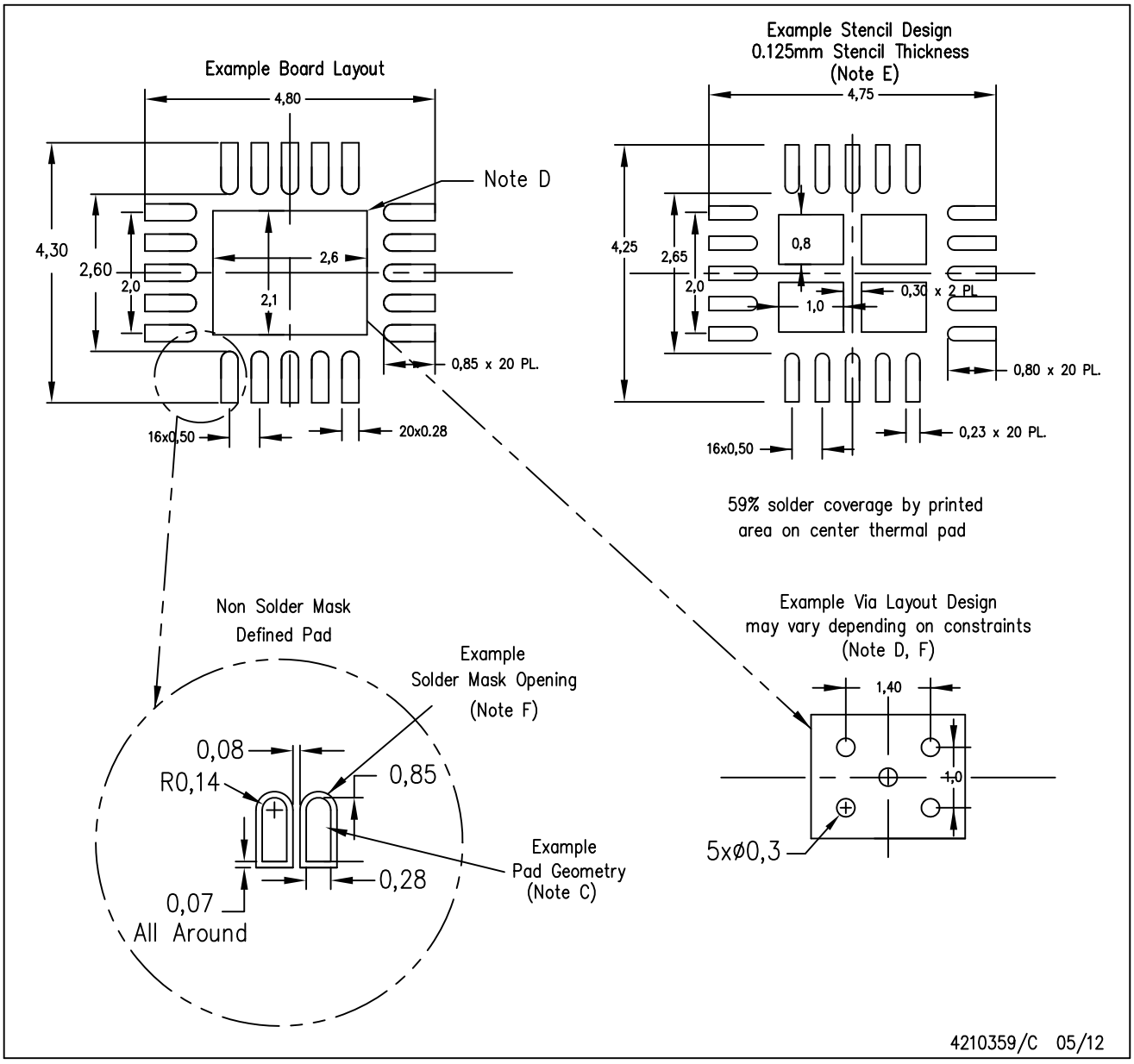
Bottom View

Exposed Thermal Pad Dimensions

4210242/C 05/12

NOTE: All linear dimensions are in millimeters

RGB (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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