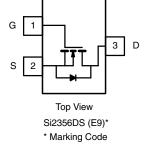


**Vishay Siliconix** 

## N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) Max.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
	0.051 at V <sub>GS</sub> = 10 V	4.3				
40	0.054 at V <sub>GS</sub> = 4.5 V	4.1	3.8 nC			
	0.070 at $V_{GS}$ = 2.5 V	3.6				





#### FEATURES

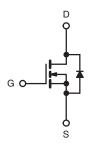
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>q</sub> Tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>



ROHS COMPLIANT HALOGEN FREE

#### APPLICATIONS

- DC/DC Converter
- Load Switch
- LED Backlighting
- Power Management



N-Channel MOSFET

Ordering Information:

Si2356DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	40	V
Gate-Source Voltage		V <sub>GS</sub>	± 12	v
	T <sub>C</sub> = 25 °C		4.3	
Continuous Drain Current (T 150 °C)	T <sub>C</sub> = 70 °C		3.4	
Continuous Drain Current ( $T_J = 150 \ ^{\circ}C$ )	T <sub>A</sub> = 25 °C	I <sub>D</sub>	3.2 <sup>a,b</sup>	
	T <sub>A</sub> = 70 °C		2.6 <sup>a,b</sup>	А
Pulsed Drain Current (t = 100 μs)		I <sub>DM</sub>	20	
	T <sub>C</sub> = 25 °C		1.4	
Continuous Source-Drain Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	0.8 <sup>a,b</sup>	
	T <sub>C</sub> = 25 °C		1.7	
Maximum Power Dissipation	T <sub>C</sub> = 70 °C		1.1	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	0.96 <sup>a,b</sup>	W
	T <sub>A</sub> = 70 °C		0.62 <sup>a,b</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient a,c	t ≤ 5 s	R <sub>thJA</sub>	100	130	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	60	75	0/11		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

c. Maximum under steady state conditions is 175  $^\circ\text{C/W}.$ 

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b. t = 5 s.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static					•	•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_{D} = 250 \mu A$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			43			
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 3.8		mV/°C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	0.6		1.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 12 V$			± 100	nA	
	I <sub>DSS</sub>	$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current		$V_{DS}$ = 40 V, $V_{GS}$ = 0 V, $T_{J}$ = 55 °C			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5$ V, $V_{GS} = 10$ V	10			Α	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 3.2 \text{ A}$		0.042	0.051		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_{D} = 3.1 \text{ A}$		0.045	0.054	Ω	
		$V_{GS} = 2.5 \text{ V}, I_D = 2 \text{ A}$		0.056	0.070		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.2 A		13		S	
Dynamic <sup>b</sup>				1	1		
Input Capacitance	C <sub>iss</sub>			370		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		50			
Reverse Transfer Capacitance	C <sub>rss</sub>			17			
	Qg	$V_{DS} = 20$ V, $V_{GS} = 10$ V, $I_{D} = 3.2$ A		8.1	13	nC	
Total Gate Charge				3.8	5.7		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 20 V, $V_{GS}$ = 4.5 V, $I_D$ = 3.2 A		0.72			
Gate-Drain Charge	Q <sub>gd</sub>			0.81			
Gate Resistance	Rg	f = 1 MHz	0.2	0.7	1.4	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			6	12		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 7.7 $\Omega$		12	20	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 2.6 A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 1 $\Omega$		13	20		
Fall Time	t <sub>f</sub>			6	12		
Turn-On Delay Time	t <sub>d(on)</sub>			10	20	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 7.7 $\Omega$		52	78	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong$ 2.6 A, $\text{V}_\text{GEN}$ = 4.5 V, $\text{R}_\text{g}$ = 1 $\Omega$		18	27		
Fall Time	t <sub>f</sub>			53	80		
Drain-Source Body Diode Characteristic	s					<b>I</b>	
Continuous Source-Drain Diode Current	ا <sub>S</sub>	$T_{C} = 25 \ ^{\circ}C$			1.4	۸	
Pulse Diode Forward Current (t = 100 $\mu$ s)	I <sub>SM</sub>				20	A	
Body Diode Voltage	V <sub>SD</sub>	$I_{S} = 2.6 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			12	20	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			5	10	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 2.6 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^\circ\text{C}$		8.5			
Reverse Recovery Rise Time	t <sub>b</sub>			3.5		ns	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

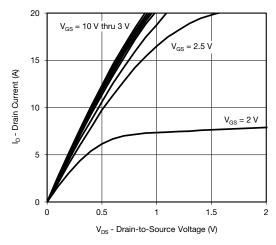
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

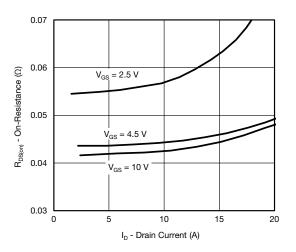


## Si2356DS Vishay Siliconix

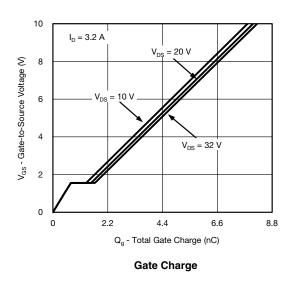
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

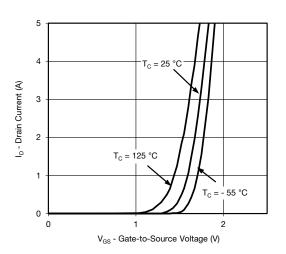




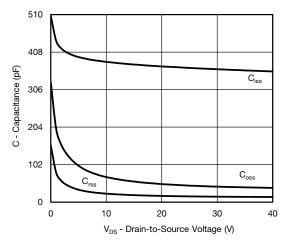


**On-Resistance vs. Drain Current and Gate Voltage** 

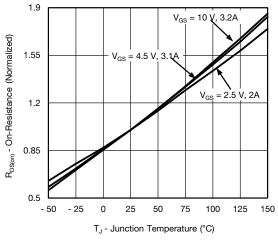




**Transfer Characteristics** 



Capacitance



**On-Resistance vs. Junction Temperature** 

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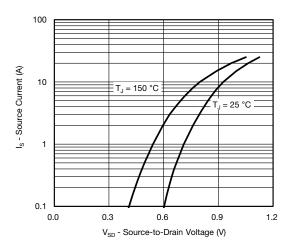
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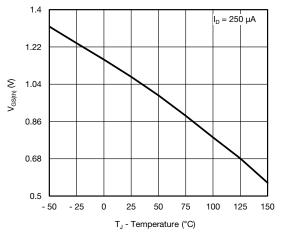




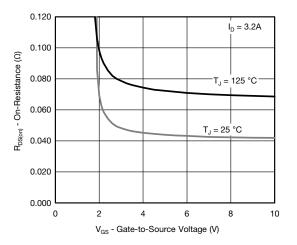
#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



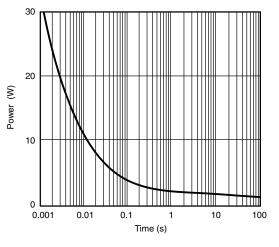
Source-Drain Diode Forward Voltage



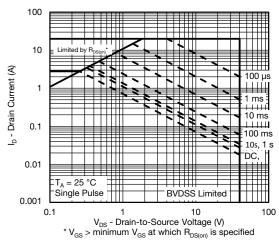
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



Safe Operating Area, Junction-to-Ambient

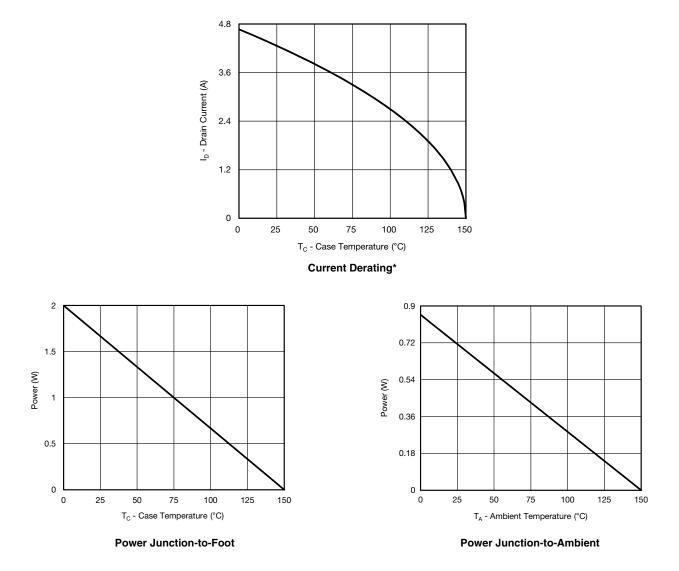
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#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

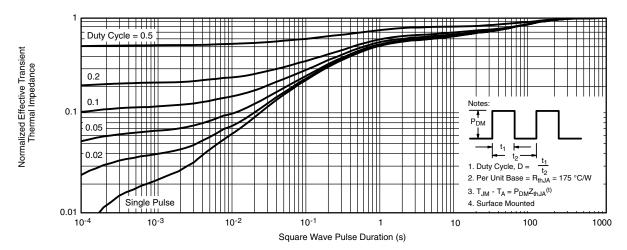


\* The power dissipation  $P_D$  is based on  $T_{J(max,)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

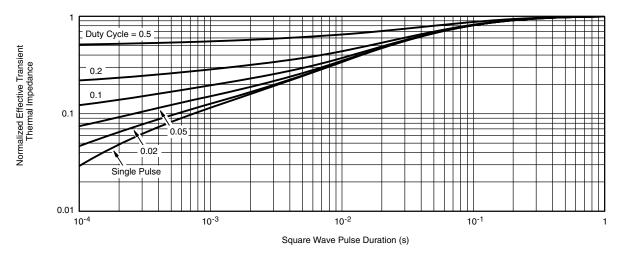


**Vishay Siliconix** 

#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?62893">www.vishay.com/ppg?62893</a>.

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## Package Information

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#### SOT-23 (TO-236): 3-LEAD







Dim	MILLIN	METERS	INCHES		
	Min	Max	Min	Мах	
Α	0.89	1.12	0.035	0.044	
A <sub>1</sub>	0.01	0.10	0.0004	0.004	
A <sub>2</sub>	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E <sub>1</sub>	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e <sub>1</sub>	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L <sub>1</sub>	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	



# Application Note 826

Vishay Siliconix

#### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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