New Industry Features

- Programmable time sequencing
- Integrated oscillator and dividers
- No crystal required
- Dual voltage monitors
- Remote delay selection
- Remote monitor/switch diagnostics
- Cascade delays of multiple devices

X80120/X80121

Voltage Supervisor/Sequencer Dual Programmable Time Delay with Local/ Remote Voltage Monitors

FEATURES

- **Dual voltage Monitor and Sequencing**
  - — Two independent voltage monitors
  - — Two time delay circuits (in circuit programmable)
  - — Remote delay via SMBus
  - — Programmable voltage thresholds and delay times
  - — Sequence up to 3 power supplies.
- **Fault detection register**
  - — Remote diagnostics of voltage fail event.
- **Debounced manual reset input**
- **Manufacturing/Configuration Memory**
  - — 2Kbits of EEPROM
  - — 400kHz SMBus interface
- **Available packages**
  - — 20-lead Quad No-Lead Frame (QFN — 5 x 5 mm)

APPLICATIONS

- **General Purpose Timers**
- **Long Time Delay Generation**
- **Cycle Timers / Waveform Generation**
- **ON/OFF Delay Timers**
- **Supply Sequencing for Distributed Power**
- **Programmable Delay Event Sequencing**
- **Multiple DC-DC ON/OFF Sequencing**
- **Voltage Window Monitoring with Reset**
- **ON/OFF switches with Programmable Delay**
- **Voltage Supervisor with Programmable Output Delays**
- **Databus Power Sequencing**
- **100 ms to 5 secs Selectable Delay Switches**
- **ATE or Data Acquisition Timing Applications**
- **Datapath/Memory Timing Applications**
- **Data Pipeline Timing Applications**
- **Batch Timer/Sequencers**
- **Adjustable Duty Cycle Applications**

DESCRIPTION

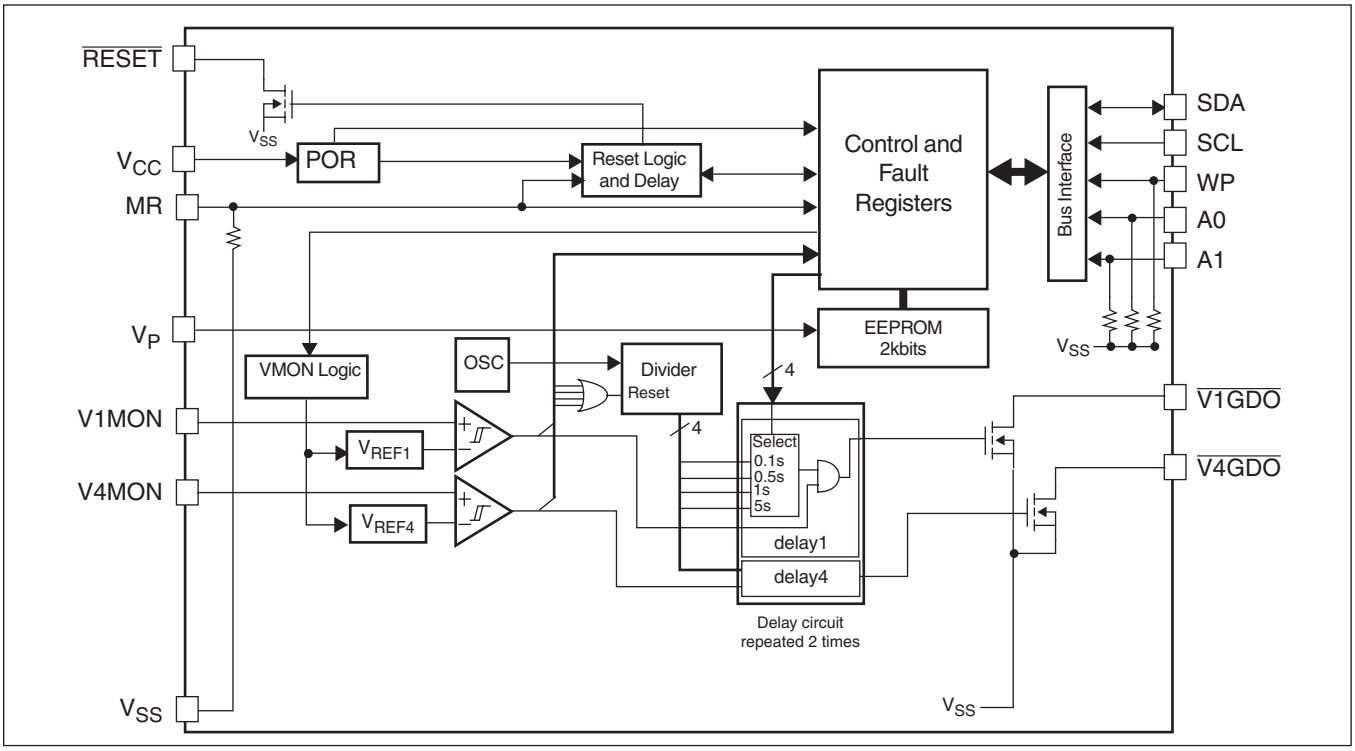
The X80120 is a voltage supervisor/sequencer with two built in voltage monitors. This allows the designer to monitor up to two voltages and sequence up to three events.

Low voltage detection circuitry protects the system from power supply failure or “brown out” conditions, resetting the system and resequencing the voltages when any of the monitored inputs fall below the minimum threshold level. The $\overline{\text{RESET}}$ pin is active until all monitored voltages reach proper operating levels and stabilize for a selectable period of time. Five common low voltage combinations are available, however, Xicor’s unique circuits allow the any voltage monitor threshold to be reprogrammed for special needs or for applications requiring higher precision.

A manual reset input provides debounce circuitry for minimum reset component count. Activating the manual reset both controls the $\overline{\text{RESET}}$ output and resequences the supplies through control of the ViFAIL pins.

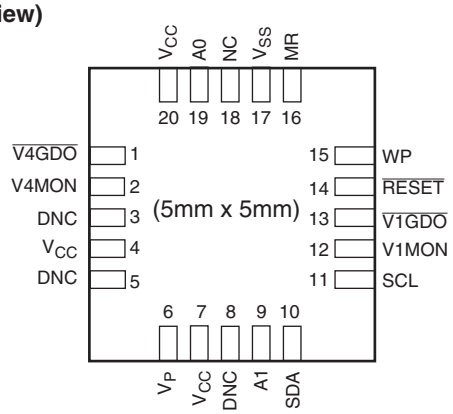
The X80120 has 2kb of EEPROM for system configuration, manufacturing or maintenance information. This memory is protected to prevent inadvertent changes to the contents.

BLOCK DIAGRAM



PIN OUTS

QFN package
(Top view)



ORDERING INFORMATION

ORDER NUMBER	V_{TRIP1}	V_{TRIP4}	Package
X80120Q20I	4.5	0.9	QFN
X80121Q20I	3.0	0.9	QFN

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... –65°C to +135°C
Storage temperature ..... –65°C to +150°C
V1MON, V4MON pins 5.5V
$\overline{V1GDO}$, $\overline{V4GDO}$ pins 5.5V
$\overline{RESET}$ pin 5.5V
SDA, SCL, WP, A0, A1 pins 5.5V
MR pin 5.5V
V_P pin 14V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Industrial (I)	–40°C	+85°C

Supply Voltage
V_{CC} = 4.5 to 5.5V

ELECTRICAL CHARACTERISTICS (Standard Settings)

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics						
V_{CC}	Supply Operating Range	4.5		5.5	V	
I_{CC}	Supply Current		1.0	2.5	mA	f_{SCL} = 0 kHz
V_P	EEPROM programming voltage	9		12	V	
I_P(3)	Programming Current			10	mA	
I_{LI}	Input Leakage Current (MR)			10	µA	V_{IL} = GND to V_{CC}
I_{LO}	Output Leakage Current ($\overline{V1GDO}$, $\overline{V4GDO}$, $\overline{RESET}$)			15	µA	
V_{IL}	Input LOW Voltage (MR)	-0.5		5 x 0.3	V	
V_{IH}	Input HIGH Voltage (MR)	5 x 0.7		5.5	V	
V_{OL}	Output LOW Voltage ($\overline{RESET}$, $\overline{V1GDO}$, $\overline{V4GDO}$)			0.4	V	I_{OL} = 4.0 mA

ELECTRICAL CHARACTERISTICS (Continued)(Standard Settings)

(Over the recommended operating conditions unless otherwise specified).

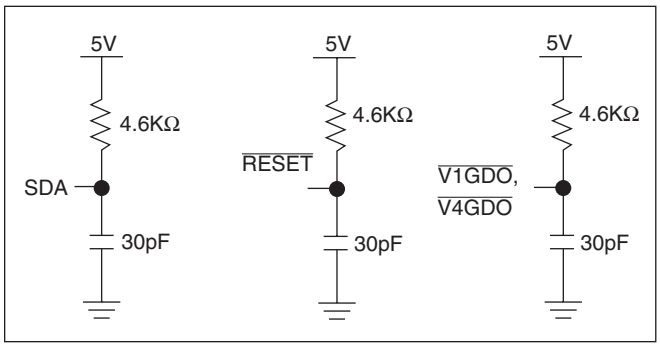
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{OUT}(1)	Output Capacitance ($\overline{RESET}$, $\overline{V1GDO}$, $\overline{V4GDO}$)			8	pF	V_{OUT} = 0V
V_{TRIP1}	V1MON Trip Point Voltage (Range) X80120 X80121	2.20 4.45 2.95	 4.50 3.00	4.7 4.55 3.05	V	
V_{TRIP4}	V4MON Trip Point Voltage All Versions	0.85 0.85	 0.90	3.5 0.95	V	
VREF	Voltage Reference Long Term Drift	0		-100	mV	10 years
AC Characteristics						
t_{MR}(3)	Minimum time high for reset valid on the MR pin	5			µs	
t_{MRE}(3)	Delay from MR enable to $\overline{V1GDO}$ LOW			1.6	µs	
$t_{\overline{RESET}\_E}$(3)	Delay from ViFAIL to $\overline{RESET}$ valid LOW			1	µs	
t_{DPOR}(3)	Internal Device Delay on Power up	45	50	55	ms	
t_{TO}(3)	ViFAIL turn off time		50		ns	

ELECTRICAL CHARACTERISTICS (Programmable Parameters)

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{SPOR}	Delay before $\overline{RESET}$ assertion					
	TPOR1 = 0 TPOR0 = 0	90	100	110	ms	Factory Default
	TPOR1 = 0 TPOR0 = 1	450	500	550	ms	(3)
	TPOR1 = 1 TPOR0 = 0	0.9	1	1.1	s	(3)
	TPOR1 = 1 TPOR0 = 1	4.5	5	5.5	s	(3)
t_{DELAYi}	Time Delay used in Power Sequencing (i = 1, 4)					
	TiD1 = 0 TiD0 = 0	90	100	110	ms	Factory Default
	TiD1 = 0 TiD0 = 1	450	500	550	ms	(3)
	TiD1 = 1 TiD0 = 0	0.9	1	1.1	s	(3)
	TiD1 = 1 TiD0 = 1	4.5	5	5.5	s	(3)

EQUIVALENT A.C. OUTPUT LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Output load	Standard output load

Figure 1. Initial Power up Timing

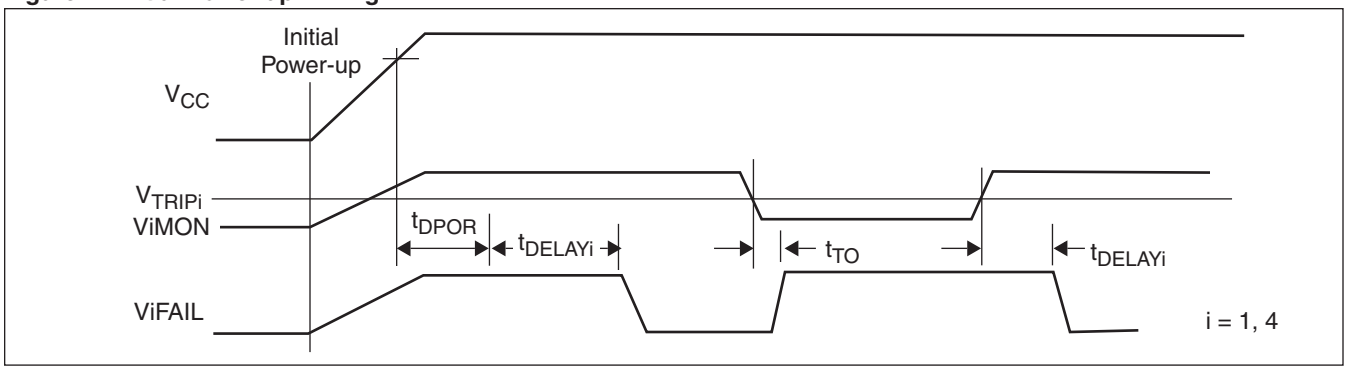


Figure 2. Manual Reset (MR)

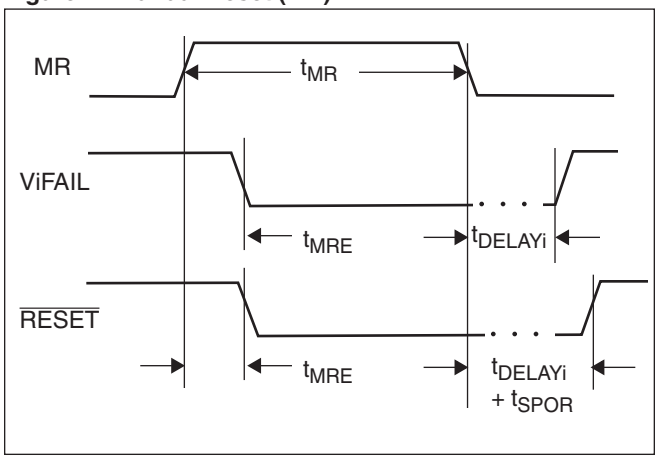
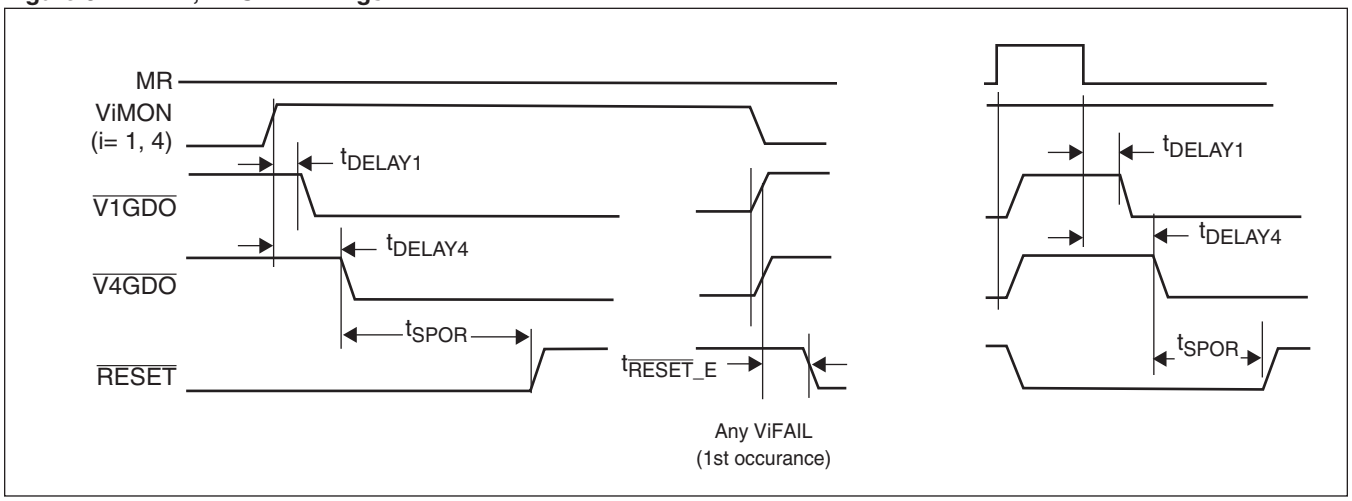


Figure 3. ViFAIL, $\overline{\text{RESET}}$ Timings



SERIAL INTERFACE

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics						
I_{CC1}	Active Supply Current (V_{CC}) Read or Write to Memory or CRs			2.5	mA	$V_{IL} = V_{CC}$ x 0.1 $V_{IH} = V_{CC}$ x 0.9, f_{SCL} = 400kHz
I_{LI}	Input Leakage Current (SCL, WP, A0, A1)			10	µA	V_{IL} = GND to V_{CC}
I_{LO}	Output Leakage Current (SDA)			10	µA	V_{SDA} = GND to V_{CC} Device is in Standby
V_{IL}	Input LOW Voltage (SDA, SCL, WP, A0, A1)	-0.5		5 x 0.3	V	
V_{IH}	Input HIGH Voltage (SDA, SCL, WP, A0, A1)	5 x 0.7		5.5	V	
V_{HYS}	Schmitt Trigger Input Hysteresis • Fixed input level • V_{CC} related level	 0.2 .05 x 5			 V V	
V_{OL}	Output LOW Voltage (SDA)			0.4	V	I_{OL} = 4.0 mA
AC Characteristics						
f_{SCL}	SCL Clock Frequency			400	kHz	
t_{IN}	Pulse width Suppression Time at inputs	50			ns	
t_{AA}[(1)]	SCL LOW to SDA Data Out Valid	0.1		1.5	µs	
t_{BUF}[(1)]	Time the bus is free before start of new transmission	1.3			µs	
t_{LOW}	Clock LOW Time	1.3			µs	
t_{HIGH}	Clock HIGH Time	0.6			µs	
$t_{SU:STA}$	Start Condition Setup Time	0.6			µs	
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs	
$t_{SU:DAT}$	Data In Setup Time	100			ns	
$t_{HD:DAT}$	Data In Hold Time	0			µs	

SERIAL INTERFACE (Continued)

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs	
t_{DH}(1)	Data Output Hold Time	50			ns	
t_R(1)	SDA and SCL Rise Time	20 +.1Cb		300	ns	
t_F(1)	SDA and SCL Fall Time	20 +.1Cb		300	ns	
$t_{SU:WP}$	WP Setup Time	0.6			µs	
$t_{HD:WP}$	WP Hold Time	0			µs	
$t_{SU:ADR}$	A0, A1 Setup Time	0.6			µs	
$t_{HD:ADR}$	A0, A1 Hold Time	0			µs	
$t_{SU:VP}$	V_P Setup Time	0.6			µs	
Cb(3)	Capacitive load for each bus line			400	pF	
t_{WC}(2)	EEPROM Write Cycle Time		5	10	ms	

Note: (1) This parameter is based on characterization data.
(2) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
(3) This parameter is not 100% tested.

TIMING DIAGRAMS

Figure 4. Bus Timing

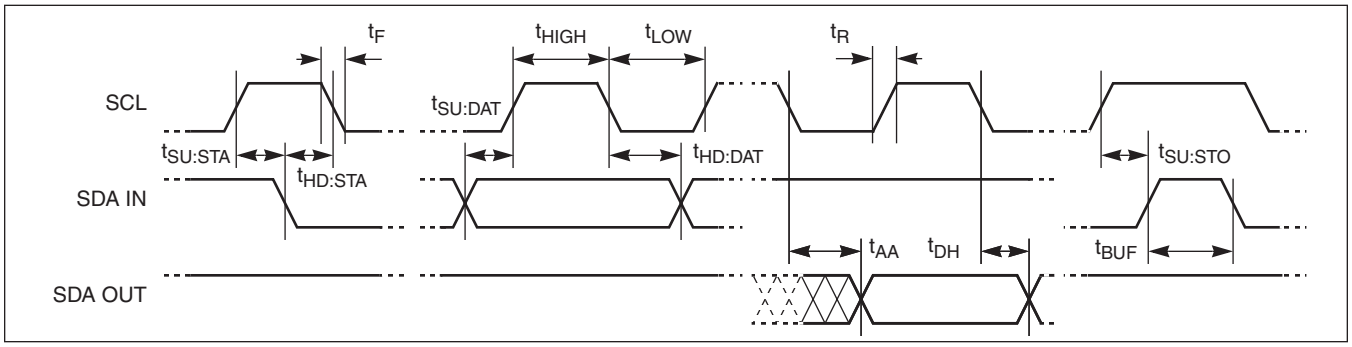


Figure 5. WP, A0, A1, V_P Pin Timing

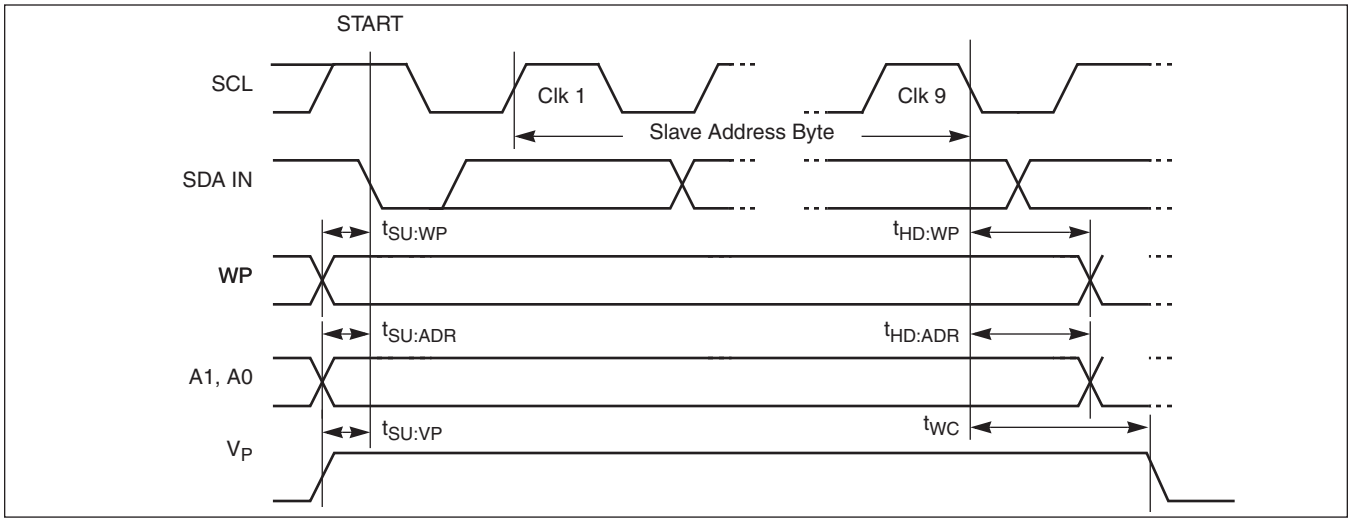
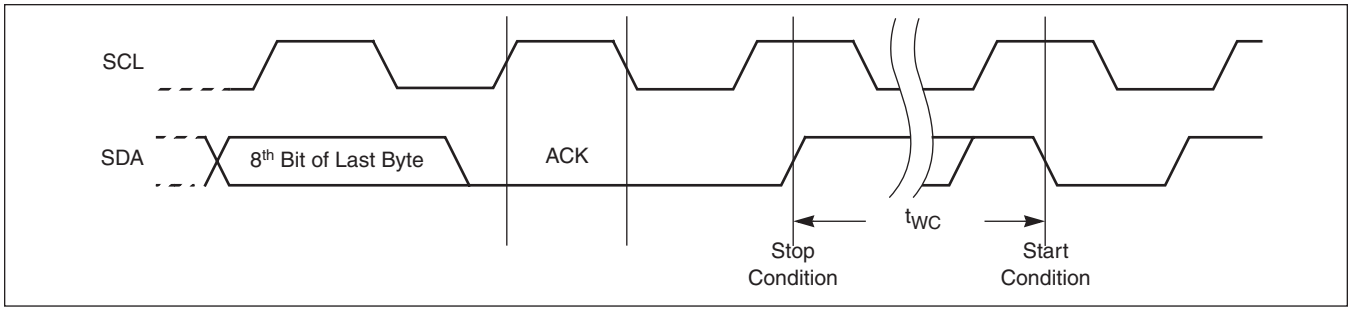


Figure 6. Write Cycle Timing

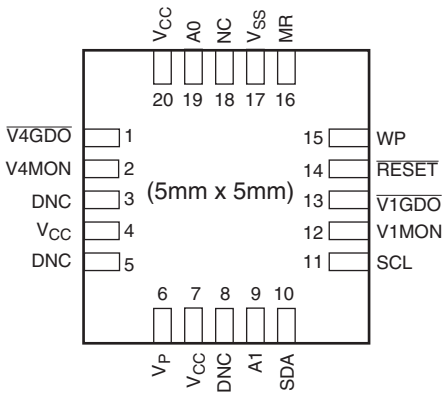


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known

PIN CONFIGURATION

X80120/21



PIN DESCRIPTIONS

Pin	Name	Description
1	$\overline{V4GDO}$	**V4 Voltage Good Delay Output (Active LOW).** This open drain output goes HIGH when V4MON is less than V_{REF4} and goes LOW when V4MON is greater than V_{REF4}. There is user selectable delay circuitry on this pin.
2	V4MON	**V4 Voltage Monitor Input.** Second voltage monitor pin. If unused connect to V_{CC}.
3	DNC	**Do Not Connect**
4	V_{CC}	**Connect to V_{CC}.**
5	DNC	**Do Not Connect**
6	V_P	**EEPROM programming Voltage.**
7	V_{CC}	**Connect to V_{CC}.**
8	DNC	**Do Not Connect.**
9	A1	Address Select Input. It has an internal pull-down resistor. (>10MΩ typical) The A0 and A1 bits allow for up to 4 X80120 devices to be used on the same SMBus serial interface.
10	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated).
11	SCL	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output.
12	V1MON	**V1 Voltage Monitor Input.** First voltage monitor pin. If unused connect to V_{CC}.
13	$\overline{V1GDO}$	**V1 Voltage Good Delay Output (Active LOW).** This open drain output goes HIGH when V1MON is less than V_{REF1} and goes LOW when V1MON is greater than V_{REF1}. There is user selectable delay circuitry on this pin.
14	$\overline{RESET}$	**RESET Output.** This open drain pin is an active LOW output. This pin will be active until all $\overline{ViGDO}$ pins go inactive and the power sequencing is complete. This pin will be released after a programmable delay.
15	WP	**Write Protect. Input Pin.** WP HIGH (in conjunction with WPEN bit=1) prevents writes to any memory location in the device. It has an internal pull-down resistor. (>10MΩ typical)
16	MR	**Manual Reset.** Pulling the MR pin HIGH initiates a RESET. The MR signal must be held HIGH for 5µsecs. It has an internal pull-down resistor. (>10MΩ typical)
17	V_{SS}	**Ground Input.**
18	NC	**No Connect.** No internal connections.
19	A0	**Address Select Input.** It has an internal pull-down resistor. (>10MΩ typical) The A0 and A1 bits allow for up to 4 X80120 devices to be used on the same SMBus serial interface.
20	V_{CC}	Supply Voltage.

FUNCTIONAL DESCRIPTION

Power On Reset and System Reset With Delay

Application of power to the X80120 activates a Power On Reset circuit that pulls the $\overline{RESET}$ pin active. This signal, if used, prevents the system microprocessor from starting to operate while there is insufficient voltage on any of the supplies. This circuit also does the following:

– It prevents the processor from operating prior to stabilization of the oscillator.
– It allows time for an FPGA to download its configuration prior to initialization of the circuit.
– It prevents communication to the EEPROM during unstable power conditions, greatly reducing the likelihood of data corruption on power up.
– It allows time for all supplies to turn on and stabilize prior to system initialization.

The POR/RESET circuit is activatived when all voltages are within specified ranges and the $\overline{V1GDO}$ and $\overline{V4GDO}$ time-out conditions are met. The POR/RESET circuit will then wait t_{SPOR} and de-assert the $\overline{RESET}$ pin. The POR delay may be changed by setting the TPOR bits in register CR2. The delay can be set to 100 ms, 500 ms, 1 second, or 5 seconds.

Table 1. POR RESET Delay Options

TPOR1	TPOR0	t_{SPOR} delay before $\overline{RESET}$ assertion
0	0	100 miliseconds (default)
0	1	500 miliseconds
1	0	1 second
1	1	5 seconds

Manual Reset

The manual reset option allows a hardware reset of the power sequencing pins. These can be used to recover the system in the event of an abnormal operating condition. Activating the MR pin for more than 5µs sets all of the ViFAIL outputs and the $\overline{RESET}$ output active (LOW). When MR is released (and if all supplies are still at their proper operating voltage) then the ViFAIL and $\overline{RESET}$ pins will be released after their programmed delay periods. (See

Dual Voltage Monitoring

X80120 monitors 2 voltage inputs. When the V1MON or V4MON input is detected to be above the input threshold, the respective output ($\overline{V1GDO}$ or $\overline{V4GDO}$) goes inactive (LOW). The ViFAIL signal is de-asserted after a delay of 100ms. This delay can be changed on each ViFAIL output individually with bits in register CR3. The delay can be 100ms, 500ms, 1s and 5s. Each ViFAIL signal remains active until its associated ViMON input rises above the threshold.

Table 2. $\overline{ViFAIL}$ output Time Delay Options

TiD1	TiD0	t_{DELAYi}
0	0	100ms (default)
0	1	500ms
1	0	1 secs
1	1	5 secs

where i is the specific voltage monitor (i = 1, 4).

Fault Detection

The X80120 contains a Fault Detection Register (FDR) that provides the user the status of the causes for a $\overline{RESET}$ pin active (See Table 20).

At power-up, the FDR is defaulted to all “0”. The system needs to initialize the register to all “1” before the actual monitoring can take place. In the event that any one of the monitored sources fail, the corresponding bit in the register changes from a “1” to a “0” to indicate the failure. When a RESET is detected by the main controller, the controller should read the FDR and note the cause of the fault. After reading the register, the controller can reset the register bit back to all “1” in preparation for future failure conditions.

Flexible Power Sequencing of Multiple Power Supplies

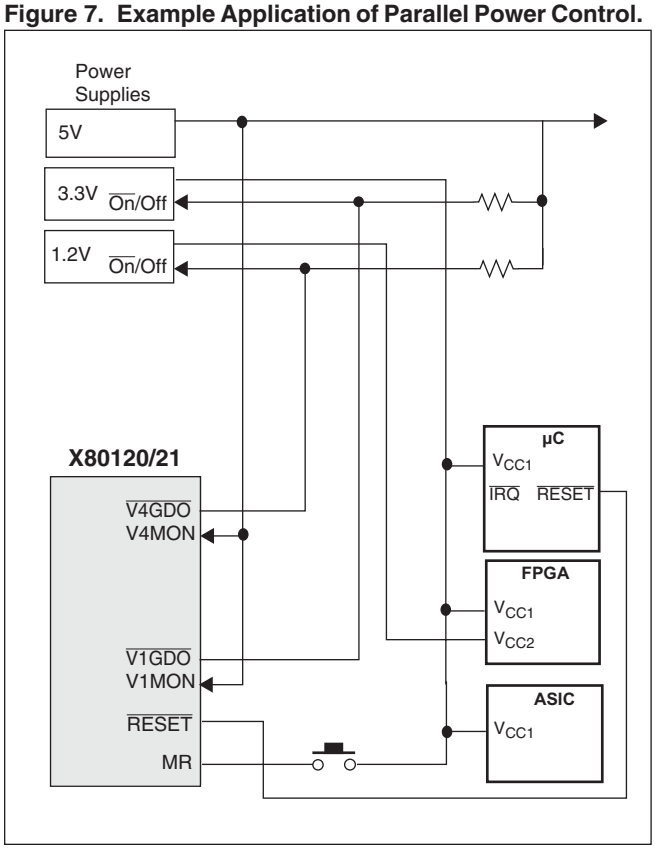
The X80120 provides several circuits such as multiple voltage monitors, programmable delays, and output drive signals that can be used to set up flexible power monitoring or sequencing schemes system power supplies. Below are two examples:

1) Power Up of Supplies In Parallel Using Programmable Delays. (See Figure 7 and Figure 8).

   The X80120 monitors several power supplies, powered by the same source voltage, that all begin power up at the same time. Each voltage source is fed into the ViMON inputs to the X80120. The ViMON inputs monitor the voltage to make sure it has reached the minimum desired level. When each voltage monitor determines that its input is good, a counter starts. After the programmed delay time, the X80120 sets the ViFAIL signals LOW. The ViFAIL signals can be wire ORed together and tied to an interrupt on the microcontroller. Any individual voltage failure can be viewed in the Fault Detection Register.

   In the factory default condition, each voltage monitor is instructed to go LOW 100ms after the the input voltage reaches its threshold. However, each ViFAIL delay is individually selectable as 100ms, 500ms, 1s and 5s. The delay times are chaged via the SMBus during calibration of the system.

Figure 7. Example Application of Parallel Power Control.



2) Power Up of Supplies Via Relay Sequencing Using Voltage Monitors (see Figure 10 and Figure 9).

Several power supplies and their respective power up start times can be controlled using the X80120 such that each of the power supplies will start in a relay sequencing fashion. In the following example, the 1st supply is allowed to power up when the input regulated supply reaches an acceptable threshold. Subsequent supplies power up after the prior supply has reached its operating voltage. This configuration ensures that each subsequent power supply turns on after the preceding supplies voltage output is valid. Again, the X80120 offers programmable delays for each voltage monitor and this delay is selectable via the SMBus during calibration of the system.

Figure 8. Parallel Power Control - Timing

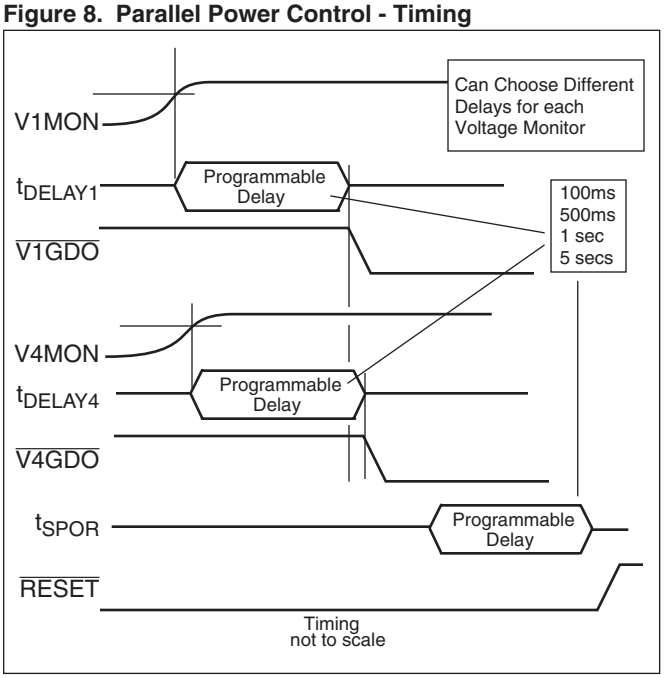


Figure 9. Example of Relay Power Supply Sequencing

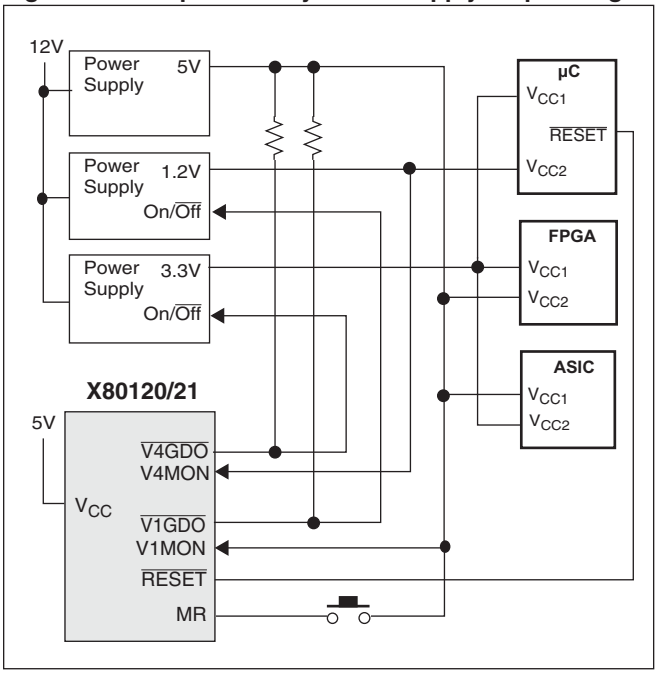
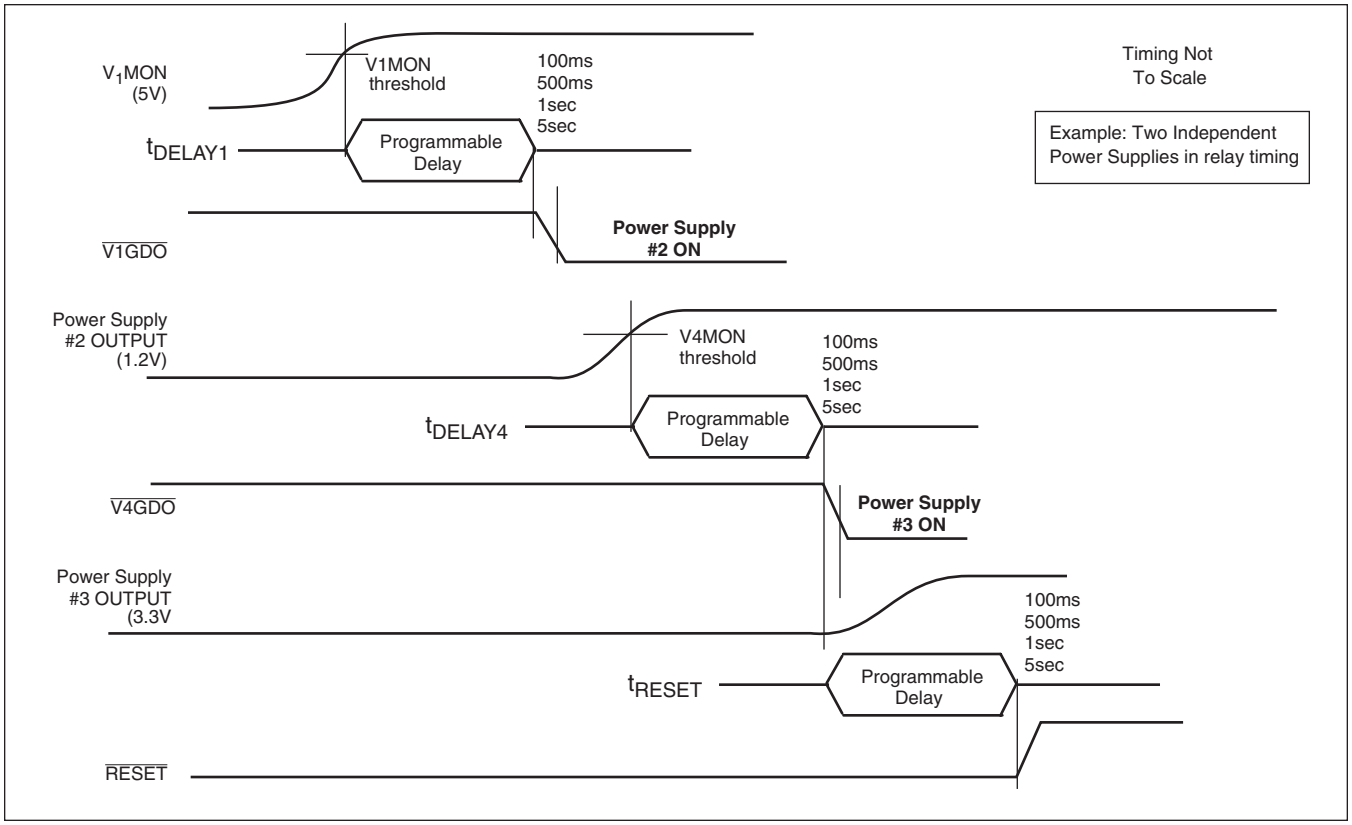


Figure 10.Relay Sequencing of DC-DC Supplies. (Timing)



CONTROL REGISTERS AND MEMORY

The user addressable internal control, status and memory components of the X80120 can be split up into three parts:

– Control Register (CR)
– Fault Detection Register (FDR)
– EEPROM array

Registers

The Control Registers and Fault Detection Register are summarized in Table 4. Changing bits in these registers change the operation of the device or clear fault conditions. Reading bits from these registers provides information about device configuration or fault conditions. Reads and writes are done through the SMBus serial port.

All of the Control Register bits are nonvolatile (except for the WEL bit), so they do not change when power is removed.

The values of the Register Block can be read at any time by performing a random read (see Serial Interface) at the specific byte address location. Only one byte is read by each register read operation.

Bits in the registers can be modified by performing a single byte write operation directly to the address of the register and only one data byte can change for each register write operation.EEPROM Array

The X80120 contains a 2kbit EEPROM memory array. This array can contain information about manufacturing location and dates, board configuration, fault conditions, service history, etc. Access to this memory is through the SMBus serial port. Read and write operations are similar to those of the control registers, but a single command can write up to 16 bytes at one time. A single read command can return the entire contents of the EEPROM memory.

Register and memory protection

In order to reduce the possibility of inadvertent changes to either a control register of the contents of memory, several protection mechanisms are built into the X80120. These are a Write Enable Latch, Block Protect bits, a Write Protect Enable bit and a Write Protect pin.

WEL: Write Enable Latch

A write enable latch (WEL) bit controls write accesses to the nonvolatile registers and the EEPROM memory array in the X80120. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address (registers or memory) will be ignored. The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register 0 (CR0). It is important to write only 00h or 80h to the CR0 register.

Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again.

Note, a write to FDR or RSR does not require that WEL=1.

BP1 and BP0: Block Protect Bits

The Block Protect Bits, BP1 and BP0, determines which blocks of the memory array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of four segments of the array.

BP1	BP0	Protected Addresses (Size)	Array Lock
0	0	None (Default)	None (Default)
0	1	C0h - FFh (64 bytes)	Upper 1/4
1	0	80h - FFh (128 bytes)	Upper 1/2
1	1	00h - FFh (256 bytes)	All

WPEN: Write Protect Enable

The Write Protect pin and Write Protect Enable bit in the CR1 register control the Programmable Hardware Write Protect feature. Hardware Protection is enabled when the WP pin is HIGH and WPEN bit is HIGH and disabled when WP pin is LOW or the WPEN bit is LOW. When the chip is Hardware Write Protected, non-volatile writes to all control registers (CR1, CR2, CR3, and CR4) are disabled including BP bits, the WPEN bit itself, and the blocked sections in the memory Array. Only the section of the memory array that are not block protected can be written.

Non voltatile Programming Voltage (V_P)

Nonvolatile writes require that a programming voltage be applied to the VP for the duration of a nonvolatile write operation.

Table 3. Write Protect Conditions

WEL	WP	WPEN	Memory Array NOT Block Protected	Memory Array Block Protected	Writes to CR1, CR2, CR3, CR4	Protection
LOW	X	X	Writes Blocked	Writes Blocked	Writes Blocked	Hardware
HIGH	LOW	X	Writes Enabled	Writes Blocked	Writes Enabled	Software
HIGH	X	LOW	Writes Enabled	Writes Blocked	Writes Enabled	Software
HIGH	HIGH	HIGH	Writes Enabled	Writes Blocked	Writes Blocked	Hardware

Table 4. Register Address Map

Byte Addr.	Name	Controi/Status	Bit								Memory Type
			7	6	5	4	3	2	1	0	
00H	CR0	Write Enable	WEL	0	0	0	0	0	0	0	Volatile
01H	CR1	EEPROM Block Control	WPEN	0	0	BP1	BP0	0	0	0	EEPROM
02H	CR2	POR Timing	0	0	0	0	TPOR1	TPOR0	0	0	EEPROM
03H	CR3	ViFAIL TIme Delay	T4D1	T4D0	0	0	0	0	T1D1	T1D0	EEPROM
FF	FDR	Fault Detection Register	0	0	0	0	V40S	0	0	V10S	Volatile

Table 5. Hardware/Software Control and Fault Detection Bits Summary

Operation	Control/ Status Bits	Location(s)		Description (See Functional for Details)
		Register	Bits	
Software Control Bits				
EEPROM Write Enable	WEL	CR0	7	WEL = 1 enables write operations to the controi registers and EEPROM. WEL = 0 prevents write operations.
EEPROM Write Protect	WPEN	CR1	7	WPEN = 1 (and WP pin HIGH) prevents writes to the control registers and the EEPROM.
EEPROM Block Protect	BP1 BP0	CR1	4:3	BP1=0, BP0=0 : No EEPROM memory protected. BP1=0, BP0=1 : Upper 1/4 of EEPROMmemory protected BP1=1, BP0=0 : Upper 1/2 of EEPROM memory protected. BP1=1, BP0=1 : All of EEPROM memory protected.
$\overline{\text{RESET}}$ Time Delay	TPOR0 TPOR1	CR2	3:2	TPOR1=0, TPOR0=0 : $\overline{\text{RESET}}$ delay = 100ms TPOR1=0, TPOR0=1 : $\overline{\text{RESET}}$ delay = 500ms TPOR1=1, TPOR0=0 : $\overline{\text{RESET}}$ delay = 1s TPOR1=1, TPOR0=1 : $\overline{\text{RESET}}$ delay = 5s
$\overline{\text{V1GDO}}$ Time Delay	T1D0 T1D1	CR3	1:0	TiD1=0, TiD0=0 : ViFAIL delay = 100ms TiD1=0, TiD0=1 : ViFAIL delay = 500ms TiD1=1, TiD0=0 : ViFAIL delay = 1s TiD1=1, TiD0=1 : ViFAIL delay = 5s
$\overline{\text{V4GDO}}$ Time Delay	T4D0 T4D1	CR3	7:6	
Status Bits				
1st Voltage Monitor	V1OS	FDR	0	V1OS = 0 : $\overline{\text{V1GDO}}$ pin has been asserted (must be preset to 1).
4th Voltage Monitor	V4OS	FDR	4	V4OS = 0 : $\overline{\text{V4GDO}}$ pin has been asserted (must be preset to 1).

BUS INTERFACE INFORMATION

Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 11.

Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 12.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the Slave Address Byte when the Device Identifier and/or Select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

Figure 11.Valid Start and Stop Conditions

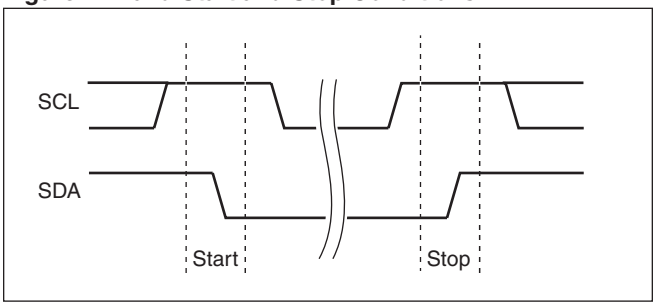
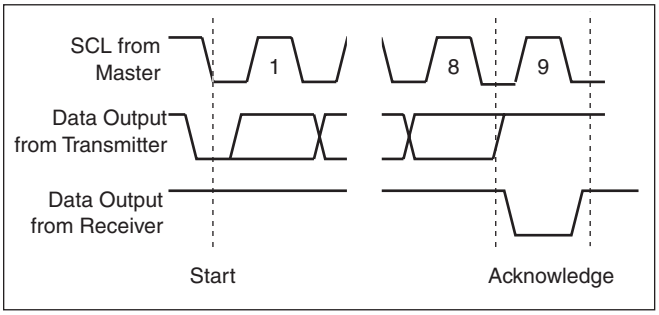


Figure 12.Acknowledge Response From Receiver



DEVICE ADDRESSING

Addressing Protocol Overview

Depending upon the operation to be performed on each of these individual parts, a 1, 2 or 3 Byte protocol is used. All operations however must begin with the Slave Address Byte being clocked into the SMBus port on the SCL and SDA pins. The Slave address selects the part of the device to be addressed, and specifies if a Read or Write operation is to be performed.

Slave Address Byte

Following a START condition, the master must output a Slave Address Byte. This byte consists of three parts:

– The Device Type Identifier which consists of the most significant four bits of the Slave Address (SA7 - SA4). The Device Type Identifier MUST be set to 1010 in order to select the device.

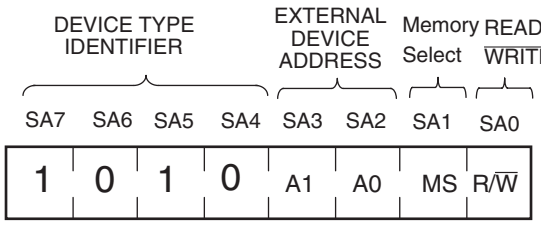
– The next two bits (SA3 - SA2) are slave address bits. The bits received via the SMBus are compared to A0 and A1 pins and must match or the communication is aborted.

– The next bit, SA1, selects the device memory sector. There

are two addressable sectors: the memory array and the control, fault detection and remote shutdown registers.

– The Least Significant Bit of the Slave Address (SA0) Byte is the R/W bit. This bit defines the operation to be performed. When the R/W bit is “1”, then a READ operation is selected. A “0” selects a WRITE operation (Refer toFigure 13).

Figure 13.Slave Address Format



Internal Address (SA1)	Internally Addressed Device
0	EEPROM Array
1	Control Register, Fault Detection Register

Bit SA0	Operation
0	WRITE
1	READ

Serial Write Operations

Before any write operations can be performed, a programming supply voltage (V_P) must be supplied. This voltage is only needed for programming, but the nonvolatile registers and EEPROM locations cannot be programmed without it.

In order to successfully complete a write operation to either a Control Register or the EEPROM array, the Write Enable Latch (WEL) bit must first be set and either the WP pin or the WPEN bit must be LOW.

Writes to the WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

Byte Write

For a write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance.

A write to a protected block of memory will suppress the acknowledge bit.

Page Write

The device is capable of a page write operation. See Figure 14. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page. See Figure 15.

This means that the master can write 16 bytes to the page starting at any location on that page. If the master begins writing at location 10, and loads 12 bytes, then the first 6 bytes are written to locations 10 through 15, and the last 6 bytes are written to locations 0 through 5. Afterwards, the address counter would point to location 6 of the page that was just written. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time.

The master terminates the Data Byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle.

Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

Acknowledge Polling

The disabling of the inputs during high voltage cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master’s byte load operation, the device initiates the internal high voltage cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the high voltage cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. See Figure 18.

Figure 14.Page Write Operation

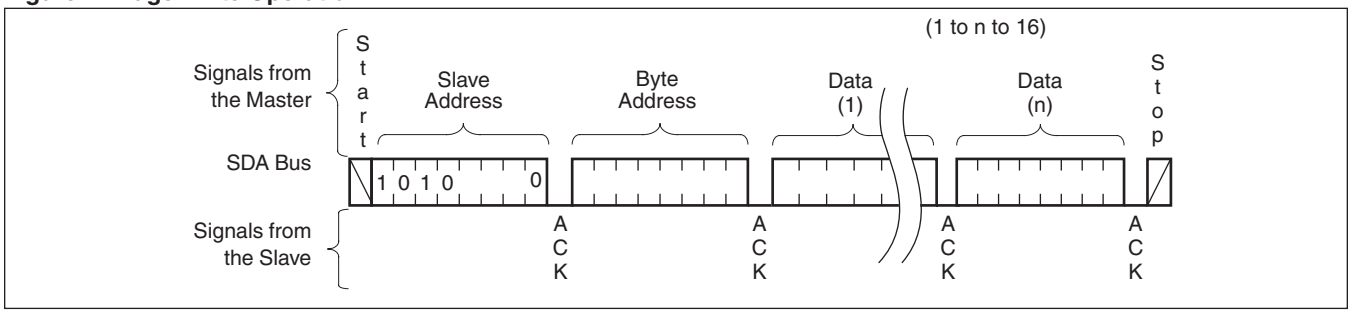


Figure 15.Writing 12 bytes to a 16-byte page starting at location 10.

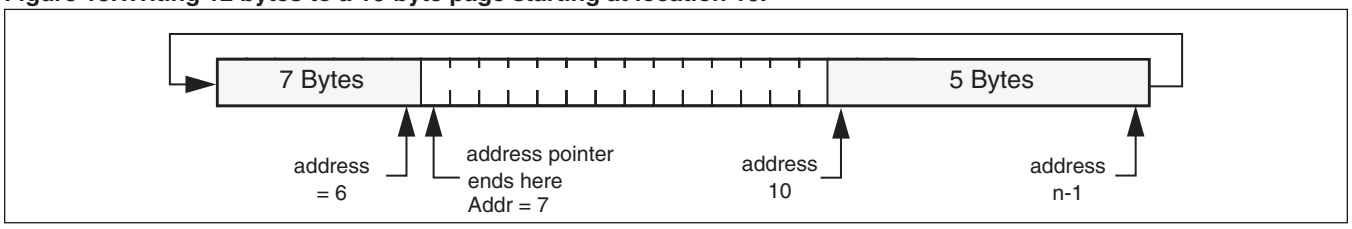


Figure 16.Random Address Read Sequence

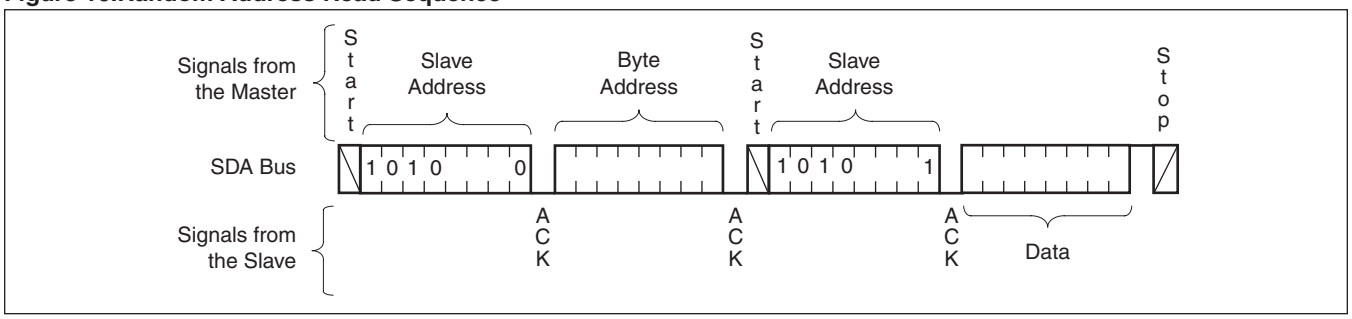


Figure 17.Current Address Read Sequence.

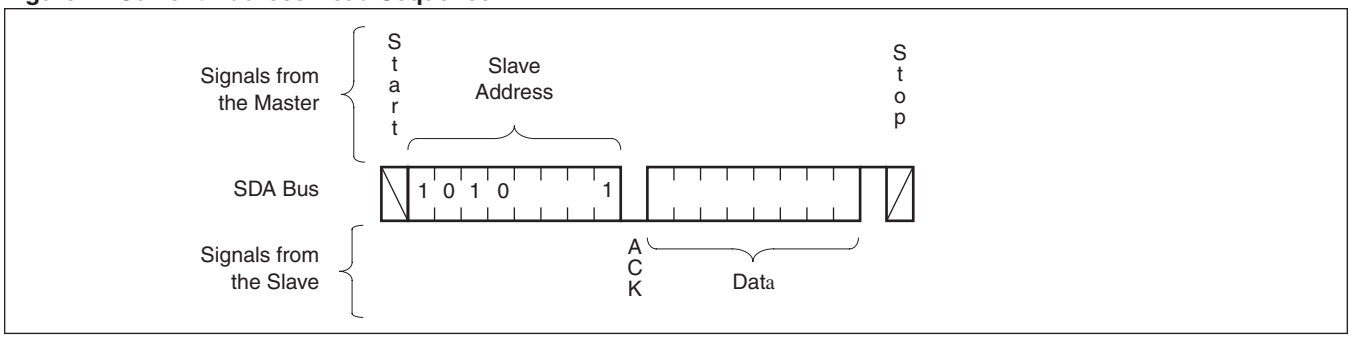
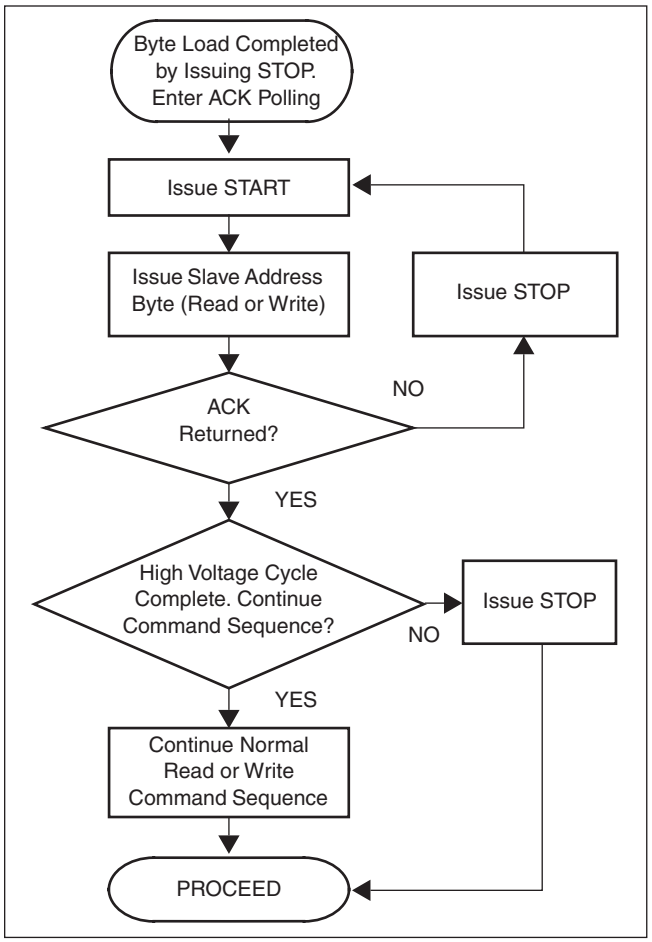


Figure 18.Acknowledge Polling Sequence



Serial Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. See Figure 16 for the address, acknowledge, and data transfer sequence.

Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. See Figure 17 or the address, acknowledge, and data transfer sequence.

Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.
– The WEL bit is set to '0'. In this state it is not possible to write to the device.
– SDA pin is the input mode.

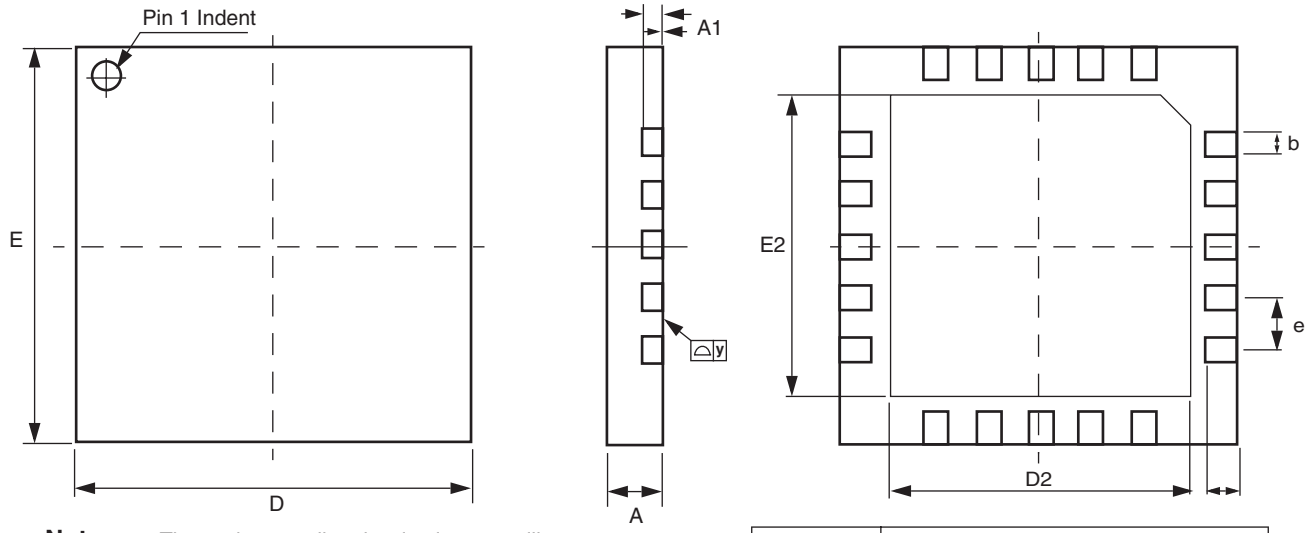
Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The WEL bit must be set to allow write operations.
– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.
– The WP pin, when held HIGH, prevents all writes to the array and all the Register.
– A programming voltage must be applied to the V_P pin prior to any programming sequence.

PACKAGING INFORMATION

20-Lead Quad Flat No Lead Package (Package Code: Q)
5mm x 5mm Body with 0.65mm Lead Pitch



Note: 1. The package outline drawing is compatilbe with JEDEC MO-220; variations: WHHC.

2. The terminal #1 identifier is a laser marked feature

Symbols	Dimensions in Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.23	0.30	0.38
C	0.19	0.20	0.25
D	4.90	5.00	5.10
D2	—	3.10	—
E	4.90	5.00	5.10
E2	—	3.10	—
e	—	0.65	—
L	0.35	0.55	0.75
y	0.00	—	0.076