

### X9315 Low Noise, Low Power, 32 Taps

#### Data Sheet

#### September 15, 2005

#### FN8179.1

# Digitally Controlled Potentiometer (XDCP™)

The Intersil X9315 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$  inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Control
- · Parameter Adjustments
- Signal Processing

#### Features

- · Solid-state potentiometer
- · 3-wire serial interface
- · 32 wiper tap points
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements
  - Temperature compensated
  - End to end resistance range ± 20%
  - Terminal voltage, 0 to V<sub>CC</sub>
- Low power CMOS
  - V<sub>CC</sub> = 2.7V or 5V
  - Active current, 50/400µA max.
  - Standby current, 1µA max.
- High reliability
  - Endurance, 100,000 data changes per bit
  - Register data retention, 100 years
- R<sub>TOTAL</sub> values = 10kΩ, 50kΩ, 100kΩ
- Packages
  - 8 Ld SOIC, MSOP and PDIP
- · Pb-free plus anneal available (RoHS compliant)

#### 5-Bit R<sub>H</sub>/V<sub>H</sub> 31 INC Up/Down V<sub>CC</sub> (Supply Voltage) Counter 30 29 R<sub>H</sub>/V<sub>H</sub> Up/Dowr (U/D 5-Bit 28 Control Increment (INC) Nonvolatile One $R_{W}/V_{W}$ and Memory Memory of Thirty Transfer Resistor **Device Select** Gates Two Arrav $(\overline{CS})$ $R_1/V_1$ Decoder 2 Store and V<sub>SS</sub> (Ground) Recall 1 V<sub>CC</sub> V<sub>SS</sub> Control General Circuitry 0 R<sub>I</sub>/V<sub>I</sub> R<sub>W</sub>/V<sub>W</sub> Detailed

#### CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures. 1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc. XDCP is a trademark of Intersil Americas Inc. Copyright Intersil Americas Inc. 2005. All Rights Reserved All other trademarks mentioned are the property of their respective owners.

## Block Diagram

# Ordering Information

R3315WM2" (Nole)     DDT       R3315WM1"     AAX       R3315WM1"     AAX       R3315WM1"     AAX       R3315WM12" (Nole)     AKW       R3315WM12" (Nole)     X8315WP       R3315WM1     X9315WP       R3315WS*     X9315W       R3315WM2" (Note)     X9315W       R3315WM2" (Note)     X9315W       R3315W1     X9315W       R3315W1     X9315W       R3315UM*     AEB       R3315UP     X9315UP	PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMP RANGE (°C)	PACKAGE
K9315WMI*     AAX       K9315WMI*     AAX       K9315WMI*     KNW       K9315WMI*     KNW       K9315WP     X9315WP       K9315WP     X9315WP       K9315WS*     X9315W       K9315UM*     X9315W       K9315UM*     AEB       K9315UM*     AEB       K9315UP1     X9315UP       K9315UP1     X9315UP       K9315UP1     X9315U       K9315US*     X9315U       K9315US*     X9315U       K9315US*     X9315U       K9315US*     X9315U       K9315US*     X9315U       K9315US*     X9315U       K9315TM*     AEJ	X9315WM*	AAW	5 ±10%	10	0 to 70	8 Ld MSOP
48315WMIZ* (Note)     AKW       48315WP     X9315WP       48315WP     X9315WP       48315WP     X9315WP       48315WS*     X9315W       48315UA*     X9315W       48315UA*     AEB       48315UP     X9315UP       48315UP     X9315UP       48315US*     X9315U       48315US*	X9315WMZ* (Note)	DDT			0 to 70	8 Ld MSOP (Pb-free)
x9315WP     x9315WP       x9315WP1     x9315WP1       x9315WP1     x9315W       x9315WS*     x9315W       x9315WA*     x9315W       x9315UM*     x9315UP       x9315UP     x9315UP       x9315UP     x9315UP       x9315UP     x9315UP       x9315UP     x9315U       x9315U     x9315	X9315WMI*	AAX			-40 to 85	8 Ld MSOP
(9315WPI     X9315WP I       (9315WPS*     X9315W       (9315W75*     X9315W       (9315W75**     X9315W       (9315W75**     X9315W       (9315W75**     X9315W       (9315W71**)     X9315W       (9315W71**)     X9315W       (9315W71**)     X9315W       (9315W7**)     X9315W       (9315W7**)     X9315W       (9315W7**)     N010***********************************	X9315WMIZ* (Note)	AKW			-40 to 85	8 Ld MSOP (Pb-free)
9315WS*     X9315W       9315WS2* (Note)     X9315W Z       9315WS2* (Note)     X9315W I       9315WS1*     X9315W I       9315UM2* (Note)     DDS       9315UM2* (Note)     DDS       9315UM2* (Note)     DDR       9315UM12* (Note)     DDR       9315UP1     X9315UP       9315US2* (Note)     X9315U I       9315US2* (Note)     X9315U I       9315US1*     X9315U I       9315U     -40 to 85     8 Ld SOIC (Pb-free)       9315U     -40 to 85     8 Ld SOIC (Pb-free)       9315U     -40 to 85     8 Ld MSOP (Pb-free)       9315T     9315T </td <td>X9315WP</td> <td>X9315WP</td> <td></td> <td></td> <td>0 to 70</td> <td>8 Ld PDIP</td>	X9315WP	X9315WP			0 to 70	8 Ld PDIP
Circle     X3315W Z       (G315WSZ* (Note)     X3315W I       (G315WS1* X3315W I     -40 to 85     8 Ld SOIC (Pb-free)       (G315WS12* (Note)     X3315W Z     -40 to 85     8 Ld SOIC (Pb-free)       (G315WS12* (Note)     X3315W Z     -40 to 85     8 Ld SOIC (Pb-free)       (G315UM2* (Note)     DDS     -40 to 85     8 Ld MSOP       (G315UM1*)     AEB     -40 to 85     8 Ld MSOP (Pb-free)       (G315UM1*)     AEB     -40 to 85     8 Ld MSOP (Pb-free)       (G315UM1*)     AEB     -40 to 85     8 Ld MSOP (Pb-free)       (G315UM1*)     X9315UP I     -40 to 85     8 Ld PDIP       (G315US1*)     X9315U Z     -40 to 85     8 Ld SOIC (Pb-free)       (G315US1*)     X9315U Z     -40 to 85     8 Ld SOIC (Pb-free)       (G315US1*)     X9315U Z     -40 to 85     8 Ld SOIC (Pb-free)       (G315US1*)     X9315U Z     -40 to 85     8 Ld MSOP       (G315US1*)     X9315U Z     -40 to 85     8 Ld MSOP (Pb-free)       (G315TM1*)     AEJ     -40 to 85     8 Ld MSOP (Pb-free)       (G315TM2*	X9315WPI	X9315WP I			-40 to 85	8 Ld PDIP
9315WSI*     X9315W I       9315WSI*     X9315W Z I       9315WSIZ* (Note)     X9315W Z I       9315UM*     DDS       9315UM2* (Note)     DDS       9315UM2* (Note)     DDS       9315UM2* (Note)     DDR       9315UM2* (Note)     DDR       9315UM2* (Note)     DDR       9315UM2* (Note)     DDR       9315UP1     X9315UP       9315US1*     X9315U P       9315US1*     X9315U P       9315US1*     X9315U Z       9315US1     440 to 85       9315US1*     X9315U Z       9315US1     440 to 85       9315TM2*	X9315WS*	X9315W			0 to 70	8 Ld SOIC
(9315WSIZ* (Note)     X9315W Z I       (9315UM2* (Note)     DDS       (9315UM2* (Note)     DDS       (9315UM1*)     AEB       (9315UM12* (Note)     DDR       (9315UM12* (Note)     DDR       (9315UM12* (Note)     DDR       (9315UM12* (Note)     DDR       (9315UP1     X9315UP       (9315US1*     X9315UP       (9315US1*     X9315U       (9315US1*     X9315U Z       (9315TM*     AEJ       (9315TM*     AEJ       (9315TM*     ADZ       (9315TM*     ADZ       (9315TP)     X9315T       (9315TP)     X9315T       (9315TP)     X9315T       (9315TS*     X9315T I       (9315TS*     X9315T I       (9315TS* <td< td=""><td>X9315WSZ* (Note)</td><td>X9315W Z</td><td></td><td></td><td>0 to 70</td><td>8 Ld SOIC (Pb-free)</td></td<>	X9315WSZ* (Note)	X9315W Z			0 to 70	8 Ld SOIC (Pb-free)
Seynomic     Seynomic	X9315WSI*	X9315W I			-40 to 85	8 Ld SOIC
K9315UMZ* (Note)     DDS       (9315UMI*     AEB       (9315UMI*     AEB       (9315UMIZ* (Note)     DDR       (9315UMIZ* (Note)     DDR       (9315UP     X9315UP       (9315UM1*     X9315UP       (9315UP     X9315UP       (9315US*     X9315U       (9315US*     X9315U       (9315US2* (Note)     X9315U       (9315US1*     X9315U I       (9315TM*     AEJ       (9315TM*     ADZ       (9315TM1*     ADZ       (9315TP1     X9315TP       (9315TP1     X9315TP       (9315TS*     X9315T       (9315TS*     X9315T Z       (9315TS*     X9315T I       (9315TS*     X9315T I	X9315WSIZ* (Note)	X9315W Z I			-40 to 85	8 Ld SOIC (Pb-free)
K9315UMI*     AEB       (9315UMI* (Note)     DDR       (9315UP     X9315UP       (9315UP     X9315UP       (9315UP1     X9315UP       (9315UP1     X9315UP       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US2* (Note)     X9315U       (9315US1*     X9315U       (9315US1*     X9315U Z       (9315US1*     X9315U Z       (9315US1*     X9315U Z       (9315US1*     X9315U Z       (9315TM*     AEJ       100     0 to 70     8 Ld SOIC (Pb-free)       (9315TM1*     ADZ       (9315TM1*     ADZ       (9315TP     X9315TP       (9315TP1     X9315TP       (9315TS*     X9315T       (9315TS*     X9315T I       (9315TS1*     X9315T I       (9315TS1*     X9315T I	X9315UM*		_	50	0 to 70	8 Ld MSOP
K9315UMIZ* (Note)     DDR       K9315UMIZ* (Note)     X9315UP       K9315UP1     X9315UP I       K9315UP1     X9315UP I       K9315US*     X9315U       K9315US*     X9315U       K9315US*     X9315U Z       K9315US1*     X9315U I       K9315US1*     X9315U I       K9315US1*     X9315U I       K9315US1*     X9315U Z I       K9315TM*     AEJ       K9315TM2* (Note)     DDN       K9315TM2* (Note)     DDN       K9315TM1*     ADZ       K9315TP     X9315TP       K9315TP1     X9315TP I       K9315TS*     X9315T Z       K9315TS*     X9315T Z       K9315TS*     X9315T Z       K9315TS*     X9315T Z       K9315TS1*     X9315T Z       K9315TS1*     X9315T I	X9315UMZ* (Note)	DDS			0 to 70	8 Ld MSOP (Pb-free)
K9315UP     X9315UP       (9315UP1     X9315UP1       (9315UP1     X9315UP1       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U Z       (9315US*     X9315U I       (9315US1*     X9315U Z       (9315US1*     X9315U Z       (9315US1*     X9315U Z       (9315TM*     AEJ       (9315TMZ* (Note)     DDN       (9315TMI*     ADZ       (9315TMI*     ADZ       (9315TP     X9315TP       (9315TP1     X9315TP 1       (9315TS*     X9315T Z       (9315TS1*     X9315T I       (9315TS1*     X9315T I	X9315UMI*	AEB			-40 to 85	8 Ld MSOP
K9315UPI     X9315UP I       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U       (9315US*     X9315U Z       (9315US1*     X9315U Z       (9315TM*     AEJ       (9315TM2* (Note)     DDN       (9315TM1*     ADZ       (9315TM1*     ADZ       (9315TP     X9315TP       (9315TP1     X9315TP       (9315TS*     X9315T       (9315TS*     X9315T       (9315TS1*     X9315T Z       (9315TS1*     X9315T I	X9315UMIZ* (Note)	DDR			-40 to 85	8 Ld MSOP (Pb-free)
K9315US*     X9315U       (9315US*     X9315U Z       (9315US*     X9315U Z       (9315US1*     X9315U I       (9315US1*     X9315U Z       (9315TM*     AEJ       (9315TM2* (Note)     DDN       (9315TM2* (Note)     DDN       (9315TM1*     ADZ       (9315TM1*     ADZ       (9315TP     X9315TP       (9315TP1     X9315TP       (9315TS*     X9315T       (9315TS1*     X9315T Z       (9315TS1*     X9315T I	X9315UP	X9315UP			0 to 70	8 Ld PDIP
K9315USZ* (Note)     X9315U Z       (9315USI*     X9315U I       (9315USI*     X9315U I       (9315USI* (Note)     X9315U Z       (9315USI* (Note)     X9315U Z I       (9315TM*     AEJ       (9315TM2* (Note)     DDN       (9315TM1*     ADZ       (9315TM1*     ADZ       (9315TM1*     ADZ       (9315TM2* (Note))     DDN       (9315TM1*     ADZ       (9315TM1*     X9315TP       (9315TM1*     X9315TP       (9315TM2* (Note))     DDL       (9315TS*     X9315TP I       (9315TS*     X9315T Z       (9315TS1*     X9315T Z       (9315TS1*     X9315T I	X9315UPI	X9315UP I			-40 to 85	8 Ld PDIP
K9315USI*     X9315U I       (9315USIZ* (Note)     X9315U Z I       (9315TM*     AEJ       (9315TMZ* (Note)     DDN       (9315TMZ* (Note)     DDN       (9315TMI*     ADZ       (9315TMI*     ADZ       (9315TMI* (Note)     DDL       (9315TMI* (Note)     DDL       (9315TMI* (Note)     DDL       (9315TMI* X9315TP     X9315TP       (9315TS1*     X9315TP I       (9315TS2* (Note)     X9315T Z       (9315TS1*     X9315T I	X9315US*	X9315U			0 to 70	8 Ld SOIC
K9315USIZ* (Note)     X9315U Z I       K9315TM*     AEJ       K9315TMZ* (Note)     DDN       K9315TMI*     ADZ       K9315TMI*     ADZ       K9315TMI*     DDL       K9315TMI*     DDL       K9315TMI*     X9315TP       K9315TMI*     X9315TP       K9315TMI*     X9315TP       K9315TMI*     X9315TP I       K9315TS*     X9315T Z       K9315TSZ* (Note)     X9315T Z       K9315TSI*     X9315T Z       K9315TSI*     X9315T I	X9315USZ* (Note)	X9315U Z			0 to 70	8 Ld SOIC (Pb-free)
K9315TM*     AEJ       K9315TMZ* (Note)     DDN       K9315TMI*     ADZ       K9315TMIZ* (Note)     DDL       K9315TMIZ* (Note)     DDL       K9315TP     X9315TP       K9315TSP     X9315TP       K9315TS*     X9315TP I       K9315TS2* (Note)     X9315T Z       K9315TS1*     X9315T I	X9315USI*	X9315U I			-40 to 85	8 Ld SOIC
K9315TMZ* (Note)     DDN       (9315TMI*     ADZ       (9315TMIZ* (Note)     DDL       (9315TMIZ* (Note))     DDL       (9315TP     X9315TP       (9315TP1     X9315TP I       (9315TS*     X9315TP I       (9315TS2* (Note))     X9315T Z       (9315TS1*     X9315T I       (9315TS1*     X9315T I	X9315USIZ* (Note)	X9315U Z I			-40 to 85	8 Ld SOIC (Pb-free)
K9315TMI*   ADZ     (9315TMIZ* (Note)   DDL     (9315TP   X9315TP     (9315TPI   X9315TP     (9315TS*   X9315TP     (9315TSZ* (Note)   X9315T Z     (9315TSI*   X9315T I     (9315TSI*   X9315T I	X9315TM*	AEJ	_	100	0 to 70	8 Ld MSOP
K9315TMIZ* (Note)     DDL       K9315TP     X9315TP       K9315TPI     X9315TP I       K9315TS*     X9315TP I       K9315TS*     X9315T       K9315TSZ* (Note)     X9315T Z       K9315TSI*     X9315T I       K9315TSI*     X9315T I	X9315TMZ* (Note)	DDN			0 to 70	8 Ld MSOP (Pb-free)
X9315TP     X9315TP       (9315TPI     X9315TP I       (9315TS*     X9315T       (9315TSZ* (Note)     X9315T Z       (9315TSI*     X9315T I       (9315TSI*     X9315T I	X9315TMI*	ADZ			-40 to 85	8 Ld MSOP
K9315TPI     X9315TP I       K9315TS*     X9315T       K9315TS*     X9315T       K9315TSZ* (Note)     X9315T Z       K9315TSI*     X9315T I	X9315TMIZ* (Note)	DDL			-40 to 85	8 Ld MSOP (Pb-free)
X9315TS*     X9315T       (9315TSZ* (Note))     X9315T Z       (9315TSI*     X9315T I       0 to 70     8 Ld SOIC (Pb-free)       -40 to 85     8 Ld SOIC	X9315TP	X9315TP			0 to 70	8 Ld PDIP
X9315TSZ* (Note)     X9315T Z     0 to 70     8 Ld SOIC (Pb-free)       <9315TSI*	X9315TPI	X9315TP I			-40 to 85	8 Ld PDIP
40 to 85     8 Ld SOIC	X9315TS*	X9315T			0 to 70	8 Ld SOIC
	X9315TSZ* (Note)	X9315T Z			0 to 70	8 Ld SOIC (Pb-free)
(9315TSIZ* (Note)     X9315T Z I     -40 to 85     8 Ld SOIC (Pb-free)	X9315TSI*	X9315T I			-40 to 85	8 Ld SOIC
	X9315TSIZ* (Note)	X9315T Z I			-40 to 85	8 Ld SOIC (Pb-free)

### **Ordering Information** (Continued)

PART NUMBER	PART MARKING	V <sub>CC</sub> LIMITS (V)	R <sub>TOTAL</sub> (kΩ)	TEMP RANGE (°C)	PACKAGE
X9315TP-2.7	X9315TP F	2.7-5.5	10	0 to 70	8 Ld PDIP
X9315TPI-2.7	X9315TP G			-40 to 85	8 Ld PDIP
X9315WM-2.7*	AAU			0 to 70	8 Ld MSOP
X9315WMZ-2.7* (Note)	AOI			0 to 70	8 Ld MSOP (Pb-free)
X9315WMI-2.7*	AAV			-40 to 85	8 Ld MSOP
X9315WMIZ-2.7* (Note)				-40 to 85	8 Ld MSOP (Pb-free)
X9315WP-2.7	X9315WP F			0 to 70	8 Ld PDIP
X9315WPI-2.7	X9315WP G			-40 to 85	8 Ld PDIP
X9315WS-2.7*	X9315W F			0 to 70	8 Ld SOIC
X9315WSZ-2.7* (Note)	X9315W Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315WSI-2.7*	X9315W G			-40 to 85	8 Ld SOIC
X9315WSIZ-2.7* (Note)	X9315W Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9315UM-2.7*	AEK		50	0 to 70	8 Ld MSOP
X9315UMZ-2.7* (Note)	AKU			0 to 70	8 Ld MSOP (Pb-free)
X9315UMI-2.7*	AEA			-40 to 85	8 Ld MSOP
X9315UMIZ-2.7* (Note)	AJG			-40 to 85	8 Ld MSOP (Pb-free)
X9315UP-2.7				0 to 70	8 Ld PDIP
X9315UPI-2.7				-40 to 85	8 Ld PDIP
X9315US-2.7*	X9315U F			0 to 70	8 Ld SOIC
X9315USZ-2.7* (Note)	X9315U Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315USI-2.7*	X9315U G			-40 to 85	8 Ld SOIC
X9315USIZ-2.7* (Note)	X9315U Z G			-40 to 85	8 Ld SOIC (Pb-free)
X9315TM-2.7*	AEI		100	0 to 70	8 Ld MSOP
X9315TMZ-2.7* (Note)	DDP			0 to 70	8 Ld MSOP (Pb-free)
X9315TMI-2.7*	ADY			-40 to 85	8 Ld MSOP
X9315TMIZ-2.7* (Note)	DDM			-40 to 85	8 Ld MSOP (Pb-free)
X9315TS-2.7*	X9315T F			0 to 70	8 Ld SOIC
X9315TSZ-2.7* (Note)	X9315T Z F			0 to 70	8 Ld SOIC (Pb-free)
X9315TSI-2.7*	X9315T G			-40 to 85	8 Ld SOIC
X9315TSIZ-2.7* (Note)	X9315T Z G			-40 to 85	8 Ld SOIC (Pb-free)

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

\*Add "T1" suffix for tape and reel.

### **Pin Descriptions**

### $R_H/V_H$ and $R_L/V_L$

The high (R<sub>H</sub>/V<sub>H</sub>) and low (R<sub>L</sub>/V<sub>L</sub>) terminals of the X9315 are equivalent to the fixed terminals of a mechanical potentiometer. The minimum voltage is V<sub>SS</sub> and the maximum is V<sub>CC</sub>. The terminology of R<sub>L</sub>/V<sub>L</sub> and R<sub>H</sub>/V<sub>H</sub> references the relative position of the terminal in relation to wiper movement direction selected by the U/D input, and not the voltage potential on the terminal.

### $R_w/V_w$

 $R_W/V_W$  is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs. The wiper terminal series resistance is typically 200 $\Omega$  at V<sub>CC</sub> = 5V.

### Up/Down (U/D)

The  $U/\overline{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

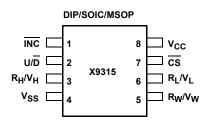
### Increment (INC)

The  $\overline{\text{INC}}$  input is negative-edge triggered. Toggling  $\overline{\text{INC}}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\overline{D}$  input.

### Chip Select (CS)

The device is selected when the  $\overline{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\overline{CS}$  is returned HIGH while the  $\overline{INC}$  input is also HIGH. After the store operation is complete the X9315 will be placed in the low power standby mode until the device is selected once again.

### Pin Configuration



### Pin Names

SYMBOL	DESCRIPTION
R <sub>H</sub> /V <sub>H</sub>	High terminal
R <sub>W</sub> /V <sub>W</sub>	Wiper terminal
R <sub>L</sub> /V <sub>L</sub>	Low terminal
V <sub>SS</sub>	Ground
V <sub>CC</sub>	Supply voltage
U/D	Up/Down control input

Pin Names

SYMBOL	DESCRIPTION
INC	Increment control input
CS	Chip Select control input

### Principles of Operation

There are three sections of the X9315: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a "make before break" mode when the wiper changes tap positions. If the wiper is moved several positions, multiple taps are connected to the wiper for  $t_{IW}$  (INC to  $V_W$  change). The  $R_{TOTAL}$  value for the device can temporarily be reduced by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

### Instructions and Programming

The  $\overline{INC}$ ,  $U/\overline{D}$  and  $\overline{CS}$  inputs control the movement of the wiper along the resistor array. With  $\overline{CS}$  set LOW the device is selected and enabled to respond to the  $U/\overline{D}$  and  $\overline{INC}$  inputs. HIGH to LOW transitions on  $\overline{INC}$  will increment or decrement (depending on the state of the  $U/\overline{D}$  input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever  $\overline{\text{CS}}$  transitions HIGH while the  $\overline{\text{INC}}$  input is also HIGH.

The system may select the X9315, move the wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep INC LOW while taking CS HIGH. The new wiper position will be maintained until

changed by the system or until a power-up/down cycle recalled the previously stored data.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, etc...

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

### Mode Selection

CS	INC	U/D	MODE	
L		Н	Wiper Up	
L	1	L	Wiper Down	
	Н	Х	Store Wiper Position	
Н	Х	Х	Standby Current	
	L	Х	No Store, Return to Standby	

### Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

#### **Absolute Maximum Ratings**

Temperature under bias65°C to +135°C
Storage temperature65°C to +150°C
Voltage on CS, INC, U/D, VH, VL and
V <sub>CC</sub> with respect to V <sub>SS</sub> 1V to +7V
$\Delta V =  V_{H} - V_{L}  \dots \dots$
Lead temperature (soldering 10 seconds)
$I_W$ (10 seconds)±7.5mA

#### **Recommended Operating Conditions**

Temperature (Commercial)	0°C to +70°C
Temperature (Industrial)	40°C to +85°C
Supply Voltage (V <sub>CC</sub> ) (Note 4) Limits	
X9315	5V ± 10%
X9315-2.7	2.7V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Potentiometer Characteristics (Over recommended operating conditions unless otherwise					
				LIM	IITS
SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	TYP	м

				LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	ТҮР	MAX.	UNIT	
	End to end resistance tolerance				±20	%	
$V_{VH}$	V <sub>H</sub> terminal voltage		0		V <sub>CC</sub>	V	
V <sub>VL</sub>	V <sub>L</sub> terminal voltage		0		V <sub>CC</sub>	V	
	Power rating	$R_{TOTAL} \geq 10 k \Omega$			10	mW	
R <sub>W</sub>	Wiper resistance	I <sub>W</sub> = 1mA, V <sub>CC</sub> = 5V		200	400	Ω	
R <sub>W</sub>	Wiper resistance	I <sub>W</sub> = 1mA, V <sub>CC</sub> = 2.7V		400	1000	Ω	
IW	Wiper current				±3.75	mA	
	Noise	Ref: 1kHz		-120		dBV	
	Resolution			3		%	
	Absolute linearity <sup>(1)</sup>	Vw(n)(actual) - Vw(n)(expected)			±1	MI <sup>(3)</sup>	
	Relative linearity <sup>(2)</sup>	V <sub>w(n + 1)</sub> - [V <sub>w(n) + MI</sub> ]			±0.2	MI <sup>(3)</sup>	
	R <sub>TOTAL</sub> temperature coefficient			±300		ppm/°C	
	Ratiometric temperature coefficient				±20	ppm/°C	
C <sub>H</sub> /C <sub>L</sub> /C <sub>W</sub>	Potentiometer capacitances	See circuit #3		10/10/25		pF	

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage =  $(V_{w(n)}(actual) - V_{w(n)}(actual)) = \pm 1$  MI Maximum.

(2) Relative linearity is a measure of the error in step size between taps =  $R_{W(n+1)} - [R_{w(n)} + MI] = \pm 0.2 \text{ MI}.$ 

(3) 1 MI = Minimum Increment =  $R_{TOT}/31$ .

(4) Typical values are for  $T_A = 25^{\circ}C$  and nominal supply voltage.

(5) This parameter is periodically sampled and not 100% tested

#### DC Electrical Specifications (Over recommended operating conditions unless otherwise specified.

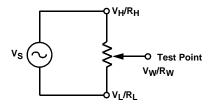
			LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	ТҮР <sup>(4)</sup>	MAX	UNIT
I <sub>CC1</sub>	V <sub>CC</sub> active current (Increment)	$\overline{\text{CS}} = \text{V}_{\text{IL}}, \text{U/}\overline{\text{D}} = \text{V}_{\text{IL}} \text{ or } \text{V}_{\text{IH}} \text{ and } \overline{\text{INC}} = 0.4\text{V}$ @ max. t <sub>CYC</sub>			50	μA
I <sub>CC2</sub>	V <sub>CC</sub> active current (Store) (EEPROM Store)	$\overline{\text{CS}} = \text{V}_{\text{IH}}, \text{U}/\overline{\text{D}} = \text{V}_{\text{IL}} \text{ or } \text{V}_{\text{IH}} \text{ and } \overline{\text{INC}} = \text{V}_{\text{IH}}$ @ max. t <sub>WR</sub>			400	μA
I <sub>SB</sub>	Standby supply current	$\overline{\text{CS}}$ = V <sub>CC</sub> - 0.3V, U/ $\overline{\text{D}}$ and $\overline{\text{INC}}$ = V <sub>SS</sub> or V <sub>CC</sub> - 0.3V			1	μA
ILI	CS, INC, U/D input leakage current	$V_{IN} = V_{SS}$ to $V_{CC}$			±10	μA
V <sub>IH</sub>	CS, INC, U/D input HIGH voltage		V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	CS, INC, U/D input LOW voltage		-0.5		V <sub>CC</sub> x 0.1	V
C <sub>IN</sub> (5)	$\overline{CS}$ , $\overline{INC}$ , U/ $\overline{D}$ input capacitance	$V_{CC}$ = 5V, $V_{IN}$ = $V_{SS}$ , $T_A$ = 25°C, f = 1MHz			10	pF

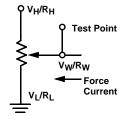
#### Endurance and Data Retention

PARAMETER	MIN	UNIT
Minimum endurance	100,000	Data changes per bit
Data retention	100	Years

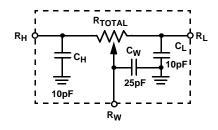
Test Circuit #1

#### Test Circuit #2





#### Circuit #3 SPICE Macro Model



### **AC Conditions of Test**

Input pulse levels	0V to 3V	
Input rise and fall times	10ns	
Input reference levels	1.5V	

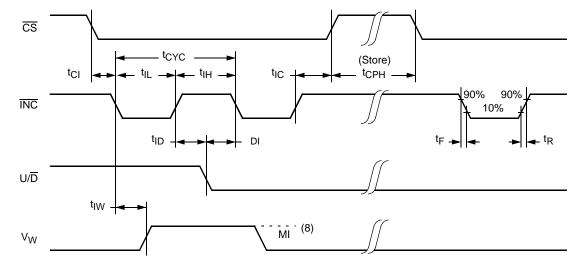
#### AC Electrical Specifications (Over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER		LIMITS		
		MIN	ТҮР(6)	MAX	UNIT
t <sub>CI</sub>	CS to INC setup	100			ns
t <sub>ID</sub>	INC HIGH to U/D change	100			ns
t <sub>DI</sub>	U/D to INC setup	2.9			μs
t <sub>IL</sub>	INC LOW period	1			μs
t <sub>IH</sub>	INC HIGH period	1			μs
t <sub>IC</sub>	INC Inactive to CS inactive	1			μs
t <sub>CPH</sub>	CS Deselect time (NO STORE)	100			ns
t <sub>CPH</sub>	CS Deselect time (STORE)	10			ms
t <sub>IW</sub>	INC to Vw change		1	5	μs
tCYC	INC cycle time	4			μs
t <sub>R,</sub> t <sub>F</sub> (7)	INC input rise and fall time			500	μs
t <sub>PU</sub> (7)	Power-up to wiper stable			5	μs
$t_{R} V_{CC}(7)$	V <sub>CC</sub> power-up rate	0.2		50	V/ms
t <sub>WR</sub>	Store cycle		5	10	ms

### Power-up and Down Requirements

There are no restrictions on the power-up or power-down conditions of V<sub>CC</sub> and the voltages applied to the potentiometer pins provided that V<sub>CC</sub> is always more positive than or equal to V<sub>H</sub>, V<sub>L</sub>, and V<sub>W</sub>, i.e., V<sub>CC</sub>  $\geq$  V<sub>H</sub>, V<sub>L</sub>, V<sub>W</sub>. The V<sub>CC</sub> ramp rate spec is always in effect.

### AC Timing

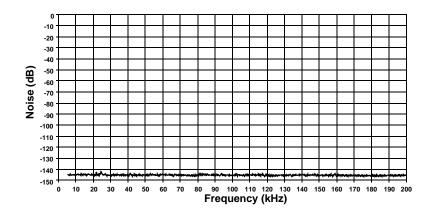


Notes: (6) Typical values are for  $T_A = 25^{\circ}C$  and nominal supply voltage.

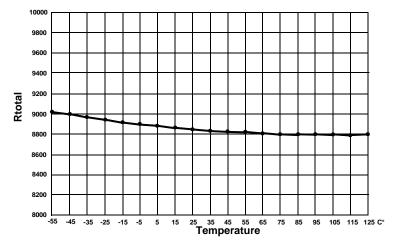
- (7) This parameter is not 100% tested.
- (8) MI in the A.C. timing diagram refers to the minimum incremental change in the V<sub>W</sub> output due to a change in the wiper position.

### Performance Characteristics (Typical)

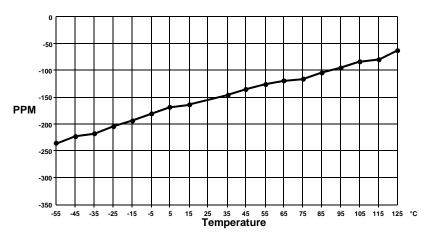
#### **Typical Noise**

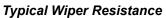


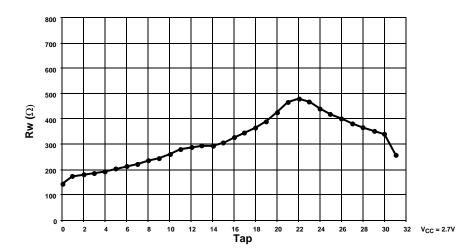
### Typical Rtotal vs. Temperature



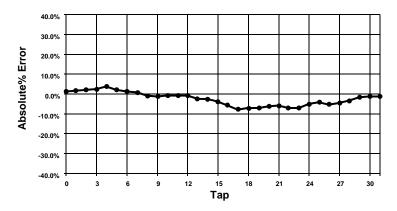
Typical Total Resistance Temperature Coefficient



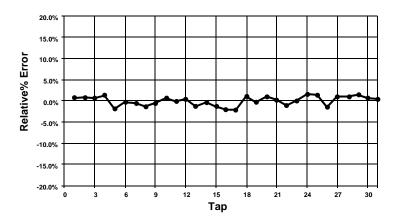




Typical Absolute% Error per Tap Position



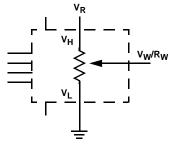
Typical Relative% Error per Tap Position



### Applications Information

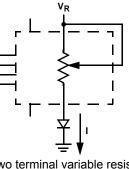
Electronic digitally controlled (XDCP) potentiometers provide three powerful application advantages; (1) the variability and reliability of a solid-state potentiometer, (2) the flexibility of computer-based digital controls, and (3) the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

#### **Basic Configurations of Electronic Potentiometers**

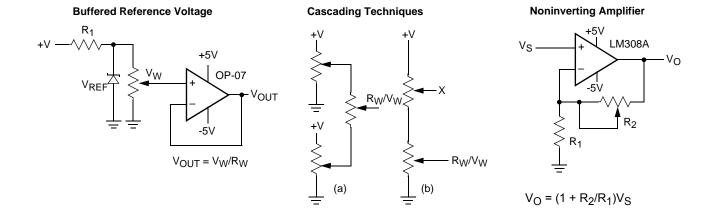


Three terminal potentiometer; variable voltage divider

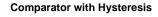
### **Basic Circuits**

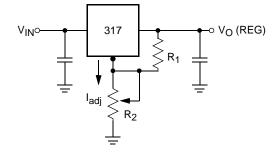


Two terminal variable resistor; variable current

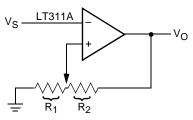


Voltage Regulator



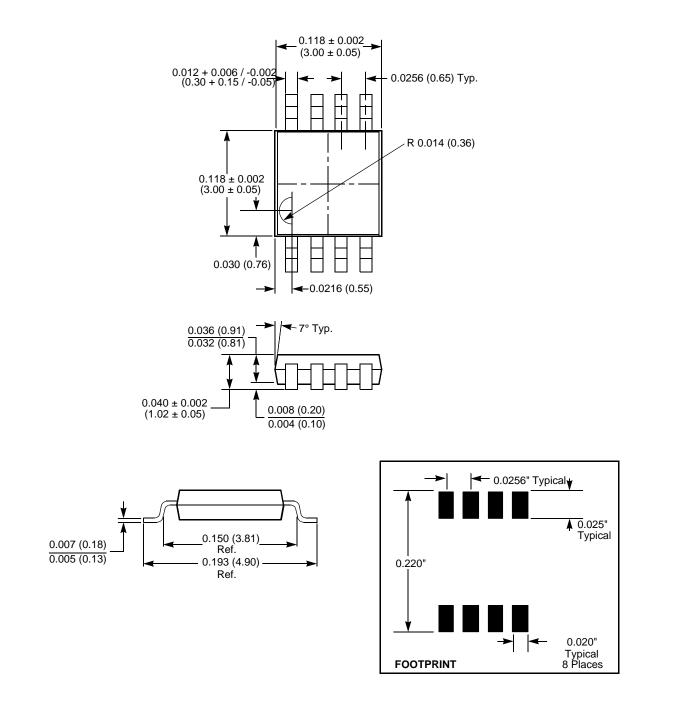


 $V_{O}$  (REG) = 1.25V (1 + R<sub>2</sub>/R<sub>1</sub>) + I<sub>adj</sub> R<sub>2</sub>



(for additional circuits see AN115)

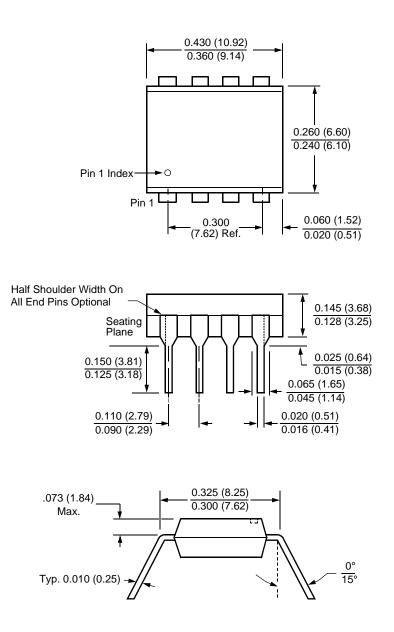
### **Packaging Information**



8-Lead Miniature Small Outline Gull Wing Package Type M

NOTE: 1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

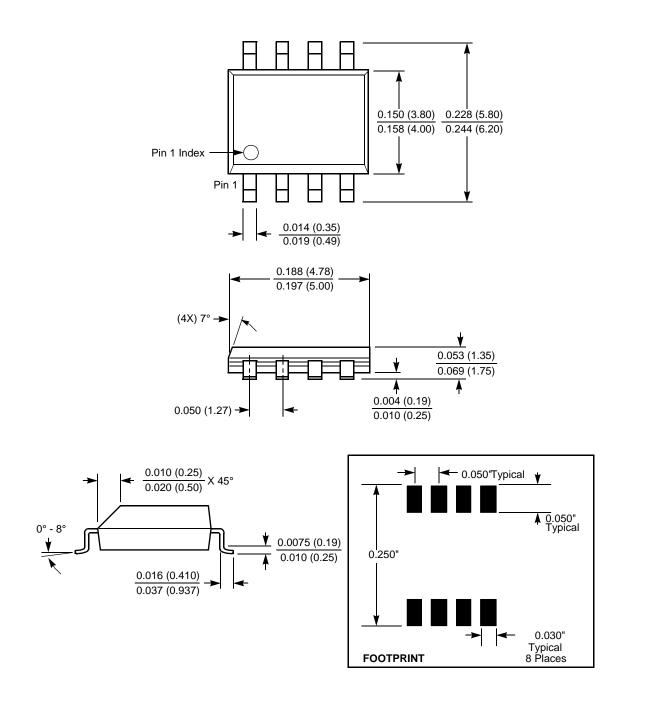
### Packaging Information



### 8-Lead Plastic Dual In-Line Package Type P



### **Packaging Information**



#### 8-Lead Plastic Small Outline Gull Wing Package Type S

#### NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com