2K/4K/8K bit Serial I²C bus EEPROM

DESCRIPTION

The CW24C02A/04A/08A provides 2048/4096/8192 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 256/512/1024 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The CW24C02A/04A/08A is accessed via a two-wire serial interface and is available in 1.7V (1.7V to 5.5V) version.

FEATURES

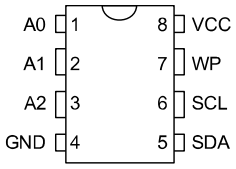
- Wide Voltage Operation V_{CC} = 1.7V to 5.5V
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized:
  - CW24C02A, 256 × 8 (2K bits)
  - CW24C04A, 512 × 8 (4K bits)
  - CW24C08A, 1024 × 8 (8K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz (5V, 3V), 400 KHz (1.7V) Compatibility
- 8-byte Page (CW24C02A),
  16-byte Page (CW24C04A/08A) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (4 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- PDIP8, SOP8, TSSOP8, UDFN8, CPC8, SOT23-5 Packages

APPLICATIONS

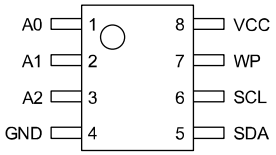
- Intelligent Instrument
- Household Appliance
- Automotive Electronics
- Communications
- Consumer electronic

PIN CONFIGURATION

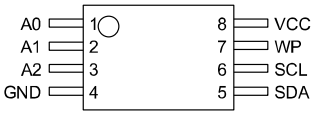
PDIP8



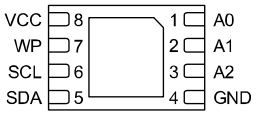
SOP8



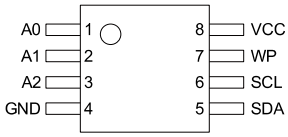
TSSOP8



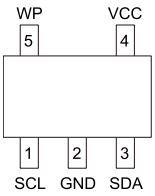
UDFN8 (bottom view)



CPC8



SOT23-5

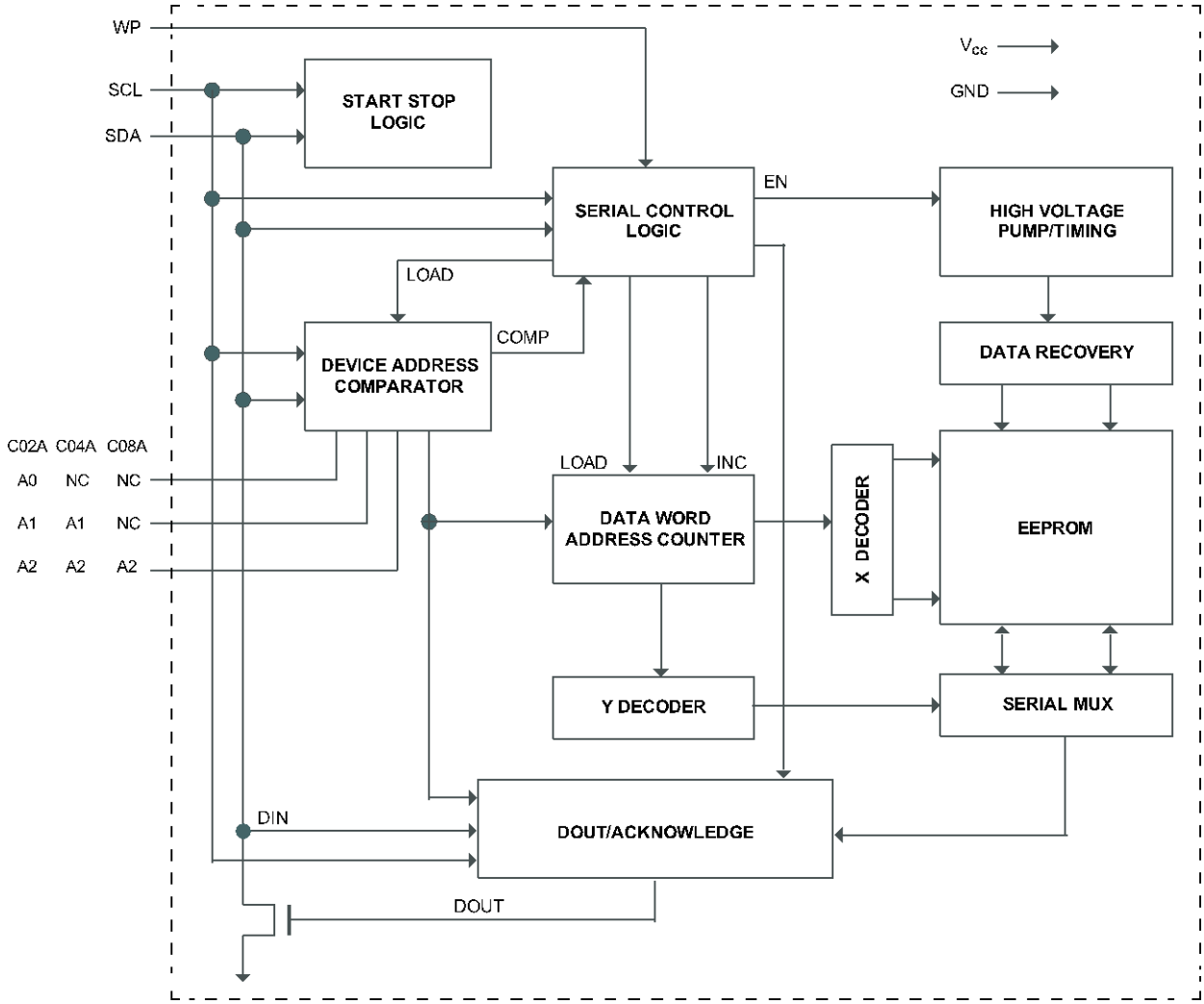


ORDERING INFORMATION

Temperature Range	Package		Orderable Device	Package Qty.
-40°C ~ +85°C	Pb-Free	PDIP8	CW24CXXXP	50 Units/Tube
		SOP8	CW24CXXXD	100 Units/Tube
			CW24CXXXDR	3000 Units/R&T
		TSSOP8	CW24CXXXT	100 Units/Tube
			CW24CXXXTR	4000 Units/R&T
		UDFN8	CW24CXXXUR	4000 Units/R&T
		CPC8	CW24CXXXCR	15K Units/R&T
		SOT23-5	CW24CXXXS5R	3000 Units/R&T

XXX= 02A/04A/08A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Maximum Ratings are those values beyond which damage to the device may occur.)

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.3 ~ + 6.5	V
DC Input Voltage	V_{IN}	GND - 0.3 ~ V_{CC} + 0.3	V
DC Output Voltage	V_{OUT}	GND - 0.3 ~ V_{CC} + 0.3	V
Operating Ambient Temperature	T_a	-55 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

(Functional operation should be restricted to the Recommended Operating Conditions.)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	1.7	5.5	V
Operating Temperature	T_A	-40	+85	°C

CAPACITANCE

(Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.7V)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input/Output Capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0V	-	8	pF
Input Capacitance (A0, A1, A2, SCL)	C_{IN}	V_{IN} = 0V	-	6	pF

DC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage	V_{CC}	-		1.7	-	5.5	V
Supply Current	I_{CC}	V_{CC} = 5V	Read at 400kHz	-	0.4	2.0	mA
			Write at 400kHz	-	1.5	2.0	mA
Standby Current	I_{SB}	V_{IN} = V_{CC} / GND, V_{CC}=1.7V		-	0.6	1.0	µA
		V_{IN} = V_{CC} / GND, V_{CC}=2.5V			1.0	2.0	µA
		V_{IN} = V_{CC} / GND, V_{CC}=5.5V		-	1.5	2.0	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND		-	0.10	2.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or GND		-	0.05	2.0	µA
Input Low Level	V_{IL}	V_{CC} = 1.8V to 5.5V		-0.3	-	V_{CC}x0.3	V
		V_{CC} = 1.7V		-0.3	-	V_{CC}x0.2	
Input High Level	V_{IH}	V_{CC} = 1.7V to 5.5V		V_{CC}x0.7	-	V_{CC}+0.3	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low Level	V_{OL3}	V_{CC} = 5.0V, I_{OL} = 3.0 mA	-	-	0.4	V
	V_{OL2}	V_{CC} = 3.0V, I_{OL} = 2.1 mA	-	-	0.4	V
	V_{OL1}	V_{CC} = 1.7V, I_{OL} = 0.15 mA	-	-	0.2	V

AC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, C_L = 1 TTL Gate and 100 pF unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Frequency, SCL	f_{SCL}	1.7V<V_{CC}<2.5V	-	-	400	kHz
		2.5V<V_{CC}<5.5V	-	-	1000	
Clock Pulse Width Low	t_{LOW}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.6	-	-	
Clock Pulse Width High	t_{HIGH}	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.4	-	-	
Noise Suppression Time	t_I	1.7V<V_{CC}<2.5V	-	-	50	ns
		2.5V<V_{CC}<5.5V	-	-	50	
Clock Low to Data Out Valid	t_{AA}	1.7V<V_{CC}<2.5V	0.1	-	0.9	μs
		2.5V<V_{CC}<5.5V	0.05	-	0.9	
Time the bus must be free before a new transmission can start	t_{BUF}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.5	-	-	
Start Hold Time	$t_{HD.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25	-	-	
Data In Hold Time	$t_{HD.DAT}$	1.7V<V_{CC}<5.5V	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	1.7V<V_{CC}<5.5V	100	-	-	ns
Inputs Rise Time	t_R	-	-	-	300	ns
Inputs Fall Time	t_F	-	-	-	300	ns
Stop Setup Time	$t_{SU.STO}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25	-	-	
Data Out Hold Time	t_{DH}	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	-	3.3	4	ms
5.0V,25°C,Byte Mode	Endurance	-	1M	-	-	Write Cycles

Note:

1. This parameter is characterized and is not 100% tested.
2. AC measurement condition :
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC};
   Input rise and fall time: 50 ns

Input and output timing reference voltages: 0.5 V_{CC}

The value of R_L should be concerned according to the actual loading on the user's system.

R_L (connects to V_{CC}): 1.3KΩ （2.5V,5V）, 10KΩ （1.7V）

PIN DESCRIPTION

No.		Name	Function Description
SOT23-5	Other packages		
-	1	A0 / NC	Address input. The A2, A1 and A0 pins are device address inputs that are hard wired for the CW24C02A. Eight CW24C02A devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). The CW24C04A uses the A2 and A1 inputs for hard wire addressing and a total of four CW24C04A devices may be addressed on a single bus system. The A0 pin is a no connect and can be connected to ground. The CW24C08A only uses the A2 input for hardwire addressing and a total of two CW24C08A devices may be addressed on a single bus system. The A0 and A1 pins are no connects and can be connected to ground.
-	2	A1 / NC	
-	3	A2	
2	4	GND	Circuit ground pin.
3	5	SDA	Serial address and data I/O. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.
1	6	SCL	Serial clock input. The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.
5	7	WP	Write protect. The WP pin that provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to V_{CC}, the write protection feature is enabled and read only.
4	8	VCC	Positive supply voltage.

MEMORY ORGANIZATION

Device	Total bits	Total pages	Bytes per page	Word address
CW24C02A	2K	32	8	8-bit
CW24C04A	4K	32	16	9-bit
CW24C08A	8K	64	16	10-bit

DEVICE OPERATION

Clock and data transitions

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

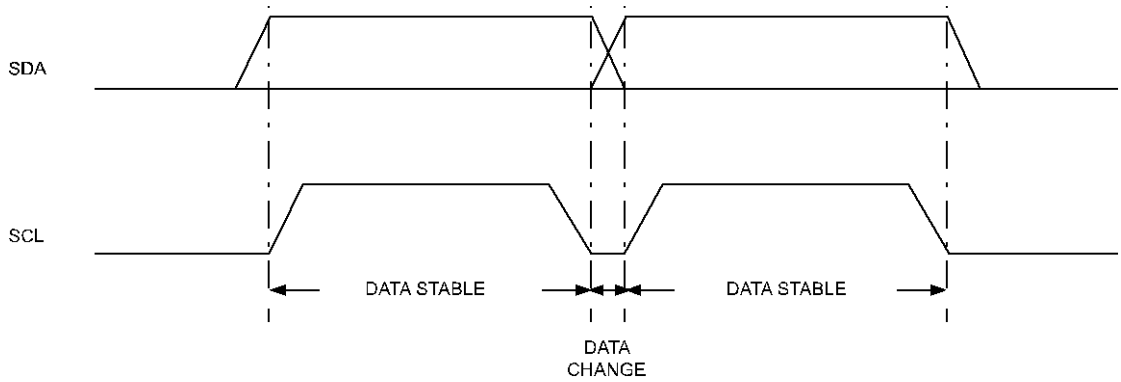


Figure 1. Data Validity

Start Conditions

A high-to-low transition of SDA with SCL high is a start condition which must precede any other Command. (see Figure 2)

Stop Conditions

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode. (see Figure 2)

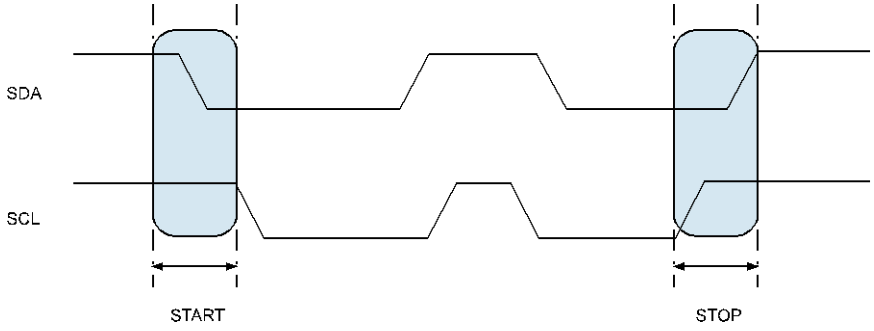


Figure 2. Start and Stop Definition

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Standby Mode

The CW24C02A/04A/08A features a low-power standby mode which is enabled:
(1) upon power-up and (2) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

(1) Clock up to 9 cycles.

(2) Look for SDA high in each cycle while SCL is high.

(3) Create a start condition.

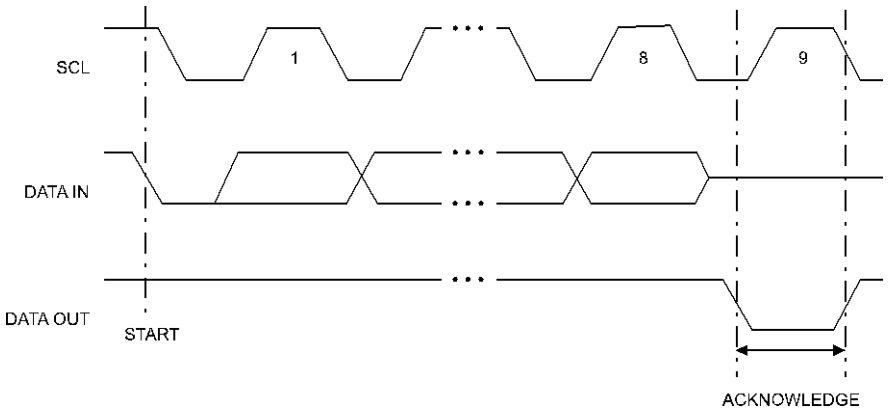


Figure 3. Output Acknowledge

DEVICE ADDRESSING

The CW24C02A/04A/08A devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the CW24C02A. These 3 bits must compare to their Corresponding hardwired input pins.

The CW24C04A only uses the A2 and A1 device address bits with the third bit being a memory page address bit. The two device address bits must compare to their corresponding hardwired input pins. The A0 pin is no connect.

The CW24C08A only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connect.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

CW24C02A	1	0	1	0	A2	A1	A0	R/W
	MSB							LSB
CW24C04A	1	0	1	0	A2	A1	P0	R/W
CW24C08A	1	0	1	0	A2	P1	P0	R/W

Figure 4. Device Address

WRITE OPERATIONS

Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

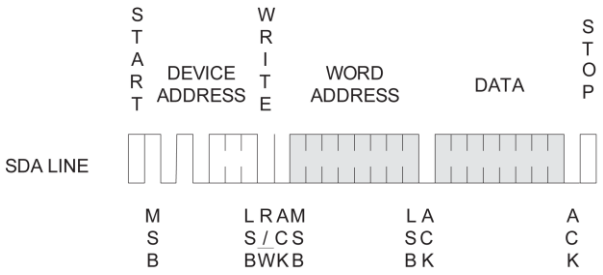


Figure 5. Byte Write

Page Write

The CW24C02A device is capable of an 8-byte page write, and the CW24C04A/08A devices are capable of 16-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 7 (CW24C02A) or 15 (CW24C04A/08A) more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

The data word address lower 3 (CW24C02A) or 4 (CW24C04A/08A) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same

page. If more than 8 (CW24C02A) or 16 (CW24C04A/08A) data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

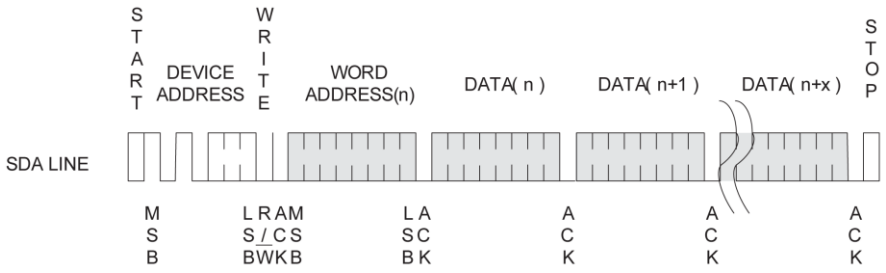


Figure 6. Page Write

Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

READ OPERATIONS

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

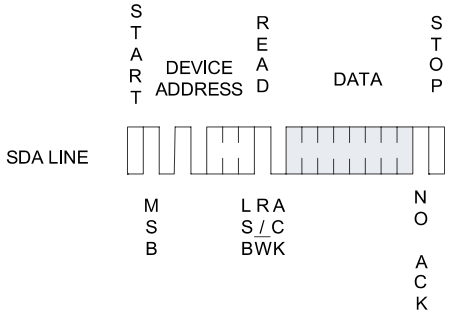


Figure 7. Current Address Read

Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8).

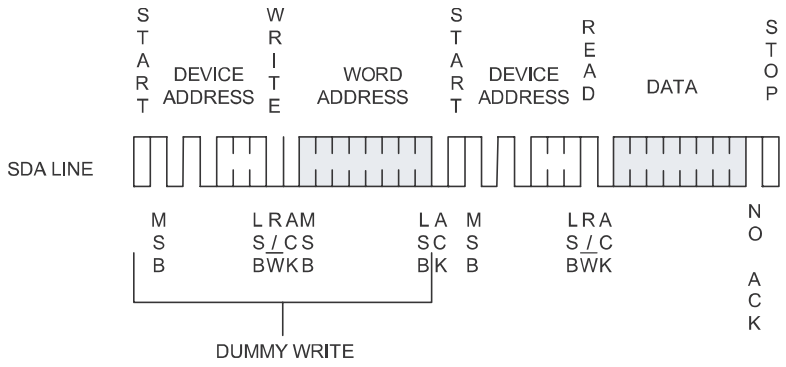


Figure 8. Random Read

Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

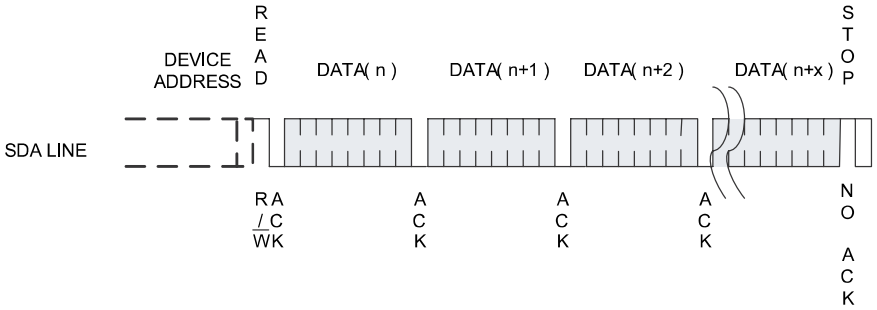


Figure 9. Sequential Read

BUS TIMING

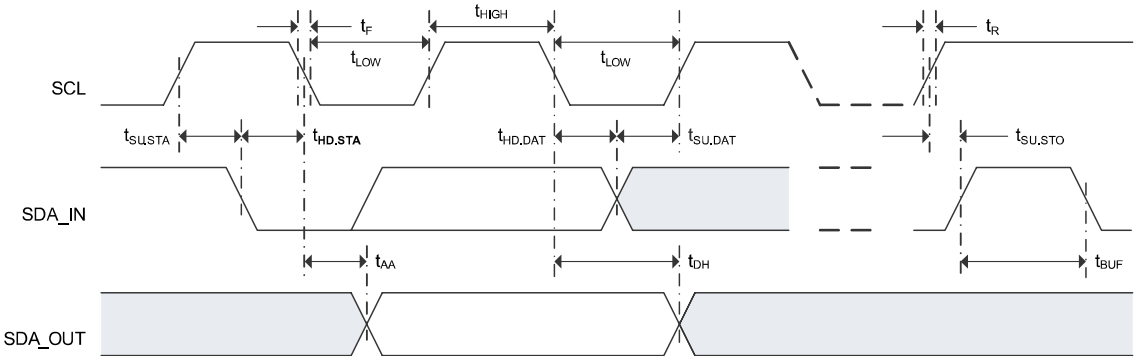
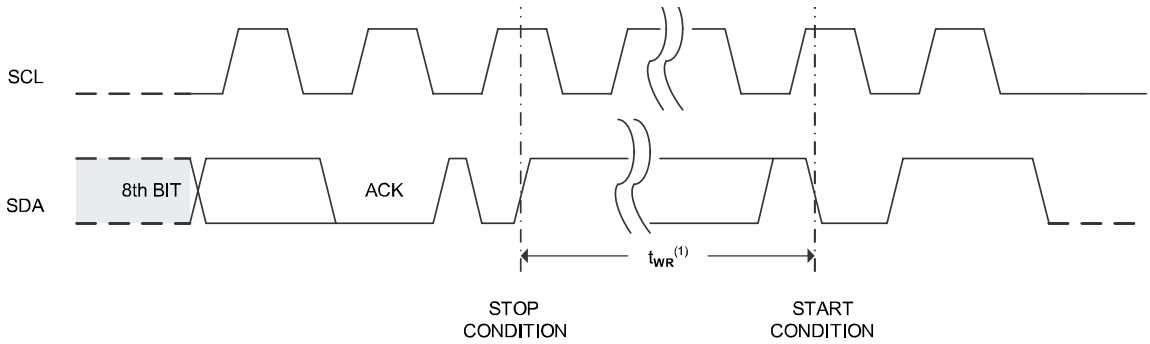


Figure 10. SCL: Serial Clock, SDA: Serial Data

WRITE CYCLE TIMING

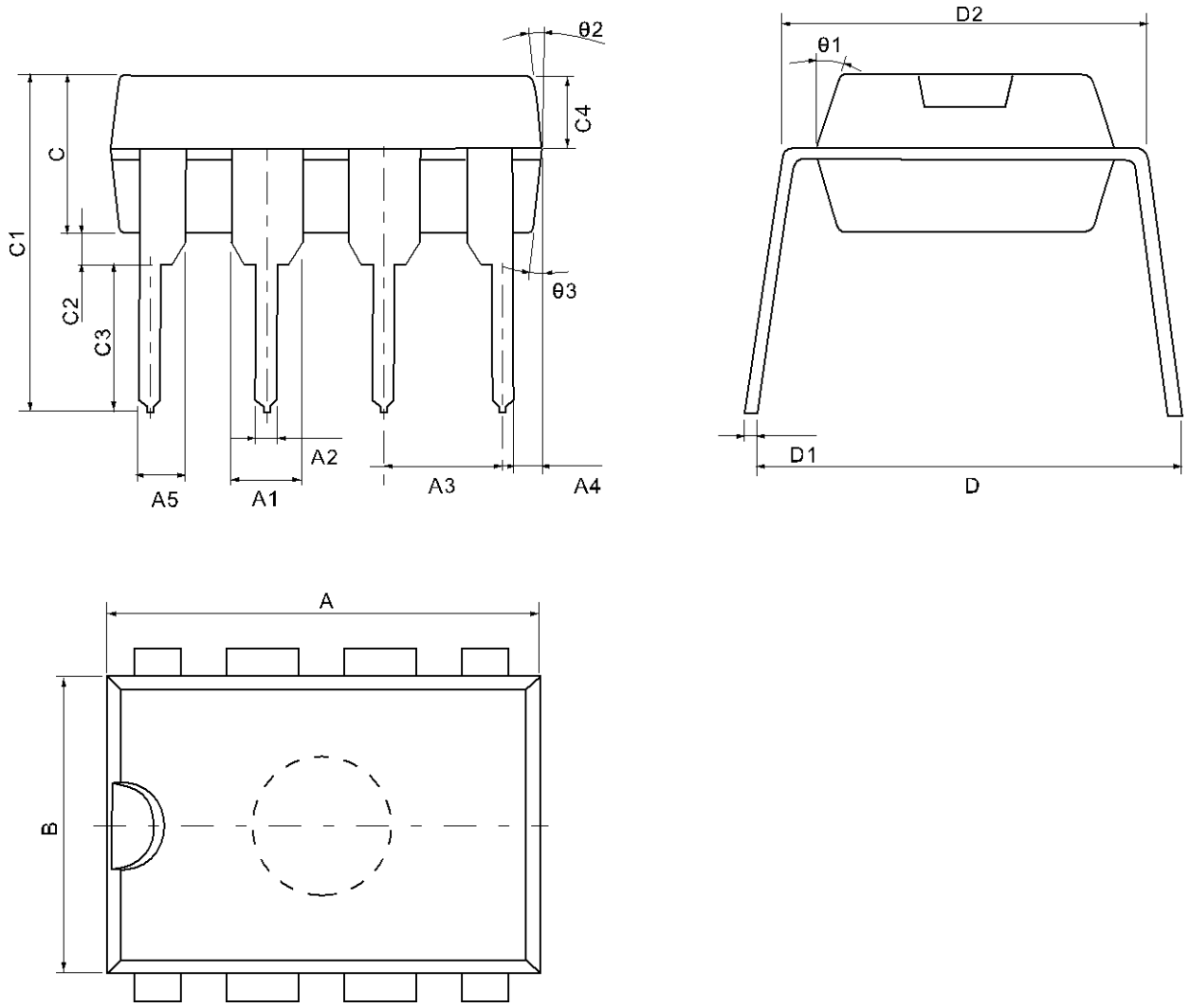


Notes: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

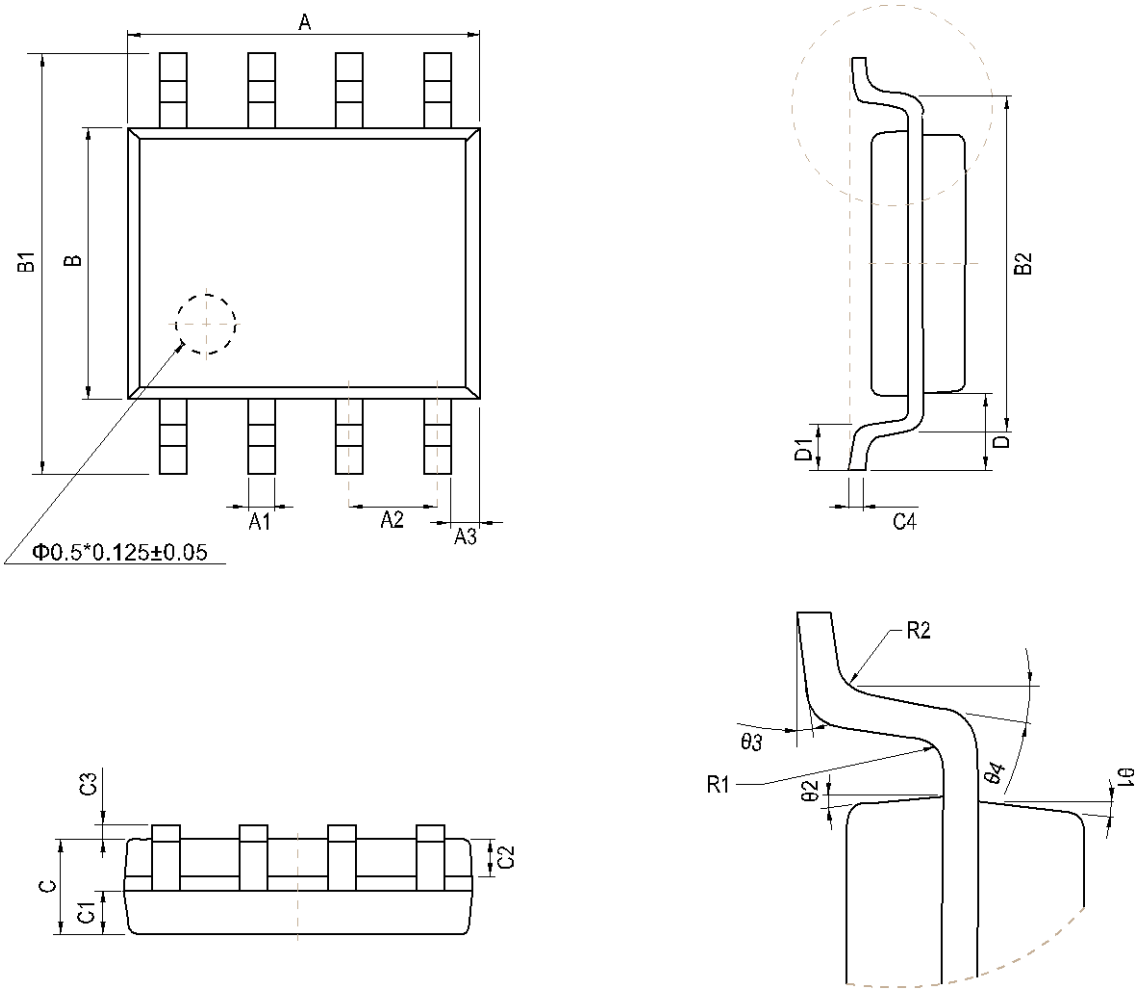
PHYSICAL DIMENSIONS

DIP8



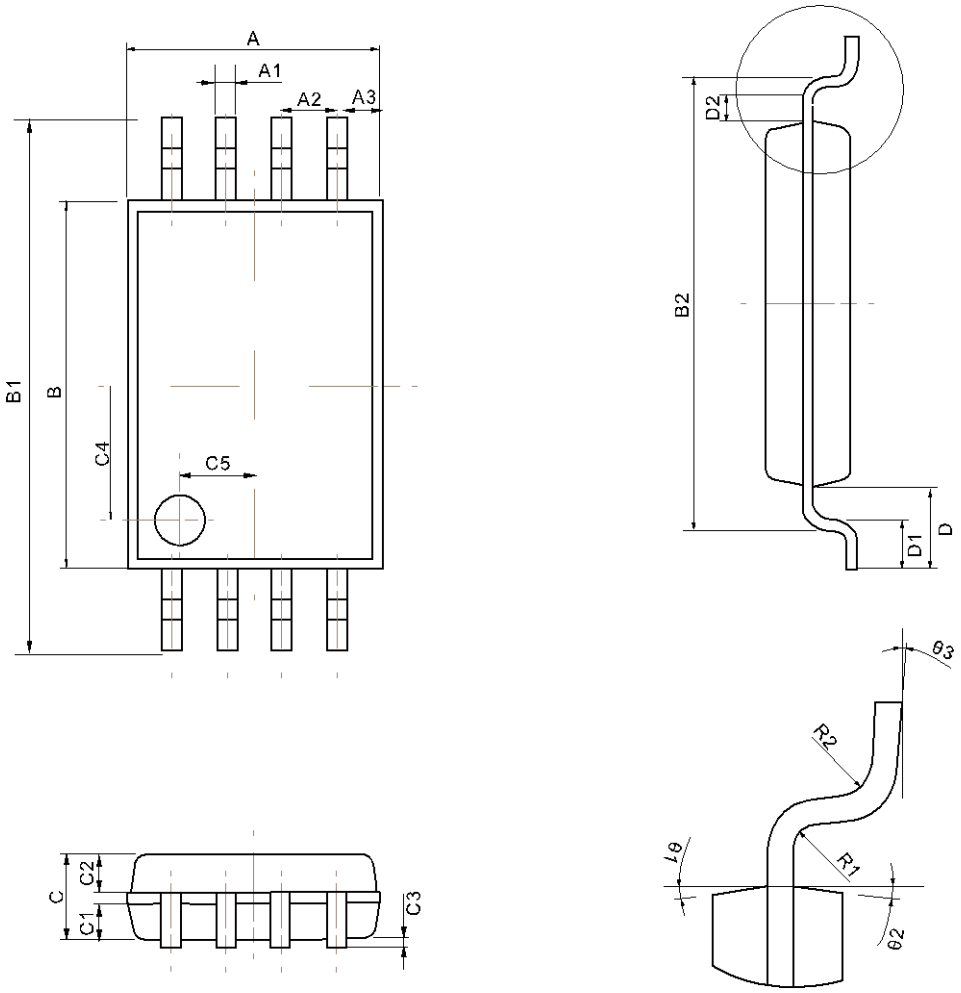
Symbol	Dimension（mm）		Symbol	Dimension（mm）	
	Min	Max		Min	Max
A	9.00	9.20	C2	0.50（TYP）	
A1	1.474	1.574	C3	3.20	3.40
A2	0.41	0.51	C4	1.47	1.57
A3	2.44	2.64	D	8.20	8.80
A4	0.51（TYP）		D1	0.244	0.264
A5	0.99（TYP）		D2	7.62	7.87
B	6.10	6.30	θ1	17°（TYP）	
C	3.20	3.40	θ2	10°（TYP）	
C1	7.10	7.30	θ3	8°（TYP）	

SOP8



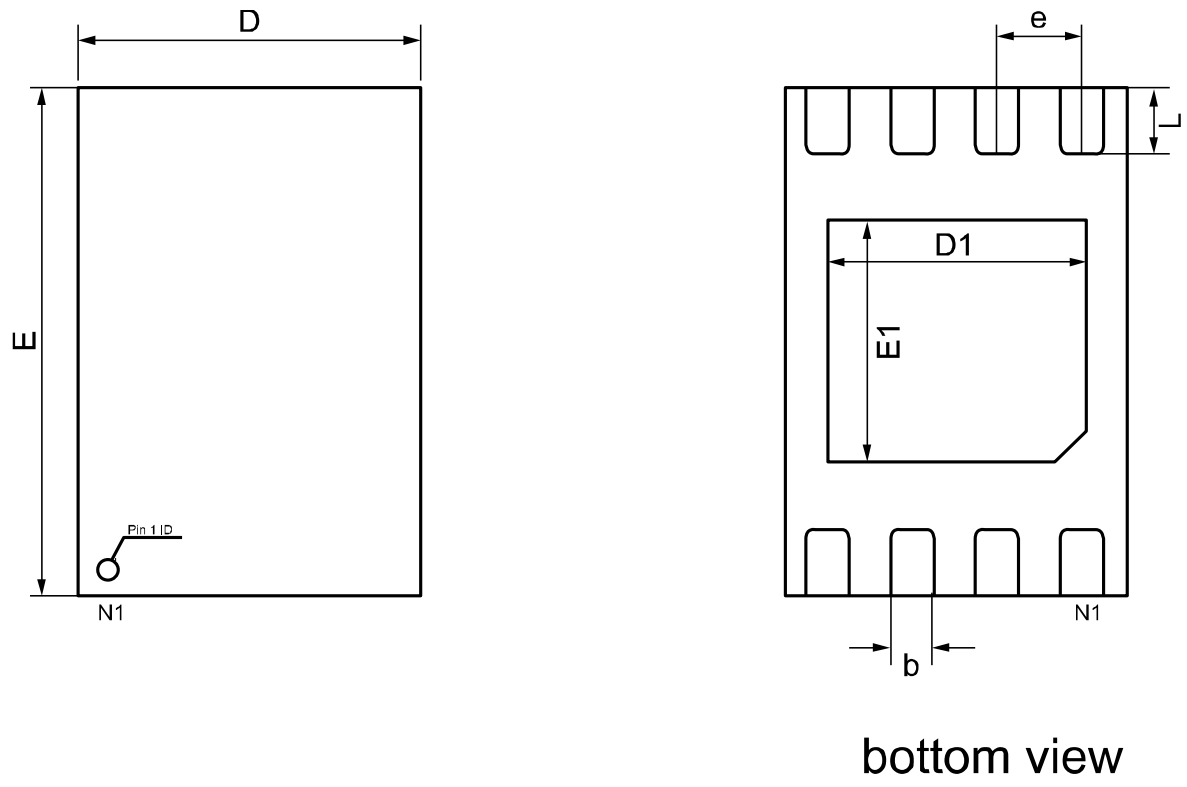
Symbol	Dimension（mm）		Symbol	Dimension（mm）	
	Min	Max		Min	Max
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27（TYP）		D	1.05（TYP）	
A3	0.345（TYP）		D1	0.40	0.80
B	3.80	4.00	R1	0.20（TYP）	
B1	5.80	6.20	R2	0.20（TYP）	
B2	5.00（TYP）		θ1	17°（TYP）	
C	1.30	1.60	θ2	13°（TYP）	
C1	0.55	0.65	θ3	0° ~ 8°（TYP）	
C2	0.55	0.65	θ4	4° ~ 12°（TYP）	

TSSOP8



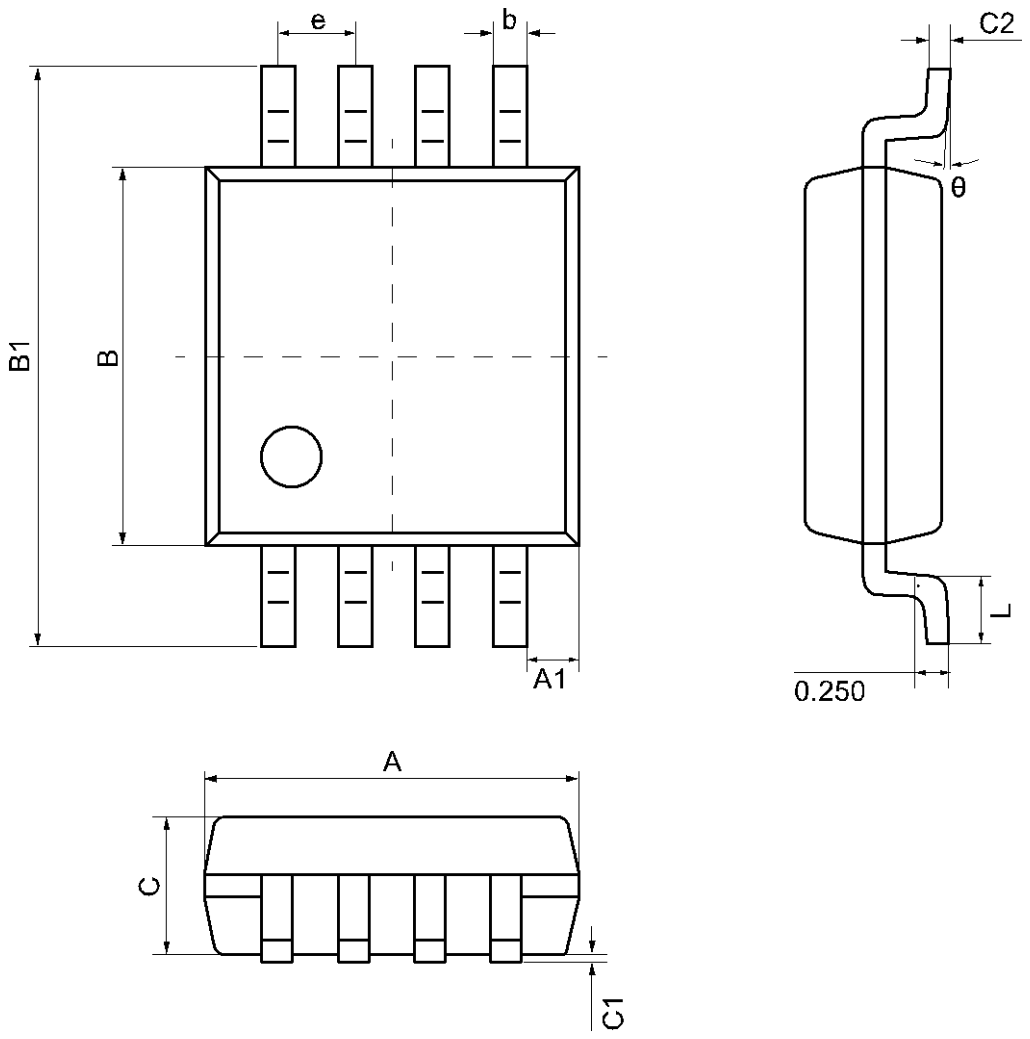
Symbol	Dimension（mm）		Symbol	Dimension（mm）	
	Min	Max		Min	Max
A	2.90	3.10	C4	1.55	1.65
A1	0.20	0.30	C5	0.85	0.95
A2	0.60	0.70	D	1.00（TYP）	
A3	0.41	0.42	D1	0.50	0.70
B	4.30	4.50	D2	0.19	0.29
B1	6.30	6.50	R1	0.15（TYP）	
B2	5.404	5.504	R2	0.15（TYP）	
C	0.95	1.05	θ1	12°（TYP）	
C1	0.415	0.465	θ2	12°（TYP）	
C2	0.39	0.49	θ3	0° ~ 7°	
C3	0.05	0.15	-	-	

UDFN8



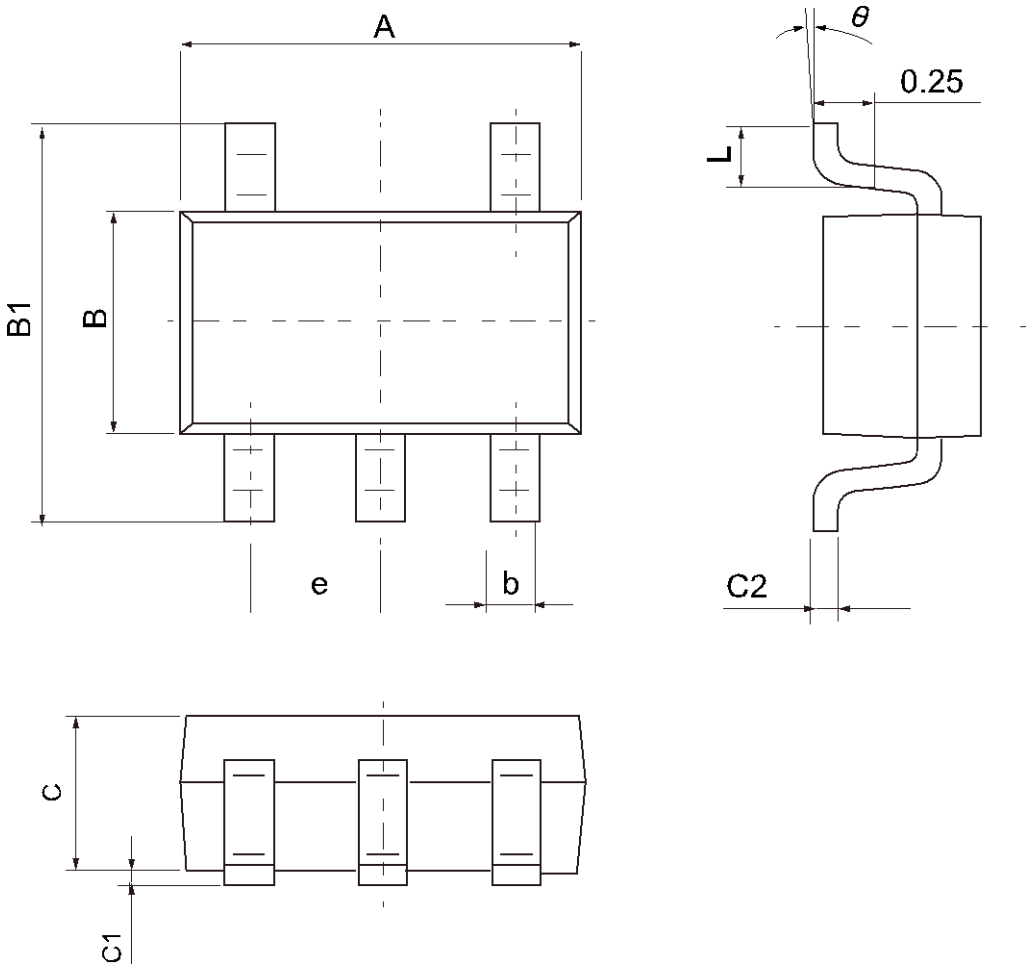
Symbol	Dimension（mm）			Symbol	Dimension（mm）		
	Min	Typ.	Max		Min	Typ.	Max
A	0.50	0.55	0.60	e	0.50TYP		
A1	0.00	0.03	0.05	E	2.95	3.00	3.05
b	0.20	0.25	0.30	E1	1.30	1.40	1.50
c	0.152REF			D1	1.40	1.50	1.60
D	1.95	2.00	2.05	L	0.35	0.40	0.45

CPC8



Symbol	Dimension（mm）		Symbol	Dimension（mm）	
	Min	Max		Min	Max
A	2.50	2.70	C	0.85	1.05
A1	0.35	0.45	C1	0.00	0.15
e	0.53（BSC）		C2	0.15	0.18
B	2.50	2.70	L	0.40	0.60
B1	3.85	4.15	θ	0°	8°
b	0.16	0.26	-	-	-

SOT23-5



Symbol	Dimension（mm）		Symbol	Dimension（mm）	
	Min	Max		Min	Max
A	2.82	3.02	C	1.05	1.15
e	0.95（BSC）		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.75	3.05	θ	0°	8°