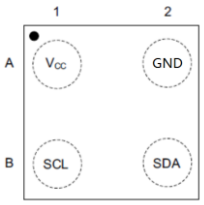
64K bit Serial I²C bus EEPROM 4 ball CSP

DESCRIPTION

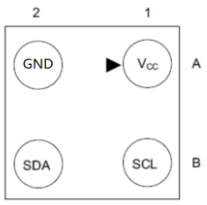
The CW24C64B provides 65536 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 8192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The CW24C64B is accessed via a two-wire serial interface and is available in 1.7V (1.7V to 5.5V) version.

PIN CONFIGURATION

WLCSP



(Top View)



(Bottom View)

FEATURES

- Wide Voltage Operation V_{CC} = 1.7V to 5.5V
- Operating Ambient Temperature: -40°C to +85°C
- Internally Organized: 8192 × 8 (64K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- Page Write, 32-byte Page
- Partial Page Writes Allowed
- Software Write protect whole memory array
- Configurable device address
- Self-timed Write Cycle (4 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Package: WLCSP-4

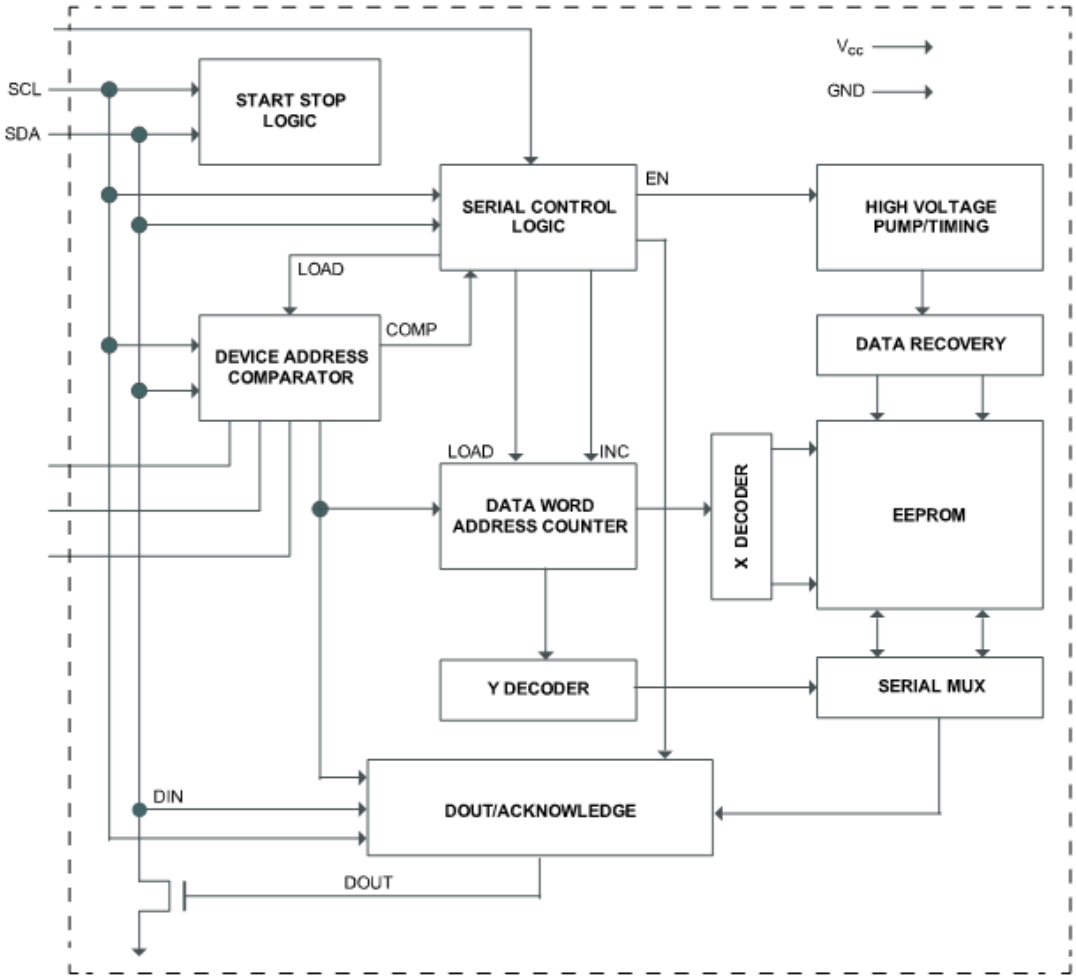
APPLICATIONS

- Intelligent Instrument
- Camera
- Automotive Electronics
- Wearable Devices

ORDERING INFORMATION

Temperature Range	Package		Orderable Device	Package Qty.
-40°C ~ +85°C	Pb-Free	WLCSP	CW24C64BW4R	3000 片/卷

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Maximum Ratings are those values beyond which damage to the device may occur.)

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.3 to + 6.5	V
DC Input Voltage	V_{IN}	GND - 0.3 to V_{CC} + 0.3	V
DC Output Voltage	V_{OUT}	GND - 0.3 to V_{CC} + 0.3	V
Operating Ambient Temperature	T_a	-55 ~ +125	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS

(Functional operation should be restricted to the Recommended Operating Conditions.)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	1.7	5.5	V
Operating Temperature	T_A	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Voltage	V_{CC1}	-		1.7	-	5.5	V
	V_{CC2}	-		2.5	-	5.5	
	V_{CC3}	-		2.7	-	5.5	
	V_{CC4}	-		4.5	-	5.5	
Supply Current	I_{CC}	V_{CC} = 5V	Read at 1MHz	-	0.02	0.1	mA
			Write at 1MHz	-	0.9	2.0	mA
Standby Current	I_{SB}	V_{IN} = V_{CC} or GND, V_{CC}=1.7V		-	0.6	1.0	μA
		V_{IN} = V_{CC} or GND, V_{CC}=2.5V			1.0	2.0	μA
		V_{IN} = V_{CC} or GND, V_{CC}=5.5V		-	1.2	2.0	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND		-	0.10	2.0	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or GND		-	0.05	2.0	μA
Input Low Level	V_{IL}	V_{CC} = 1.8V to 5.5V		-0.3	-	V_{CC}x0.3	V
		V_{CC} = 1.7V		-0.3	-	V_{CC}x0.2	
Input High Level	V_{IH}	V_{CC} = 1.7V to 5.5V		V_{CC}x0.7	-	V_{CC}+0.3	V
Output Low Level	V_{OL3}	V_{CC} = 5.0V, I_{OL} = 3.0 mA		-	-	0.4	V
	V_{OL2}	V_{CC} = 3.0V, I_{OL} = 2.1 mA		-	-	0.4	V
	V_{OL1}	V_{CC} = 1.7V, I_{OL} = 0.15 mA		-	-	0.2	V

AC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, C_L = 1 TTL Gate and 100 pF unless otherwise noted)

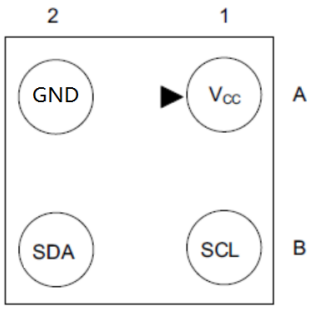
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Frequency, SCL	f_{SCL}	1.7V<V_{CC}<2.5V	-	-	400	kHz
		2.5V<V_{CC}<5.5V	-	-	1000	
Clock Pulse Width Low	t_{LOW}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.6	-	-	
Clock Pulse Width High	t_{HIGH}	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.4	-	-	
Noise Suppression Time	t_I	1.7V<V_{CC}<2.5V	-	-	50	ns
		2.5V<V_{CC}<5.5V	-	-	50	
Clock Low to Data Out Valid	t_{AA}	1.7V<V_{CC}<2.5V	0.1	-	0.9	μs
		2.5V<V_{CC}<5.5V	0.05	-	0.9	
Time the bus must be free before a new transmission can start	t_{BUF}	1.7V<V_{CC}<2.5V	1.2	-	-	μs
		2.5V<V_{CC}<5.5V	0.5	-	-	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Start Hold Time	$t_{HD.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	1.7V<V_{CC}<2.5V	0.6	-	-	μs
		2.5V<V_{CC}<5.5V	0.25			
Data In Hold Time	$t_{HD.DAT}$	1.7V<V_{CC}<5.5V	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	1.7V<V_{CC}<5.5V	100	-	-	ns
Inputs Rise Time	t_R	-	-	-	300	ns
Inputs Fall Time	t_F	-	-	-	300	Ns
Stop Setup Time	$t_{SU.STO}$	1.7V<V_{CC}<2.5V	0.6	-	-	Ms
		2.5V<V_{CC}<5.5V	0.25	-	-	
Data Out Hold Time	t_{DH}	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	-	3.3	4	ms
5.0V,25°C,Byte Mode	Endurance	-	1M	-	-	Write Cycles

Note:

1. This parameter is characterized and is not 100% tested.
2. AC measurement condition:
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC};
   Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 V_{CC}
   The value of R_L should be concerned according to the actual loading on the user's system.
   R_L (connects to V_{CC}): 1.3KΩ （2.5V,5V）, 10KΩ （1.7V）

PIN DESCRIPTION



(Bottom View)

No.	Name	Function Description
A1	VCC	Positive supply voltage.
A2	SCL	Serial clock input. The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.
B1	SDA	Serial address and data I/O. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.
B2	GND	Circuit ground pin.

MEMORY ORGANIZATION

Device	Total bits	Total pages	Bytes per page	Word address
CW24C64BW4R	64K	256	32	13-bit

DEVICE OPERATION

Clock and data transitions

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined below.

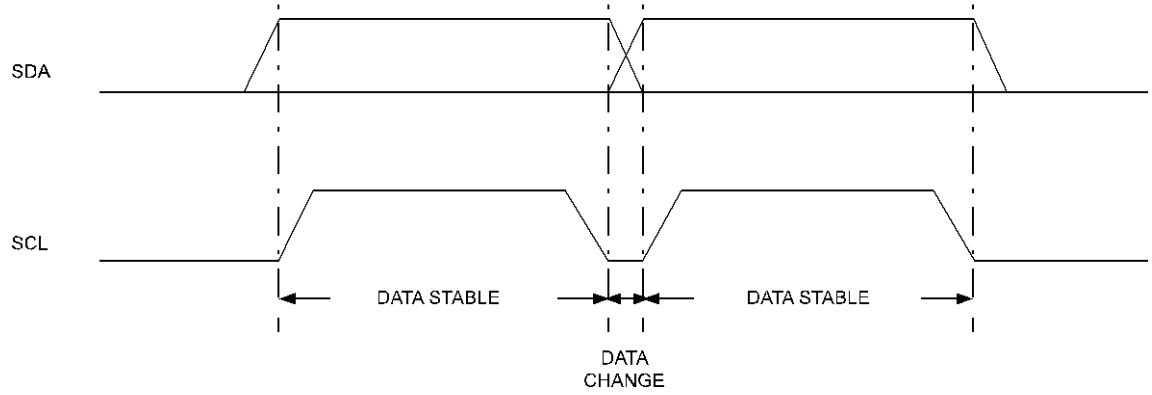


Figure 1. Data Validity

Start Conditions

A high-to-low transition of SDA with SCL high is a start condition which must precede any other Command. (see Figure 2)

Stop Conditions

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode. (see Figure 2)

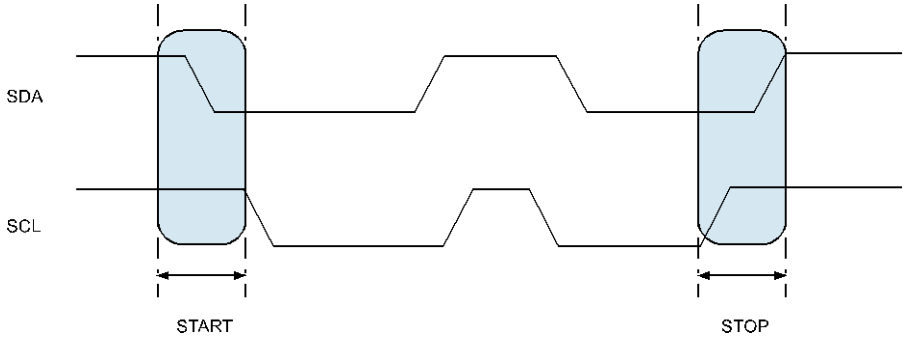


Figure 2. Start and Stop Definition

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

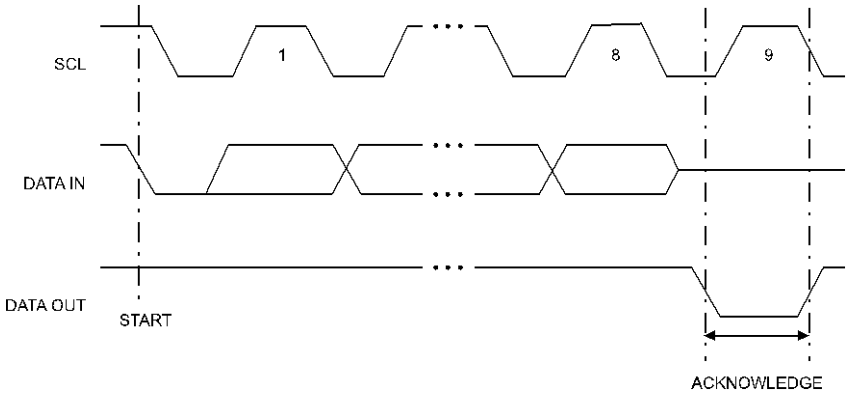


Figure 3. Output Acknowledge

Standby Mode

The EEPROM features a low-power standby mode which is enabled:
(1) upon power-up and (2) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:
(1) Clock up to 9 cycles.
(2) Look for SDA high in each cycle while SCL is high.
(3) Create a start condition.

CSP configurations

Configurable Device Address (CDA)

Since there are no A0, A1, A2 pins, the CW24C64B WLCSP package provides the address configuration for user to implement CDA features. When power-on, the device will load address configuration automatically.

The CDA contains C0/C1/C2 three NVM bits, and corresponding to A0/A1/A2 pins respectively. The CDA factory default is “000”.

Software Write Protection (SWP)

Since there are no WP pin, the CW24C64B WLCSP package provides write protection by SWP. The SWP is one NVM bit, when power-on, the device will load SWP configuration automatically. The SWP factory default is “0” means protect disable.

Access CDA and SWP

Access to the CDA and SWP is obtained by beginning the device address word with a ‘1011b’ sequence, the next three bits of device address (C2, C1 and C0) must be the same as previously configured CDA value. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Table – device address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	C2	C1	C0	R/W
CSP Configurations	1	0	1	1	C2	C1	C0	R/W

Table-first word address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	x	x	x	A12	A11	A10	A9	A8
CSP Configurations	x	x	x	x	x	1	1	x

The first word address bit2 and bit1 must be '11b' to recognize it is a CDA/SWP access, the second word address is don't care but must exist. The first byte data contains CDA and SWP value, and only one byte should be accessed. These NVM bits' location is shown at below table

Table – CDA and SWP bits location

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C2	C1	C0	x	x	x	SWP	x

Write CDA/SWP operation do not support Ack polling to check whether the internal write cycle has completed. The next instruction issuing must wait for the end of the internal write cycle(max 5ms), otherwise the instruction is invalid.

Reading CDA/SWP sequence is similar with normal random read, which needs a dummy write with two words address, then uses a device address command with direction "read" to read the CDA and SWP value.

WRITE OPERATIONS

Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).

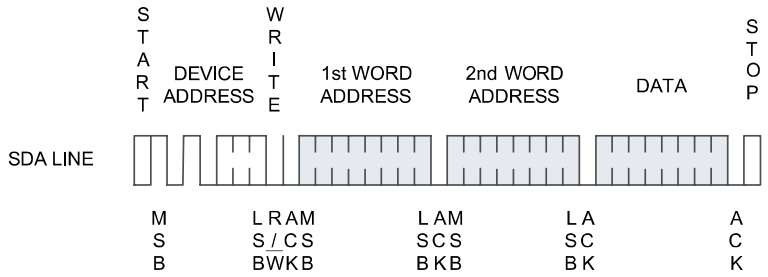


Figure 5. Byte Write

Page Write

The CW24C64B devices is capable of 32-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

The data word address lower 5 (CW24C64B) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

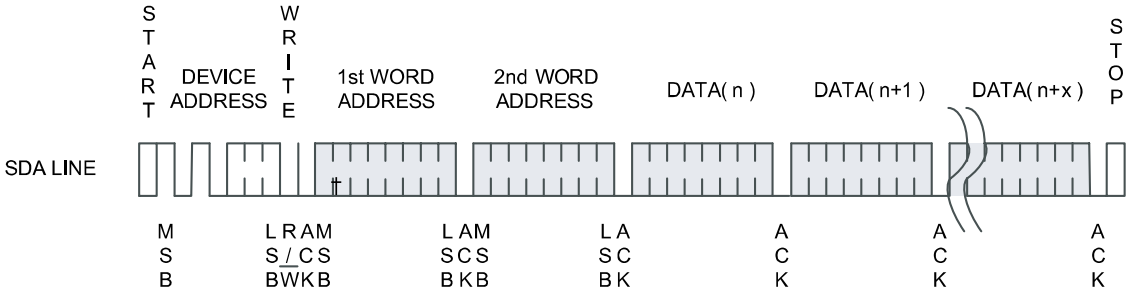


Figure 6. Page Write

Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

READ OPERATIONS

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

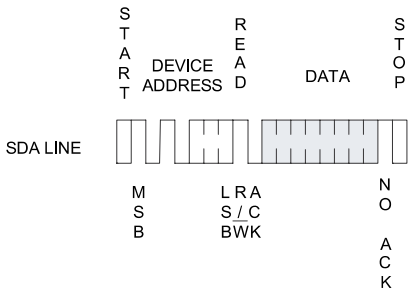


Figure 7. Current Address Read

Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8).

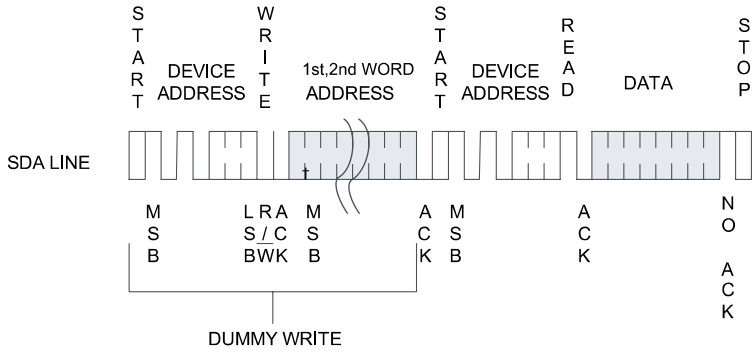


Figure 8. Random Read

Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

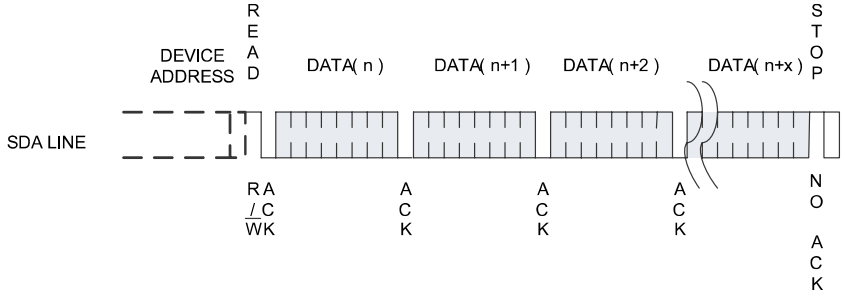


Figure 9. Sequential Read

BUS TIMING

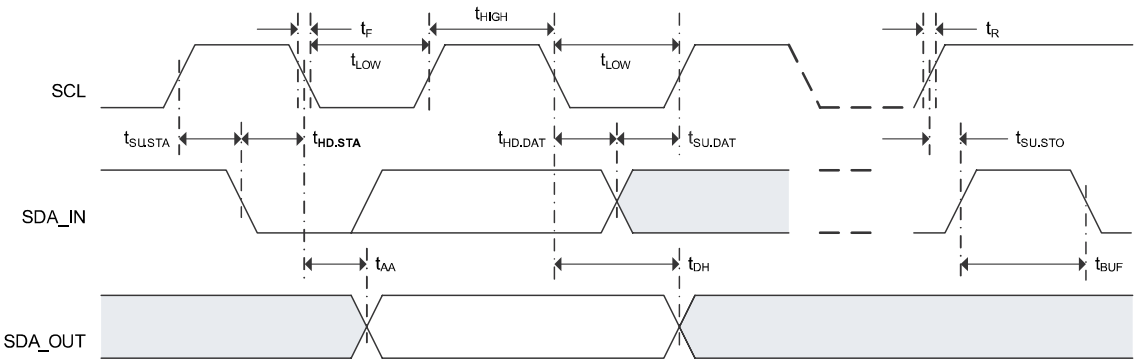
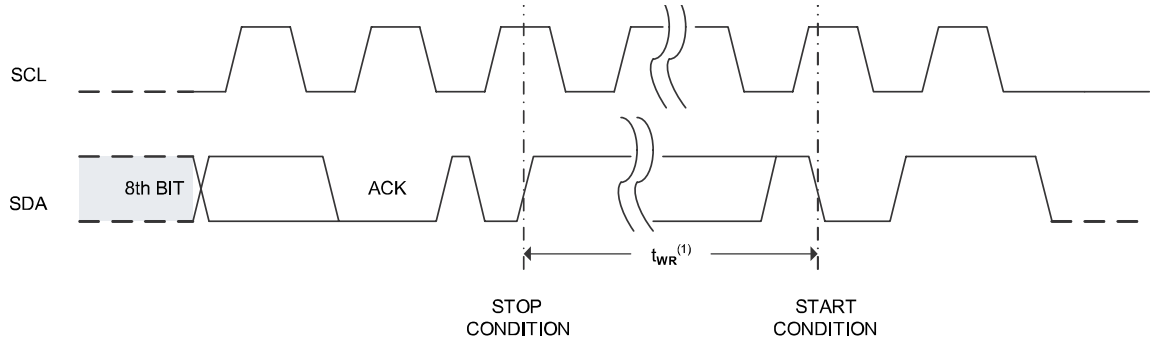


Figure 10. SCL: Serial Clock, SDA: Serial Data

WRITE CYCLE TIMING

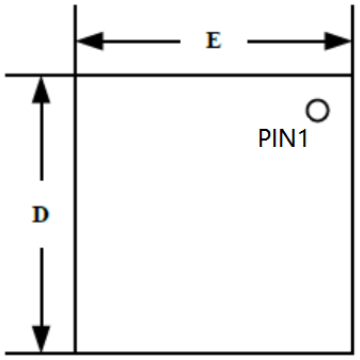


Notes: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

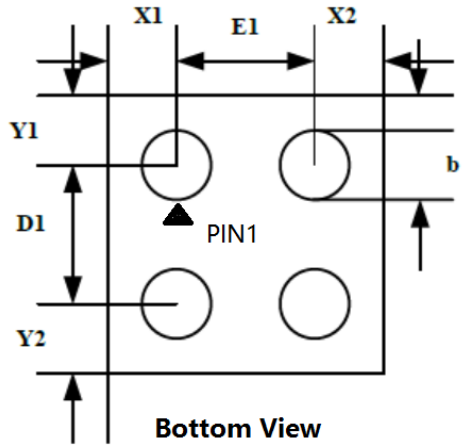
Figure 11. SCL: Serial Clock, SDA: Serial Data I/O

PHYSICAL DIMENSIONS

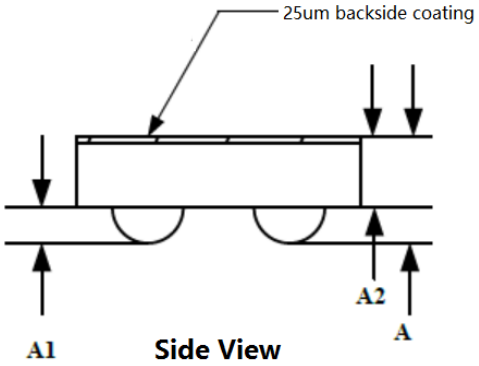
WLCSP-4



Top View



Bottom View



Side View

Symbol	Dimension（mm）			Symbol	Dimension（mm）		
	Min	Typ.	Max		Min	Typ.	Max
A	0.245	0.270	0.295	E1	0.400BSC		
A1	0.045	0.055	0.065	b	0.140	0.160	0.180
A2	0.195	0.215	0.235	X1	0.1395REF		
D	0.640	0.665	0.690	X2	0.1395REF		
D1	0.400BSC			Y1	0.1325REF		
E	0.654	0.679	0.704	Y2	0.1325REF		

Application Notes

1. The device cannot be reset by 2-wire bus during internally timed write cycle, if the device does not give correct acknowledge after 4ms write cycle, and if the device pulls down the SDA and never release it, must use power up to reset the device.
2. Once CDA re-configured, the following command with device address bits must be in accordance with the modified CDA, otherwise the device will not response and return to standby state.
3. If SWP is enabled, CDA is protected by SWP. CDA can't be modified even during the SWP disable operation, the value of CDA in DATA0 of config CDA/SWP command sequence is ignored.
4. When SWP is enable, writing data will get NoAck from device.