Programmable On-Chip Oscillator Compensation

by Peter Chan, July 2000

What is an On-Chip Oscillator Compensation?

An on-chip oscillator compensation is an additional feature on Xicor's real time clocks. It allows the real time clock to be connected with crystals that have different load capacitance (CL) requirements. This new enhancement widens the choices of a crystal working with Xicor's real time clocks and it also simplifies the setup and layout of the device within your system. This single chip solution saves PCB board space because no RC circuitry is needed and reduces the total cost of the system for customers.

In general, when you connect a crystal to the real time clock, you need to make sure the load capacitance requirement matches with the crystal manufacturers' specifications in order for the proper oscillating frequency.

The new X1226/27/28 real time clocks offer programmable on-chip oscillator compensation using software routine to program the load capacitance adjustment for clock accuracy and stability.

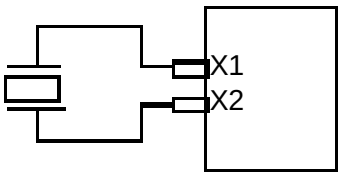

Figure 1: Recommended Crystal Connection

Digital Trimming Register (DTR) - DTR2, DTR1 and DTR0 (Nonvolatile)

The digital trimming bits DTR2, DTR1 and DTR0 adjust the number of count per second and average the ppm error to achieve a high accuracy over a long period of time. DTR2 is a sign bit when equal to 1 means positive ppm and 0 means negative ppm compensation. A range from -30ppm to +30ppm can be represented by using the three bits. The DTR register is located in the clock control register with an address at 13h.

Table 1: Digital Trimming Register (DTR

DTR2D	DTR1	TR0	PPM
0	0	0	-0
0	1	0	-10
0	0	1	-20
0	1	1	-30
1	0	0	+0
1	1	0	+20
1	1	1	+30

Analog Trimming Register (ATR) - ATR5, ATR4…and ATR0 (Nonvolatile)

Six analog trimming Bits from ATR5 to ATR0 are provided to adjust the on-chip loading capacitance range from 10pF to 39.5pF for X1 and X2 pins. The effective load capacitance range from 5pF to 19.75pF. Each bit has different weight for capacitance adjustment. This will allow 6pF or 12.5pF crystal being used and widen the selection. In addition, refer to Table 2, using a Seiko VT-200 crystal with the different ATR bits combinations, it provides an estimated PPM range from +116ppm to -37ppm to the nominal frequency compensation. The combination of digital and analog trimming can give up to +146ppm adjustment. The ATR register is located in the clock control register with an address at 12H.

Writing to the DTR and ATR register

In order to perform any write operation, the following steps are required:

1. Perform a Write Enable Operation to set the "Write Enable Latch" (WEL) in the status register.

2. Perform a Write Enable Operation to set both the "Register Write Enable Latch" (RWEL) and the "Write Enable Latch" (WEL) in the status register.
3. Write one to eight bytes of data to the Clock Control Registers or to the memory array with the desired values.

Addr	7	6	5	4	3	2	1	0
8FH	BAT	AL1	AL0	0	0	RWEL	WEL	RTCF

Figure 2: Status Register (SR)

SUMMARY

Overall, it has been shown that the X1226/27/28 real time clock with the programmable on-chip oscillator compensation really simplifies the setup and layout of the device within the system. This single chip solution saves PCB board space because no RC circuitry is needed and reduces the total cost of the system for customers. The integration of the on-chip oscillator compensation improves accuracy and stability of the real time clock during the lifetime of the product over a wide range of temperature.

Table 2: Analog Trimming Register (ATR)

Analog Trimming Register Bits Setting															
5	4	3	2	1	0	Load Capacitance[1]	Estimated PPM[2]	5	4	3	2	1	0	Load Capacitance2	Estimated PPM1
1	0	0	0	0	0	5.00pF	116	0	0	0	0	0	0	12.50pF	0
1	0	0	0	0	1	5.25pF	110	0	0	0	0	0	1	12.75pF	-2
1	0	0	0	1	0	5.50pF	104	0	0	0	0	1	0	13.00pF	-4
1	0	0	0	1	1	5.75pF	98	0	0	0	0	1	1	13.25pF	-6
1	0	0	1	0	0	6.00pF	93	0	0	0	1	0	0	13.50pF	-7
1	0	0	1	0	1	6.25pF	87	0	0	0	1	0	1	13.75pF	-9
1	0	0	1	1	0	6.50pF	82	0	0	0	1	1	0	14.00pF	-11
1	0	0	1	1	1	6.75pF	77	0	0	0	1	1	1	14.25pF	-12
1	0	1	0	0	0	7.00pF	72	0	0	1	0	0	0	14.50pF	-14
1	0	1	0	0	1	7.25pF	67	0	0	1	0	0	1	14.75pF	-15
1	0	1	0	1	0	7.50pF	63	0	0	1	0	1	0	15.00pF	-17
1	0	1	0	1	1	7.75pF	58	0	0	1	0	1	1	15.25pF	-18
1	0	1	1	0	0	8.00pF	54	0	0	1	1	0	0	15.50pF	-19
1	0	1	1	0	1	8.25pF	50	0	0	1	1	0	1	15.75pF	-21
1	1	0	0	0	0	8.50pF	46	0	1	0	0	0	0	16.00pF	-22
1	1	0	0	0	1	8.75pF	42	0	1	0	0	0	1	16.25pF	-23
1	1	0	0	1	0	9.25pF	39	0	1	0	0	1	0	16.50pF	-25
1	1	0	0	1	1	9.50pF	35	0	1	0	0	1	1	16.75pF	-26
1	1	0	1	0	0	9.75pF	32	0	1	0	1	0	0	17.00pF	-27
1	1	0	1	0	1	10.00pF	29	0	1	0	1	0	1	17.25pF	-28
1	1	0	1	1	0	10.25pF	25	0	1	0	1	1	0	17.50pF	-29
1	1	0	1	1	1	10.25pF	22	0	1	0	1	1	1	17.75pF	-30
1	1	1	0	0	0	10.50pF	19	0	1	1	0	0	0	18.00pF	-31
1	1	1	0	0	1	10.75pF	17	0	1	1	0	0	1	18.25pF	-32
1	1	1	0	1	0	11.00pF	14	0	1	1	0	1	0	18.50pF	-33
1	1	1	0	1	1	11.25pF	11	0	1	1	0	1	1	18.75pF	-34

Table 2: Analog Trimming Register (ATR)

Analog Trimming Register Bits Setting															
5	**4**	**3**	**2**	**1**	**0**	**Load Capacitance[1]**	**Estimated PPM[2]**	**5**	**4**	**3**	**2**	**1**	**0**	**Load Capacitance2**	**Estimated PPM1**
1	1	1	1	0	0	11.50pF	9	0	1	1	1	0	0	19.00pF	-35
1	1	1	1	0	1	11.75pF	6	0	1	1	1	0	1	19.25pF	-36
1	1	1	1	1	0	12.00pF	4	0	1	1	1	1	0	19.50pF	-36
1	1	1	1	1	1	12.25pF	2	0	1	1	1	1	1	19.75pF	-37

1. For reference only. Values are based on characterization only.
2. For Seiko VT-200 crystal