AND8097/D

New MiniGate Device Performs Up and Down Translation

Prepared by: Fred Zlotnick
ON Semiconductor
Applications Manager

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APPLICATION NOTE

Often a designer encounters a problem requiring voltage translation. The designer will need one translator to go from a lower to higher voltage and a second one to go from a lower voltage to a higher voltage. This note will outline one possible way of accomplishing this goal.

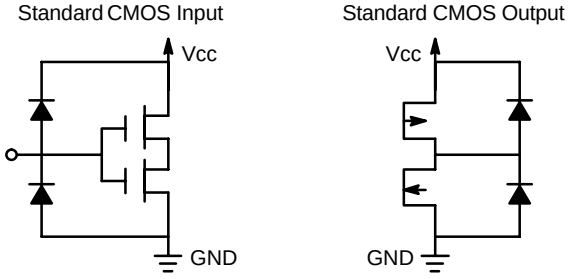

Figure 1.

Why Do We Need to Translate?

Most standard CMOS devices have a circuit similar to Figure 1 for its Input and Output. Most ASICs, Microprocessors, and FPGAs are like Figure 1 and require that the voltage applied not exceed Vcc.

Example: A design requires two total translators, one from 2.2 V to 3.3 V and one from 3.3 V to 2.2 V. Space is critical and the data rate is 10 MHz, with a 7 pF load, the output should not be inverted with respect to the input.

Solution: The NL27WZ07DFT2 is a dual noninverting buffer with open drains. Unlike the sketches in Figure 1, the device has no diodes connected to Vcc in either the input or output. The I/Os are therefore OVT (Overvoltage Tolerant). This allows us to operate the device at the lower of the two voltages, with no harm, and let the output go to a separate voltage that we pull up to. The output is OVT as well and this allows us to pull up to a higher voltage. Since the data rate is 10 MHz, I have arbitrarily set the maximum delay to 25 ns. The device operating at 2.2 V will introduce about 7 ns, the leaves us 18 ns. Assuming 2.0 time constants, this means τ can be 9.0 ns. If the load C is 7.0 pF, then R can be 1.2 k. This will draw 1.6 mA max, and 0.8 mA per circuit with a 50% duty cycle. If the current draw is too high or the delay is too high, then we will need another solution. The same function is available as a single (NL17SZ07DFT2) and triple (NL37WZ07US).

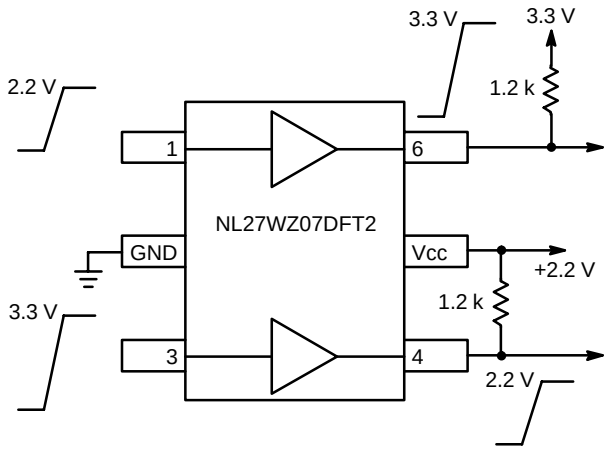

Figure 2. Dual Bi–Level Translators

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