NL17SZ125

Non-Inverting 3-State Buffer

The NL17SZ125 is a high performance non−inverting buffer operating from a 1.65 V to 5.5 V supply.

- Extremely High Speed: t_{PD} 2.6 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Overvoltage Tolerant Inputs and Outputs
- LVTTL Compatible − Interface Capability With 5.0 V TTL Logic with V_{CC} = 3.0 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- 3−State OE Input is Active−Low
- Replacement for NC7SZ125
- Chip Complexity = 36 FETs
- Pb−Free Package is Available

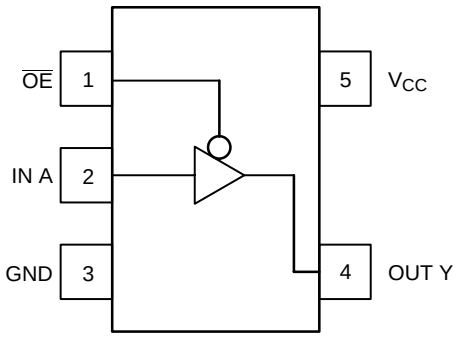


Figure 1. Pinout (Top View)

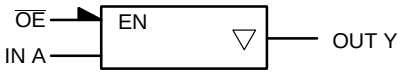


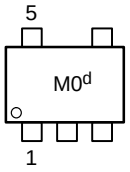
Figure 2. Logic Symbol

ON Semiconductor®

http://onsemi.com

SC−88A (SOT−353)
DF SUFFIX
CASE 419A

MARKING DIAGRAM



d = Date Code

PIN ASSIGNMENT	
1	$\overline{OE}$
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

$\overline{OE}$ Input	A Input	Y Output
L	L	L
L	H	H
H	X	Z

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current		−50	mA
I_{OK}	DC Output Diode Current		−50	mA
I_{OUT}	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)		350	°C/W
P_D	Power Dissipation in Still Air at 85°C		150	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.65	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	5.5	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 1.8 V ±0.15 V V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0 0 0	20 20 10 5.0	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

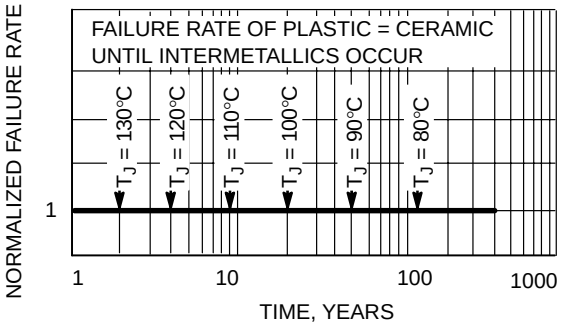


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit	Condition
			Min	Typ	Max	Min	Max		
V_{IH}	High−Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V	
V_{IL}	Low−Level Input Voltage	1.65 to 1.95 2.3 to 5.5			0.25 V_{CC} 0.3 V_{CC}		0.25 V_{CC} 0.3 V_{CC}	V	
V_{OH}	High−Level Output Voltage V_{IN} = V_{IH}	1.65 1.8 2.3 3.0 4.5	1.55 1.7 2.2 2.9 4.4	1.65 1.8 2.3 3.0 4.5		1.55 1.7 2.2 2.9 4.4		V	I_{OH} = −100 μA
		1.65 2.3 3.0 3.0 4.5	1.29 1.9 2.4 2.3 3.8	1.52 2.15 2.80 2.68 4.20		1.29 1.9 2.4 2.3 3.8		V	I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IL}	1.65 1.8 2.3 3.0 4.5		0.0 0.0 0.0 0.0 0.0	0.1 0.1 0.1 0.1 0.1		0.1 0.1 0.1 0.1 0.1	V	I_{OL} = 100 μA
		1.65 2.3 3.0 3.0 4.5		0.08 0.10 0.15 0.22 0.22	0.24 0.30 0.40 0.55 0.55		0.24 0.30 0.40 0.55 0.55	V	I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±1.0		±1.0	μA	0 V ≤ V_{IN} ≤ 5.5 V
I_{OZ}	3−State Output Leakage	1.65 to 5.5			±0.5		±5.0	μA	V_{IN} = V_{IH} or V_{IL} 0 V ≤ V_{OUT} ≤ 5.5 V
I_{OFF}	Power Off Leakage Current	0.0			1.0		10	μA	V_{IN} or V_{OUT} = 5.5 V
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μA	V_{IN} = 5.5 V, GND

AC ELECTRICAL CHARACTERISTICS ($t_R = t_F$ = 3.0 ns)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay AN to YN (Figures 4 and 5, Table 1)	R_L = 1 MΩ C_L = 15 pF	1.8 ± 0.15	2.0	9.0	10	2.0	10.5	ns
		R_L = 1 MΩ C_L = 15 pF	2.5 ± 0.2	1.0		7.5	1.0	8.0	
		R_L = 1 MΩ C_L = 15 pF R_L = 500 Ω C_L = 50 pF	3.3 ± 0.3	0.8 1.2		5.2 5.7	0.8 1.2	5.5 6.0	
		R_L = 1 MΩ C_L = 15 pF R_L = 500 Ω C_L = 50 pF	5.0 ± 0.5	0.5 0.8		4.5 5.0	0.5 0.8	4.8 5.3	
t_{PZH} t_{PZL}	Output Enable Time (Figures 6, 7and 8, Table 1)	R_L = 250 Ω C_L = 50 pF	1.8 ± 0.15	2.0	7.6	9.5	2.0	10	ns
			2.5 ± 0.2	1.8		8.5	1.8	9.0	
			3.3 ± 0.3	1.2		6.2	1.2	6.5	
			5.0 ± 0.5	0.8		5.5	0.8	5.8	
t_{PHZ} t_{PLZ}	Output Disable Time (Figures 6, 7and 8, Table 1)	R_L and R_1= 500 Ω C_L = 50 pF	1.8 ± 0.15	2.0	8.0	10	2.0	10.5	ns
			2.5 ± 0.2	1.5		8.0	1.5	8.5	
			3.3 ± 0.3	0.8		5.7	0.8	6.0	
			5.0 ± 0.5	0.3		4.7	0.3	5.0	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	9 11	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

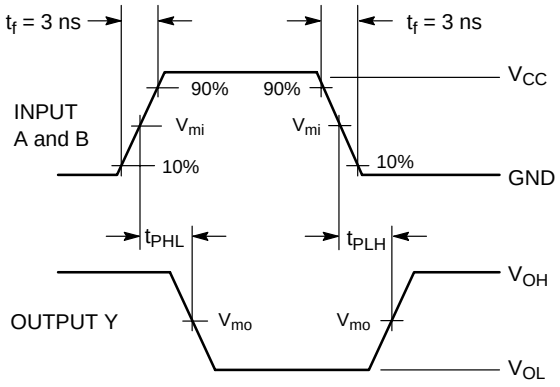
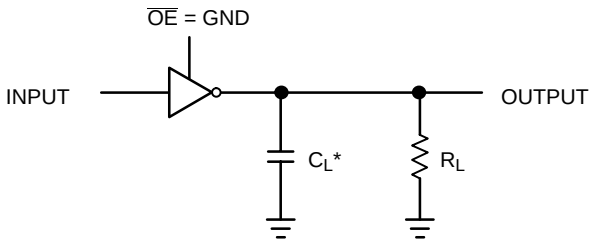
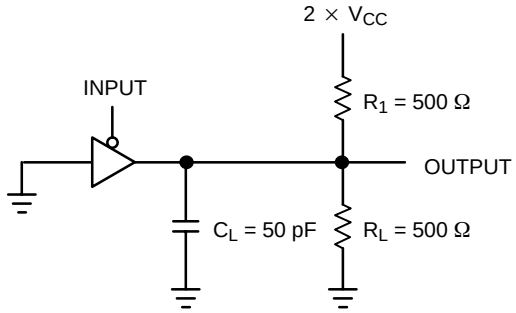


Figure 4. Switching Waveform



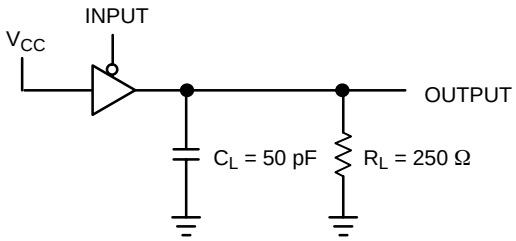
*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 5. T_{PLH} or T_{PHL}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZL} or T_{PL}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 7. T_{PZH} or T_{PHZ}

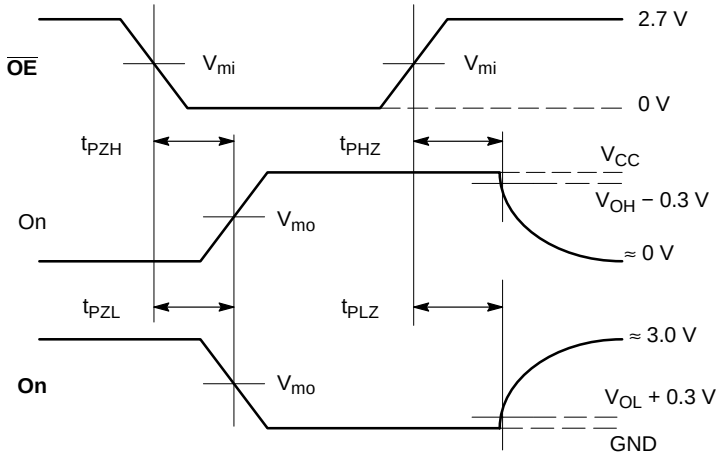


Figure 8. AC Output Enable and Disable Waveform

Table 1. Output Enable and Disable Times
$t_R = t_F$ = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Symbol	V_{CC}		
	3.3 V ± 0.3 V	**2.7 V**	**2.5 V ± 0.2 V**
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

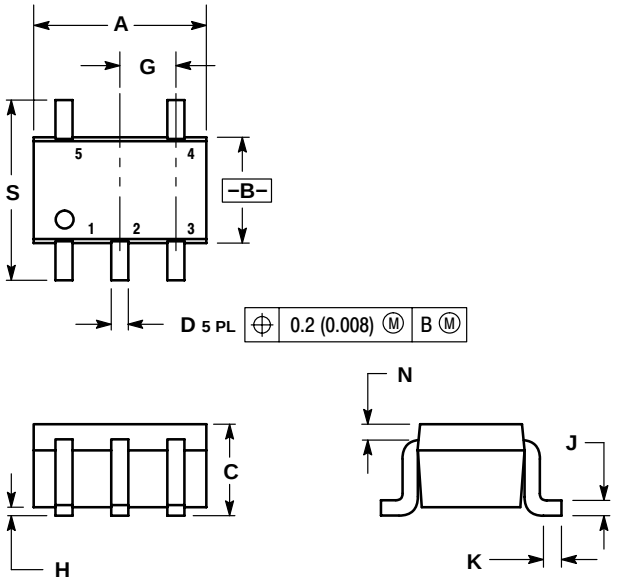
DEVICE ORDERING INFORMATION

Device	Device Nomenclature							Package	Shipping†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZ125DFT2	NL	1	7	SZ	125	DF	T2	SC−88A (SOT−353)	3000 / Tape & Reel 178 mm (7”)
NL17SZ125DFT2G	NL	1	7	SZ	125	DF	T2G	SC−88A (SOT−353) (Pb−Free)	3000 / Tape & Reel 178 mm (7”)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

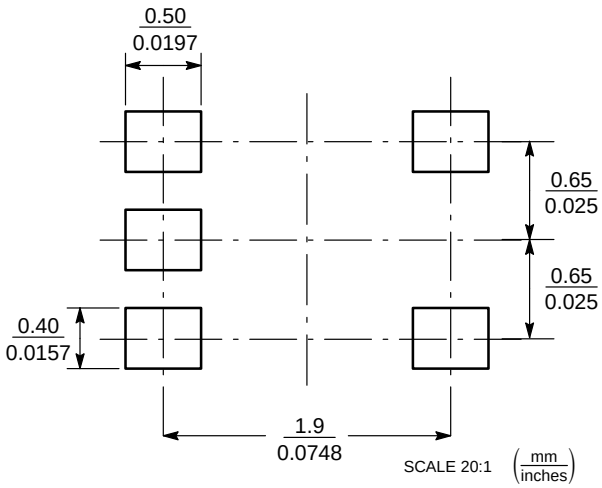
SC−88A (SOT−353)
DF SUFFIX
CASE 419A−02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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