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Selecting the Right Texas Instruments Signal Switch

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ABSTRACT

Texas Instruments offers a wide variety of electronic switches (digital, analog, bilateral, bilateral analog) in a variety of families, including CBT, CBTLV, HC, LV, and LVC. Depending on the application, the right solution may be an analog switch that passes digital signals, or vice versa. This application report summarizes the various switching technologies and provides application considerations for choosing the appropriate TI signal switch.

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1 Introduction

Texas Instruments offers a wide variety of signal switches in a variety of families, including CBT, CBTLV, CD4000, HC, LV-A, and LVC. These signal switches can be digital, analog, bilateral, or bilateral analog. Selecting the right one can be a formidable task. The purpose of this application report is to make the selection process easier by illustrating the differences between the families and removing ambiguity in the naming conventions.

2 Background

When first considering switches, a schematic of the ideal switch (similar to Figure 1) might come to mind.

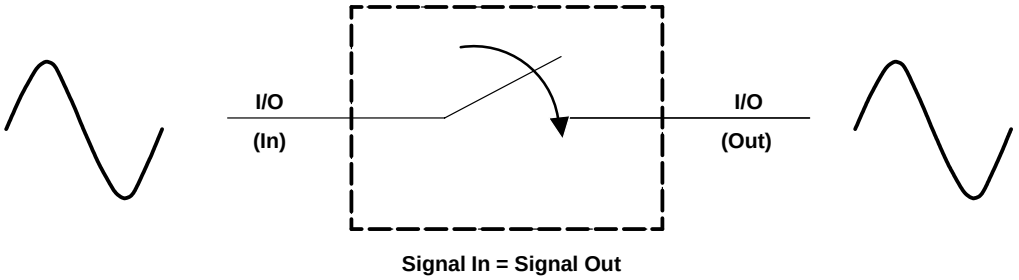


Figure 1. Ideal Switch

An input signal applied to the left I/O pin (or port) in Figure 1 results in an identical output signal at the right I/O pin, and vice versa. However, in the real world, switches are not ideal and there always is some loss. In the case of clean, properly working mechanical switches, the loss is so miniscule that it hardly bears noting.

Like mechanical switches, solid-state switches are not ideal either. In fact, losses associated with solid-state switches can be significant. Why use a switch like this if it is so far from ideal? The answer is convenience. Solid-state switches are small, fast, easy to use, easy to control, and consume relatively little power compared to traditional electrically controlled switches, such as relays. The switches referred to in this application report are complementary metal-oxide semiconductor (CMOS) field-effect transistor (FET) switches. As mentioned previously, they are not ideal, so we need a way to examine and compare the performance characteristics of the different CMOS families. Figure 2 shows a simplified-circuit model of a CMOS switch.

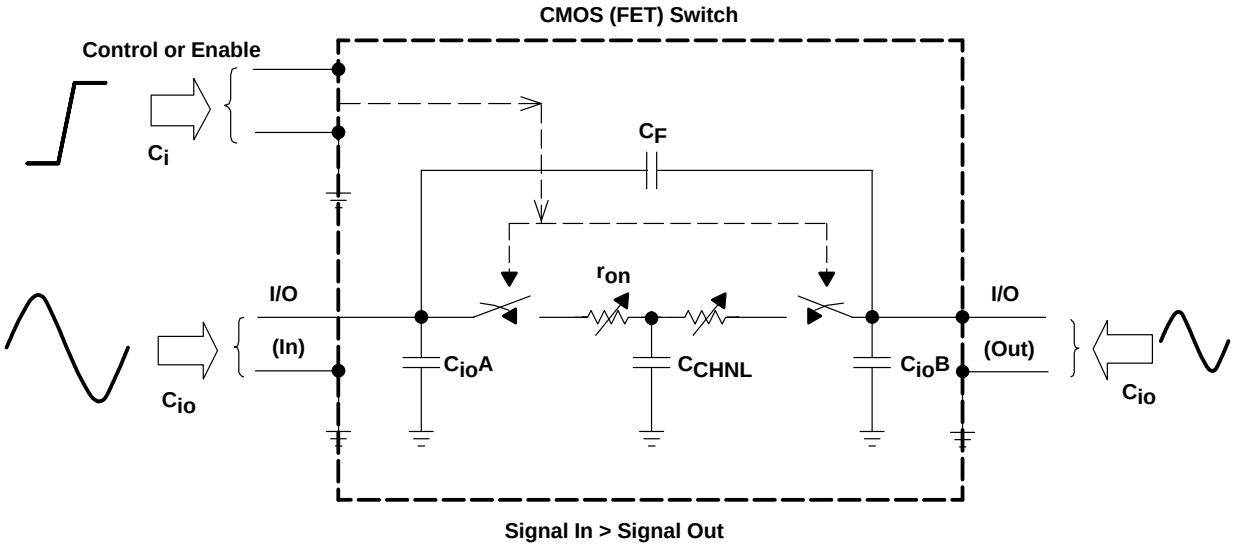


Figure 2. Simplified CMOS (FET) Switch

The output signal (right side, Figure 2) is altered due to parasitic effects of the switch. Results may include decreased amplitude, signal distortion, phase shift, the introduction of noise, and frequency attenuation.

Parameters contributing to the nonideal characteristics include:

- C_i – Control (enable) pin input capacitance
- C_F – Feedthrough capacitance
- C_{io} – Capacitance measured from either the input or output of the switch
- C_{CHNL} – NMOS (PMOS) channel capacitance
- r_{on} – On-state resistance from drain to source $r_{ds(on)}$ of the pass FET

As mentioned previously, TI offers a variety of CMOS-technology switches. Table 1 summarizes the families by switch type.

Table 1. TI Switch Technologies

TECHNOLOGY	ABBREVIATION	SWITCH TYPE
Crossbar	CBT	N-channel FET
CMOS	CD4000	Parallel n-/p-channel FET
High-speed CMOS	HC	Parallel n-/p-channel FET
Low-voltage CMOS	LV-A	Parallel n-/p-channel FET
Low-voltage CMOS	LVC	Parallel n-/p-channel FET
Low-voltage crossbar	CBTLV	Parallel n-/p-channel FET

2.1 Single FET Switch

Figure 3 shows a simplified FET switch, which consists of an n-channel transistor and gate bias and enable circuitry. The switch is bidirectional; the source and drain are interchangeable (while operating, the side with the lowest $V_{I/O}$ is the source). TI CBT bus switches are this type.

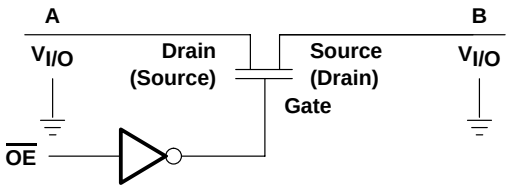


Figure 3. N-Channel FET Switch

For an n-channel FET to operate properly, the gate should be biased more positive than the magnitude of the signals to be passed. This is because the on-state resistance, r_{on} (or $r_{DS(on)}$ as it also is called), increases as the gate, minus source voltage, V_{GS}, decreases. In the case of CBT, when $\overline{OE}$ is low, the gate of the FET is biased to near V_{CC}. If the lowest $V_{I/O}$ signal approaches the magnitude of V_{CC}, V_{GS} decreases and r_{on} increases (see Figure 4). The ability to maintain a low r_{on} in a FET switch depends on maintaining V_{GS} as large as possible. In many applications, this characteristic is not a problem, but the designer should be aware of the nonlinearity of this type of device.

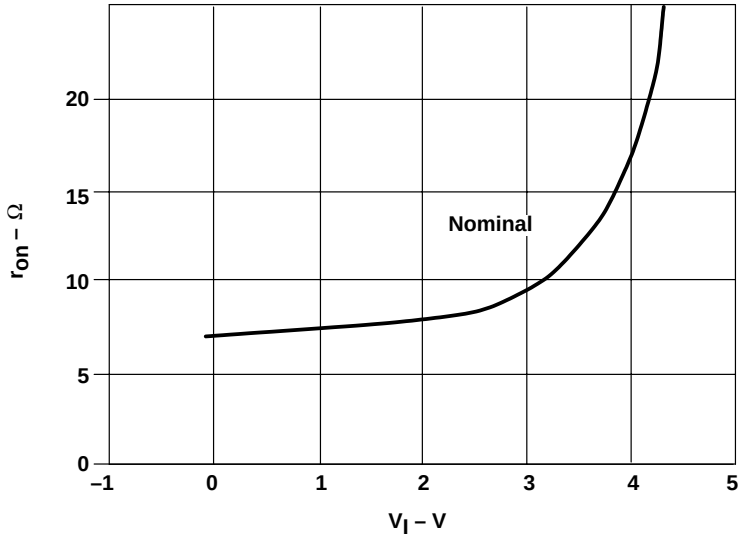


Figure 4. On-State Resistance vs Lowest I/O Voltage for an n-Channel FET Switch With V_{CC} = 5 V

2.2 Analog (Bilateral) Switches

Analog (or bilateral, as they also are called) switches consist of a single n-channel transistor in parallel with a single p-channel transistor (see Figure 5).

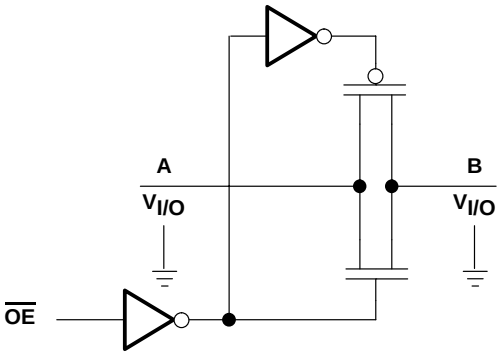


Figure 5. Parallel n-/p-Channel FET Switch

As before, when $V_{I/O}$ approaches V_{CC}, the n-channel conductance decreases (r_{on} increases) while the p-channel gate-source voltage is maximum and its r_{on} is minimal. The resulting parallel resistance combination is much flatter than individual channel resistances (see Figure 6).

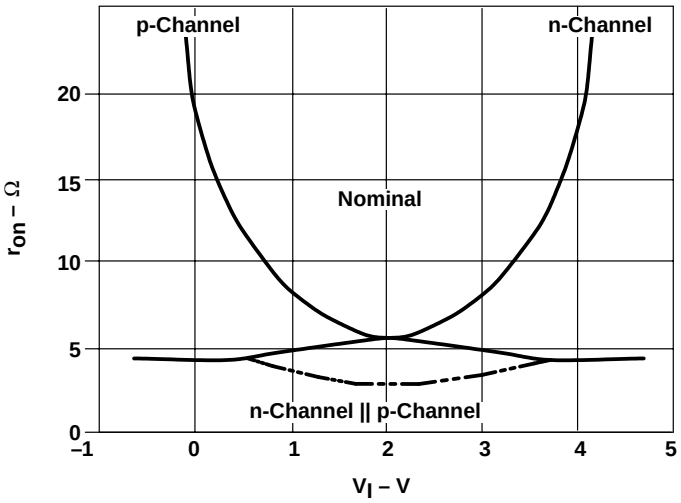


Figure 6. On-State Resistance vs Input Voltage for a Parallel n-/p-Channel FET Switch

A flat r_{on} is especially important if $V_{I/O}$ signals must swing from rail to rail. However, the tradeoff is increased switch capacitance due to the additional p-channel transistor and associated bias circuitry. TI offers a variety of choices of analog switches: HCT, HC, CD4000, LV-A, LVC, and CBTLV.

Some manufacturers offer n-channel signal switches with charge-pump-enabled pass transistors. A design of this type allows the gate voltage to be higher than V_{CC}. This increases V_{GS} above what is possible in noncharge-pump devices and allows signals at or above V_{CC} to be passed. A switch of this type has the advantage of low, relatively flat r_{on} (over the signal range), without the addition of a p channel and while maintaining C_{io} values comparable to pure n-channel FET switches. This performance comes at the expense of increased I_{CC} (from a few μA to several mA in some cases).

2.3 Analog Versus Digital Signal Switches

TI offers a wide variety of signal switches, and sometimes the nomenclature can be confusing to the point of implying limited functionality for a device or family. In reality, a switch, is a switch, is a switch (well, almost):

- Digital switch. Designed to pass (or isolate) digital signal levels. May exhibit the capability to satisfactorily pass analog signals. Examples are CBT and CBTLV switch families.
- Analog switch. Designed to pass (or isolate) analog signals. Often exhibits good digital signal performance as well. Examples are CD4066B, CD74HCT4066, CD74HC4066, SN74HC4066, SN74LV4066A, and SN74LVC1G66 switches.
- Bilateral switch. There are two meanings:
  - Signals can be passed in either direction (A to B, or B to A) through the switch.
  - Switch can be used in analog or digital applications.

  Examples are CD4066B, CD74HCT4066, CD74HC4066, SN74HC4066, SN74LV4066A, and SN74LVC1G66 switches.
- Bus switch. Digital switches designed for multibit switching in computing applications. Examples are CBT and CBTLV switch families.

The name bus switch implies digital only. However, with better understanding of switch characteristics, it is apparent that this view of their application might be too limited. Tables 2, 4, 5, 6, 7 and 14 summarize the performance of the CBT3125 and CBTLV3125 quadruple FET bus switches versus other TI bilateral analog switches. With regard to analog performance, these bus switches outperformed at least one bilateral switch in every parameter measurement.

It should be apparent that the most important switch characteristic depends on how it is used:

- What V_{CC} levels are present?
- What amplitude signals are required to be passed?
- What is the maximum signal distortion limit for the system?

In the following paragraphs, performance of TI signal switches is summarized to aid in the selection of the best signal switch for a given application.

2.4 Application Considerations

2.4.1 Digital Signal Considerations

- V_{CC}. There are a number of considerations and tradeoffs here. What voltage levels are present on the board? What is the amplitude of the signal levels to be passed? Is level translation required?
- V_{IH}/V_{IL}. Switch control (Enable). How will the switch be controlled? Logic level output? Comparator? ASIC? Should the switch turn on if the control signal is high or low?
- Switch output level. The maximum signal level a switch without a charge pump can pass is limited to the switch V_{CC}. Is there sufficient noise margin on the device downstream of the switch such that signal attenuation in the switch will not cause data errors? For instance, the n-channel transistor of a CBT device clamps the switch output at a little more than 1 V below the operating V_{CC}, making it unsuitable for 5-V CMOS high-level (V_{IH} = 3.5 V) signal transmission unless operated from at least 4.5-V V_{CC}.
- r_{on}.
  - Is the switch connected to a transmission line? If so, what is the impedance? The switch r_{on} should be less than or equal to the line impedance to allow for proper matching and to prevent unwanted signal reflections.
  - For nontransmission-line connections, the switch r_{on} and the load resistance form an undesired voltage divider. In this case, that is a switch with a r_{on} small enough to ensure the switch output is not reduced below a valid input high level (V_{IH}) for the connected load. As mentioned previously, the tradeoff for low r_{on} is often higher signal-path capacitance, which reduces frequency response.
- t_{en}/t_{dis}. These parameters determine how quickly the switch can respond to a desired on or off state. In general, switch enable and disable times are not symmetrical. This is not usually an issue, as few applications require high control (enable) signal frequencies.
- t_{pd}. This parameter is negligible for all but the most critical timing budgets. When the switch is on, the propagation delay through the pass transistor(s) is minimal. TI specifies this number as the mathematical calculation of the typical r_{on} times the load capacitance.
- Number of bits required to be switched. With TI's wide variety of signal switches, it is possible to switch between 1 to 32 bits at the same time with a single device. For instance, the LVC1G66 or CBT1G125 can be used to switch a single bit, while the CBTLV16211 is capable of switching 24 bits total in banks of 12. Or, by tying the adjacent enable pins together, it is possible to control 24 bits with one enable signal.
- Special features. TI offers bus switches with special features, such as an integrated diode for single-component level shifting (CBTD), active clamps for undershoot protection (CBTK), Schottky-diode clamps for undershoot protection (CBTS), a bus-hold option (CBTH) for holding floating or unused I/O pins at valid logic levels, and an integrated-series-resistor option (CBTR) to reduce signal-reflection noise.

Table 2 summarizes the digital performance characteristics of eight TI signal switches from which generalities can be derived regarding switch-family performance. For exact parameters, refer to the respective data sheets.

2.4.2 Digital Performance

Table 2. Summary of Digital Performance†

PARAMETER	CD4066	CD74HC4066	CD74HCT4066	SN74HC4066	LVC1G66	LV4066A	CBT3125	CBTLV3125
V_{CC}	3–18 V	2–10 V	4.5–5.5 V	2–6 V	1.65–5.5V	2–5.5 V	4–5.5 V	2.3–3.6 V
r_{on}	200–1300 Ω	15–142 Ω	25–142 Ω	30–150 Ω	3–30 Ω	21–225 Ω	5–22 Ω	5–40 Ω
t_{pd}‡	7–40 ns	4–90 ns	4–18 ns	3–75 ns	0.6–2 ns	0.3–18 ns	0.25–0.35ns	0.15–0.25 ns
t_{en}§	15–70 ns	8–150 ns	4–18 ns	18–225 ns	1.5–10 ns	1.6–32 ns	1.8–5.6 ns	2–4.6 ns
t_{dis}¶	15–70 ns	12–225 ns	9–36 ns	22–250 ns	1.4–10 ns	3.2–32 ns	1–4.6 ns	1–4.2 ns
V_{IH} (control inputs)	approx. $0.7 \times V_{CC}$	5-V CMOS	5-V TTL	5-V CMOS	5-V CMOS	5-V CMOS	5-V TTL/ LVTTL	LVTTL/ 2.5-V CMOS
V_{IL} (control inputs)	approx. $0.2 \times V_{CC}$	5-V CMOS	5-V TTL	5-V CMOS	5-V CMOS	5-V CMOS	5-V TTL/ LVTTL	LVTTL/ 2.5-V CMOS
C_i (control)	5–7.5 pF	10 pF	10 pF	3–10 pF	2 pF	1.5 pF	3 pF	2.5 pF
C_{io} (on)					13 pF			
C_{io} (off)	8 pF	5 pF	5 pF	9 pF	6 pF	5.5 pF	4 pF	7 pF

† Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.
‡ t_{pd} is the same as t_{PLH}/t_{PHL}. The switch contributes no significant propagation delay other than the RC delay of the typical on-state resistance of the switch and the load capacitance when driven by an ideal voltage source (zero output impedance)
§ t_{en} is the same as t_{PZL}/t_{PZH}.
¶ t_{dis} is the same as t_{PLZ}/t_{PHZ}.

2.4.3 Analog Signal Considerations

- V_{CC}. For noncharge-pump switches, V_{CC} determines the amplitude of the analog signals that can be passed without clipping. The gate(s) of the pass transistors must be biased relative to the minimum and maximum values of the expected input voltage range. Switches, such as the CD4000 series, allow for biasing from two supplies, making it easy to pass both positive and negative signals. Switches with integrated charge pumps can elevate the gate voltage above V_{CC} (at the expense of larger I_{CC}) and, thus, pass signals of a magnitude greater than V_{CC}.
- V_{IH}/V_{IL}. Why are these important analog switch considerations? In most applications, the signal switch is controlled by the output of a digital source, therefore, the control signal levels, V_{IH} and V_{IL}, must be compatible with that source to ensure proper operation of the switch. The CD74HC4066 and CD74HCT4066 are excellent examples of switches with almost exactly the same performance characteristics, but very different control signal levels. The V_{IH} of the CD74HC4066 is 3.15 V, with V_{CC} at 4.5 V, while CD74HCT4066 is specified with V_{IH} of 2 V for V_{CC} between 4.5 and 5.5 V.
- r_{on}. Because it contributes to signal loss and degradation, low r_{on} tradeoffs must be considered. Noncharge-pump switches achieve low r_{on} with large pass transistors. These larger transistors lead to larger die sizes and increased C_{io}. This additional channel capacitance can be very significant as it limits the frequency response of the switch. As stated in section 2.4.1, switches utilizing charge-pump technology can achieve low r_{on} and C_{io}, but require significantly higher I_{CC}.

- Frequency response. All CMOS switches have an upper limit to the frequency that can be passed. No matter how low r_{on} and C_{io} can be maintained in the chip manufacturing process, they still form an undesired low-pass filter that attenuates the switch output signal.
- Sine-wave distortion or total harmonic distortion. These are measurements of the linearity of the device. Nonlinearity can be introduced a number of ways (design, device physics, etc.) but, typically, the largest contributor is r_{on}. As shown in Figures 2 and 4, r_{on} varies with $V_{I/O}$ for all types of CMOS switches. Having a low r_{on} is important, but a flat r_{on} over the signal range is almost equally important. N-channel switches, such as CBT, exhibit very flat r_{on} characteristics for signal ranges of $0 < V_{I/O} < (V_{CC} – 2\ V)$, but r_{on} increases very rapidly as $V_{I/O}$ approaches V_{CC} and V_{GS} decreases. Parallel n-/p-channel switches offer good r_{on} flatness for signal ranges of $0 < V_{I/O} < V_{CC}$, with the best flatness characteristic at the highest recommended switch V_{CC}.
- Crosstalk. There are two types of crosstalk to consider:
  - Control (enable) to output. The level of crosstalk is a measure of how well decoupled the switch control signal is from the switch output. Due to the parasitic capacitance of CMOS processes, changing the state on the control signal causes noise to appear on the output. In audio applications, this can be a source of the annoying pop that is sometimes heard when switching the unit on or off.
  - Between switches. The level of crosstalk also is a measure of adjacent-channel rejection. As with control-to-output crosstalk, parasitic capacitance can couple the signal on one switch with that on another switch.
- Charge Injection (Q). TI specifies enable-to-output crosstalk and some competitors use this parameter. As with enable-to-output crosstalk, changing the state on the control pin causes a charge to be coupled to the channel of the transistor introducing signal noise. It is presented in this report for a relative comparison with the competition.
- Feedthrough. This characteristic is related to the ability of the switch to block signals when off. As with crosstalk, parasitic capacitance allows high frequencies to couple through the switch, making it appear to be on.

2.4.4 Analog Performance

Table 3. V_{CC} Above 5.5 V†

PARAMETER	← BETTER PERFORMANCE		
r_{on} (typical to maximum)	CD74HC4066 15–126 Ω	CD74HC4066‡ 30 Ω	CD4066 200–550 Ω
r_{on} (peak) (typical to maximum)	SN74HC4066‡ 50 Ω (typ)	CD74HC4066 not specified	CD4066 not specified
Frequency response	CD74HC4066§ 200 MHz	CD4066 40 MHz	SN74HC4066§ 30 MHz
THD/Sine-wave distortion	CD74HC4066 0.008%	SN74HC4066§ 0.05%	CD4066 0.4%
Crosstalk (enable to output)	SN74HC4066 20 mV	CD4066 50 mV	CD74HC4066 550 mV
Crosstalk (between switches)	CD4066 –50 dB at 8 MHz	CD74HC4066§ –72 dB at 1 MHz	SN74HC4066§ –45 dB at 1 MHz
Feedthrough attenuation	CD74HC4066§ –72 dB at 1 MHz	CD4066 –50 dB at 1 MHz	SN74HC4066§ –42 dB at 1 MHz

† Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.
‡ Specification at V_{CC} = 6 V
§ Specification at V_{CC} = 4.5 V

Table 4. V_{CC} = 4.5 V†

PARAMETER	← BETTER PERFORMANCE					
r_{on} (typical to maximum)	LVC1G66 3–10 Ω	CBT3125‡ 5–15 Ω	LV4066A 21–100 Ω	CD74HC/ HCT4066 25–142 Ω	SN74HC4066 50–106 Ω	CBT3125§ 5–1000 Ω
r_{on} (peak) (typical to maximum)	CBT3125‡§ 10 Ω	LVC1G66 6–15 Ω	LV4066A 31–125 Ω	CD74HC/ HCT4066§ 50–70 Ω	SN74HC4066 70–215 Ω	CBT3125§ 1000 Ω
Frequency response	CBT3125‡§ >200 MHz	LVC1G66 195 MHz	CD74HC/ HCT4066¶ 200 MHz	LV4066A 50 MHz	SN74HC4066 30 MHz	
THD/Sine-wave distortion	LVC1G66 0.01%	CD74HC/ HCT4066 0.023%	CBT3125‡§ 0.035%	SN74HC4066 0.05%	LV4066A 0.1%	
Crosstalk (enable to output)	SN74HC4066 15 mV	LV4066A 50 mV	LVC1G66 100 mV	CBT3125§ 120 mV	CD74HCT4066 130 mV	CD74HC4066 200 mV
Crosstalk (between switches)	CD74HC/HCT4066 –72 dB	LVC2G66 –58 dB	CBT3125‡§ –53 dB	SN74HC4066 –45 dB	LV4066A –45 dB	
Feedthrough attenuation	CD74HC/HCT4066 –72 dB	LVC1G66 –58 dB	SN74HC4066 –42 dB	LV4066A –40 dB	CBT3125§ –36 dB	

† Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.
‡ CBT3125, $0 \le V_{I/O} \le (V_{CC} - 2\ V)$
§ Value from application report measurement. Not specified in data sheet.
¶ Ranked here due to load variation from other devices in this report

Table 5. V_{CC} = 3 V†

PARAMETER	◀ BETTER PERFORMANCE				
r_{on} (typical to maximum)	LVC1G66 6–15 Ω	CBTLV3125 5–15 Ω	LV4066A 29–190 Ω	CD74HC4066‡ Not specified	SN74HC4066‡ Not specified
r_{on} (peak) (typical to maximum)	CBTLV3125§ 15–20 Ω	LVC1G66 12–20 Ω	LV4066A 57–225 Ω	CD74HC4066‡ Not specified	SN74HC4066‡ Not specified
Frequency response	CBTLV3125§ >200 MHz	LVC1G66 175 MHz	CD74HC4066‡ Not specified	LV4066A 35MHz	SN74HC4066† Not specified
THD/Sine-wave distortion	LVC1G66 0.015%	CD74HC4066‡ Not specified	SN74HC4066‡ Not specified	CBTLV3125§ 0.09%	LV4066A 0.1%
Crosstalk (enable to output)	SN74HC4066‡ Not specified	LV4066A 20 mV	LVC1G66 70 mV	CBTLV3125§ 70 mV	CD74HC4066‡ Not specified
Crosstalk (between switches)	CD74HC4066‡ Not specified	LVC2G66 –58 dB	CBTLV3125§ –49 dB	SN74HC4066‡ Not specified	LV4066A –45 dB
Feedthrough attenuation	CD74HC4066‡ Not specified	LVC1G66 –58 dB	CBTLV3125 –52 dB	SN74HC4066‡ Not specified	LV4066A –40 dB

† Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.
‡ Position in table based on estimated performance. Information not specified in data sheet.
§ Value from application report measurement. Not specified in data sheet.

Table 6. V_{CC} = 2.5 V†

PARAMETER	◀ BETTER PERFORMANCE				
r_{on} (typical to maximum)	LVC1G66 9–20 Ω	CBTLV3125 5–40 Ω	LV4066A 38–225 Ω	CD74HC4066‡ Not specified	SN74HC4066§ 150 Ω
r_{on} (peak) (typical to maximum)	CBTLV3125¶ 15–45 Ω	LVC1G66 20–30 Ω	LV4066A 143–600 Ω	CD74HC4066‡ Not specified	SN74HC4066§ 320 Ω
Frequency response	CBTLV3125¶ >200 MHz	LVC1G66 120 MHz	CD74HC4066‡ Not specified	LV4066A 30 MHz	SN74HC4066‡ Not specified
THD/Sine-wave distortion	LVC1G66 0.025%	CD74HC4066‡ Not specified	SN74HC4066‡ Not specified	LV4066A 0.1%	CBTLV3125¶ 0.11%
Crosstalk (enable to output)	SN74HC4066‡ Not specified	LV4066A 15 mV	CBTLV3125‡ 30 mV	LVC1G66 50 mV	CD74HC4066‡ Not specified
Crosstalk (between switches)	CD74HC4066‡ Not specified	LVC2G66 –58 dB	CBTLV3125 –45 dB	SN74HC4066‡ Not specified	LV4066A –45 dB
Feedthrough attenuation	CD74HC4066‡ Not specified	LVC1G66 –58 dB	CBTLV3125 –52 dB	SN74HC4066‡ Not specified	LV4066A –40 dB

† Data are based on data-sheet parameters for the parts tested for this application report. Refer to the respective data sheets for specific parameters and load conditions.
‡ Position in table based on estimated performance. Information not specified in data sheet.
§ Data at V_{CC} = 2 V
¶ Value from application report measurement. Not specified in data sheet.

2.4.5 SN74CBT Characteristics

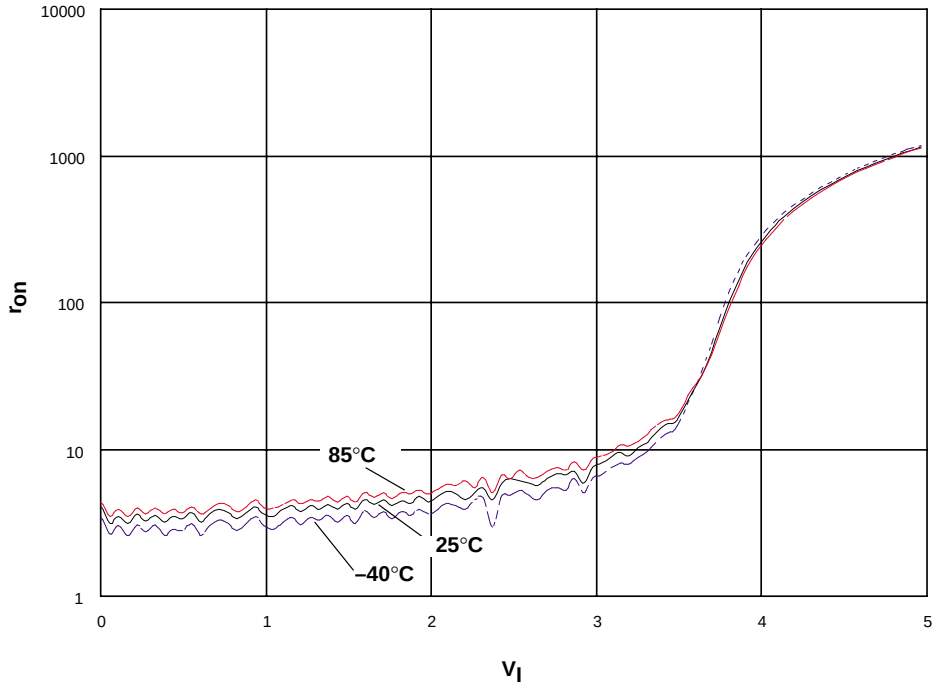


Figure 7. Log r_{on} vs V_I, V_{CC} = 5 V (SN74CBT3125)

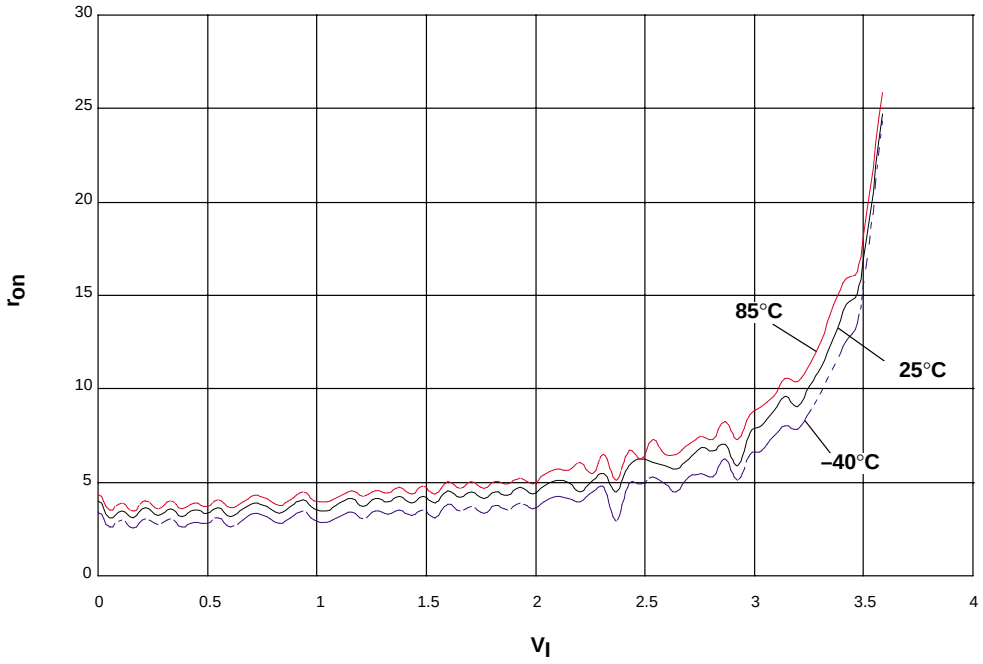


Figure 8. r_{on} vs V_I, V_{CC} = 5 V (SN74CBT3125)

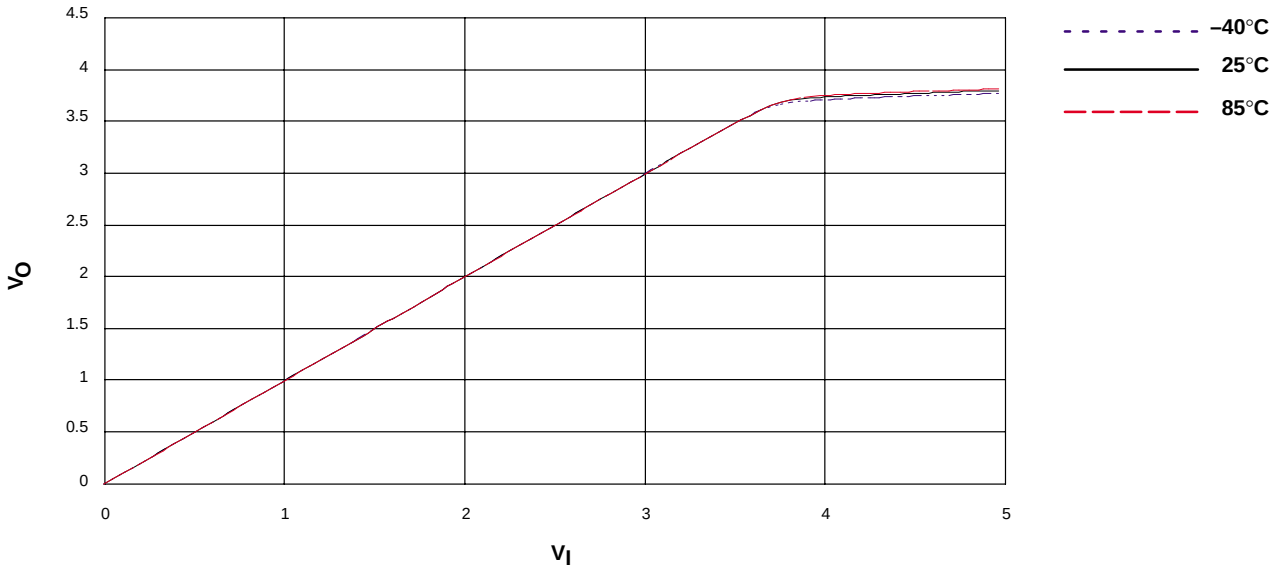


Figure 9. V_I vs V_O, V_{CC} = 5 V (SN74CBT3125)

Table 7. SN74CBT3125 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion	Total Harmonic Distortion	Crosstalk		Charge Injection	Feedthrough
		1 kHz		Between Switches	Enable to Output		
5 V	>200 MHz	0.035%	0.15%	–53 dB	120 mV	7.2 pC	–36 dB

† Postcharacterization measurement for SN74CBT3125

2.4.6 CD74HCT Characteristics

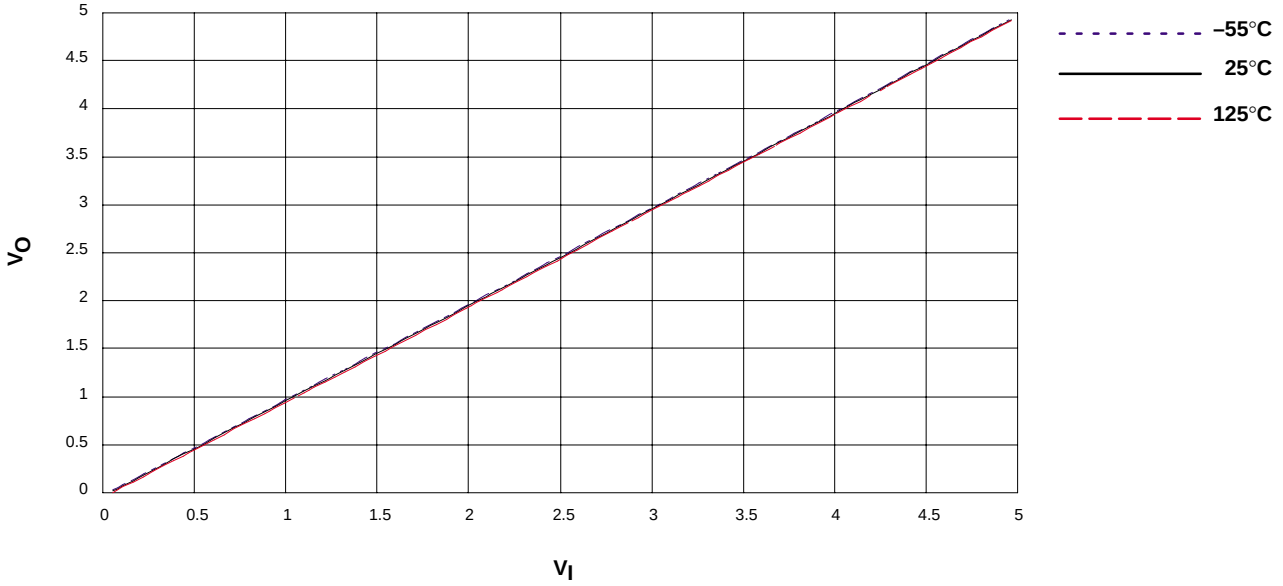


Figure 10. V_I vs V_O, V_{CC} = 5 V (CD74HCT4066)

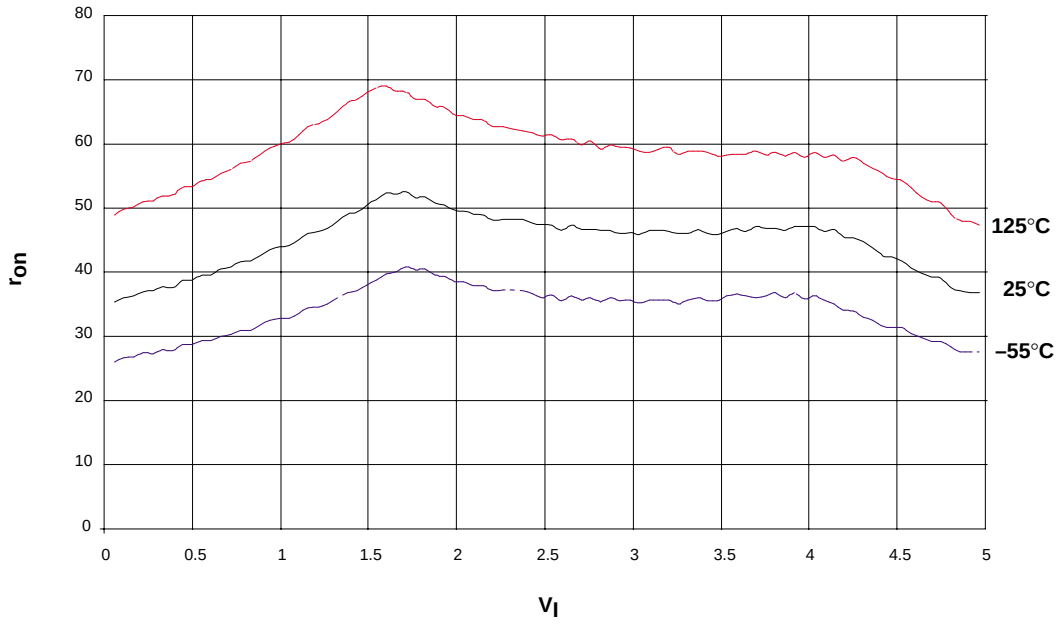


Figure 11. r_{on} vs V_I, V_{CC} = 5 V (CD74HCT4066)

Table 8. CD74HCT4066 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection‡	Feedthrough
		1 kHz	Between Switches	Enable to Output		
4.5 V	200 MHz	0.023%	–72 dB	130 mV	8.1 pC	–72 dB

† Data-sheet values for CD74HCT4066, except as noted
‡ Postcharacterization measurement for CD74HCT4066

2.4.7 CD74HC Characteristics

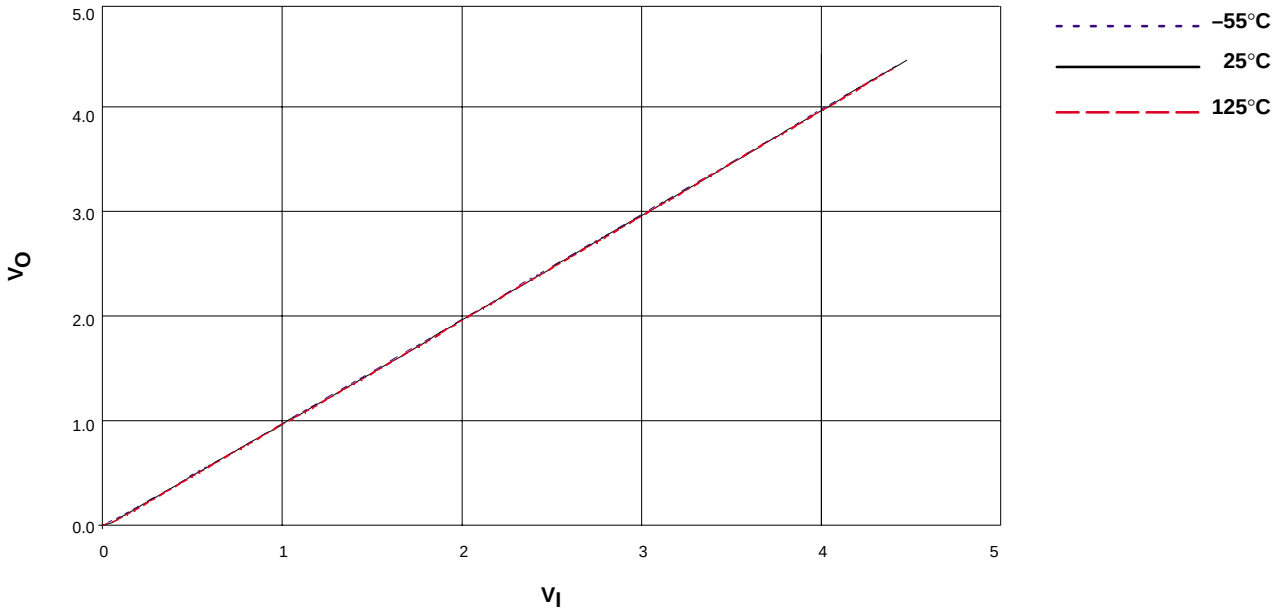


Figure 12. V_I vs V_O, V_{CC} = 4.5 V (CD74HC4066)

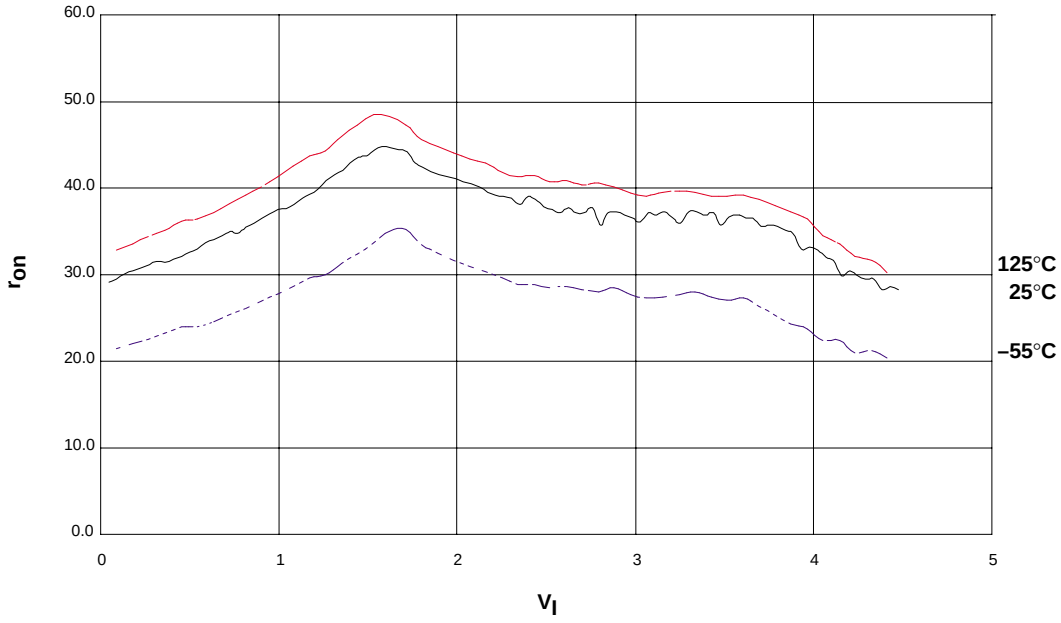


Figure 13. r_{on} vs V_I, V_{CC} = 4.5 V (CD74HC4066)

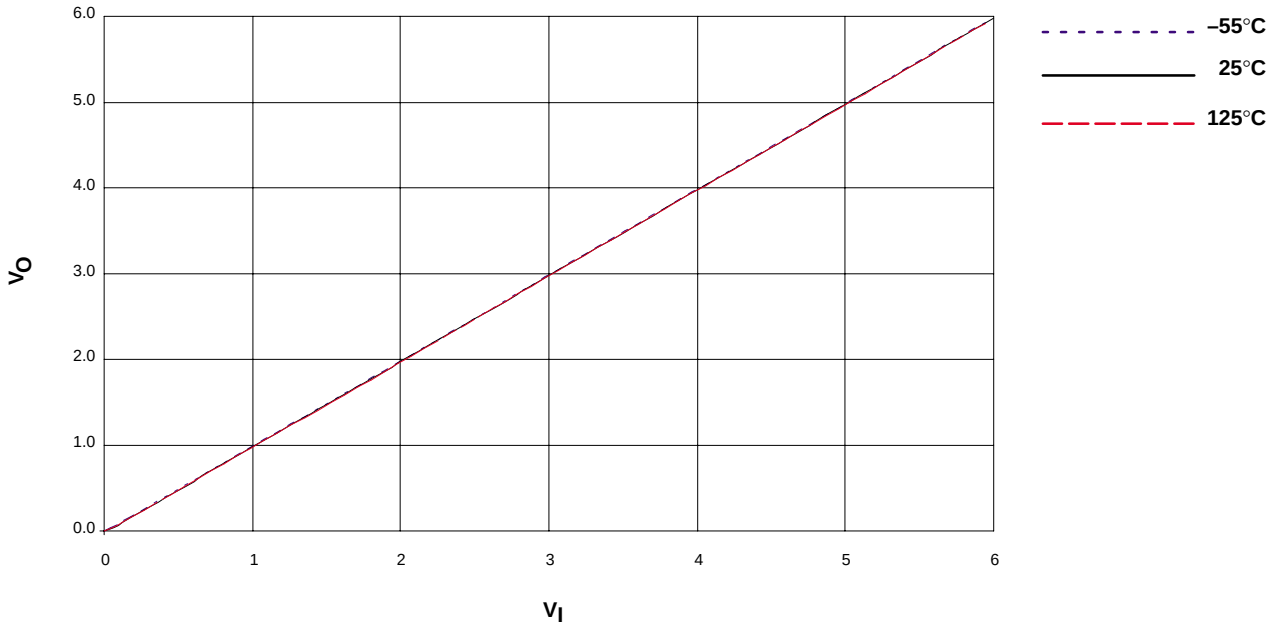


Figure 14. V_O vs V_I, V_{CC} = 6 V (CD74HC4066)

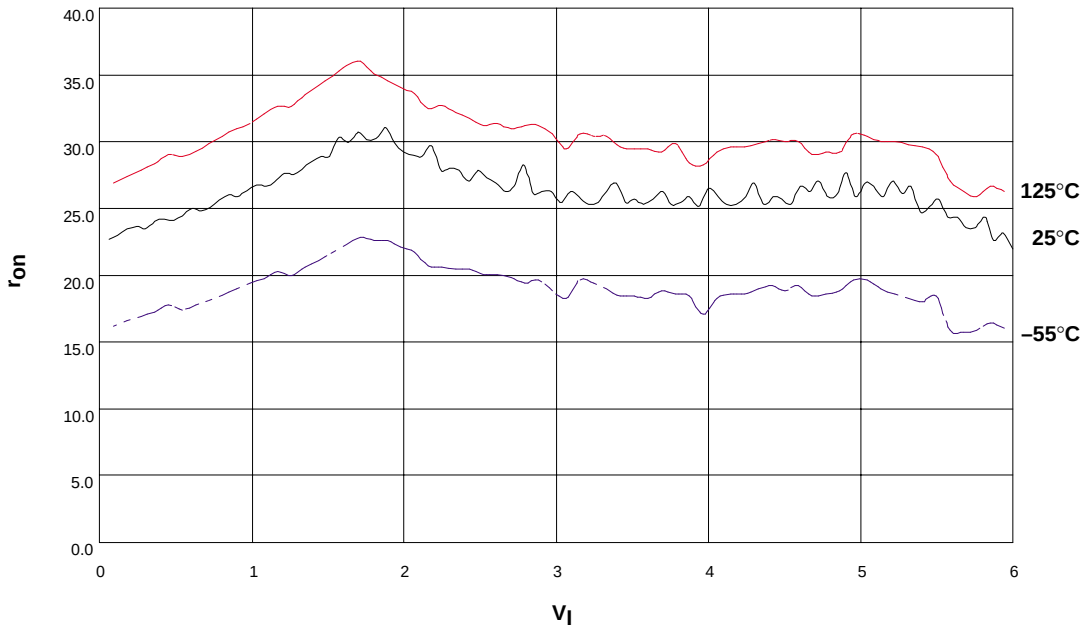


Figure 15. r_{on} vs V_I, V_{CC} = 6 V (CD74HC4066)

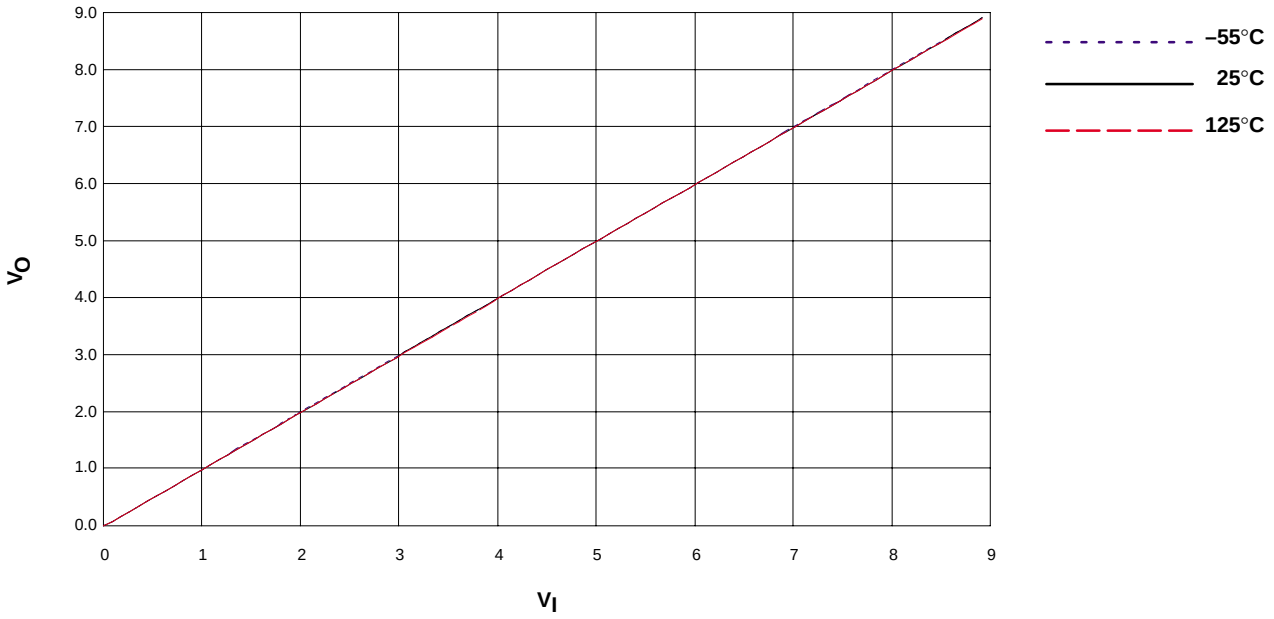


Figure 16. V_O vs V_I, V_{CC} = 9 V (CD74HC4066)

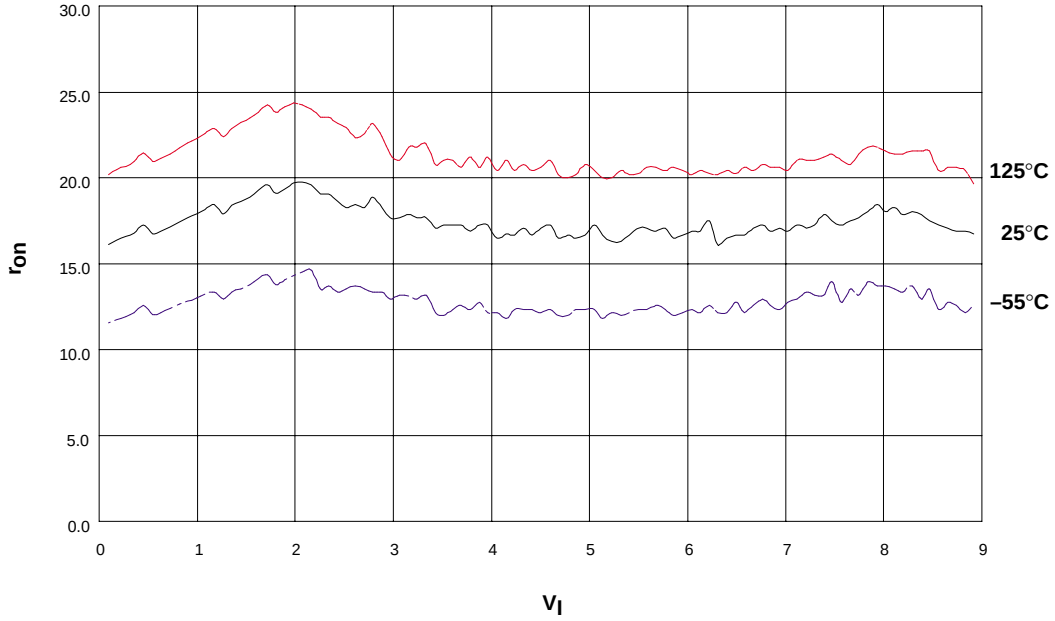


Figure 17. r_{on} vs V_I, V_{CC} = 9 V (CD74HC4066)

Table 9. CD74HC4066 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection‡	Feedthrough
		1 kHz	Between Switches	Enable to Output		
4.5 V	200 MHz	0.022%	–72 dB	200 mV	6.2 pC	–72 dB
9 V	200 MHz	0.008%	N/A	550 mV	9.0 pC	N/A

† Data-sheet values for CD74HC4066, except as noted
‡ Postcharacterization measurement for CD74HC4066

2.4.8 SN74HC Characteristics

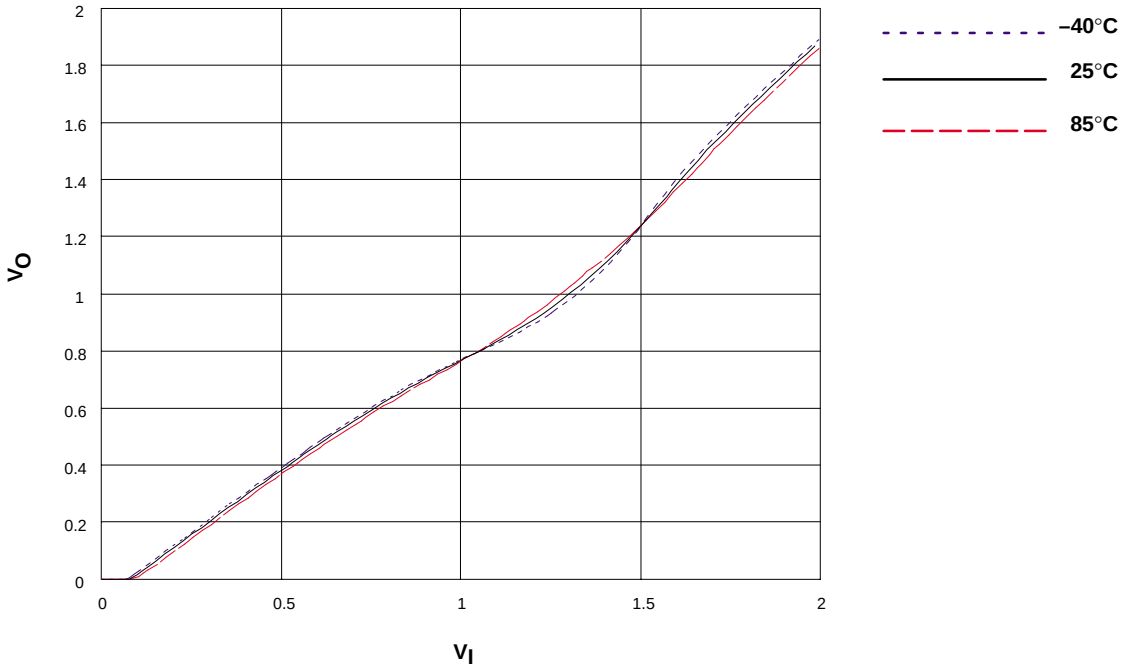


Figure 18. V_O vs V_I, V_{CC} = 2 V (SN74HC4066)

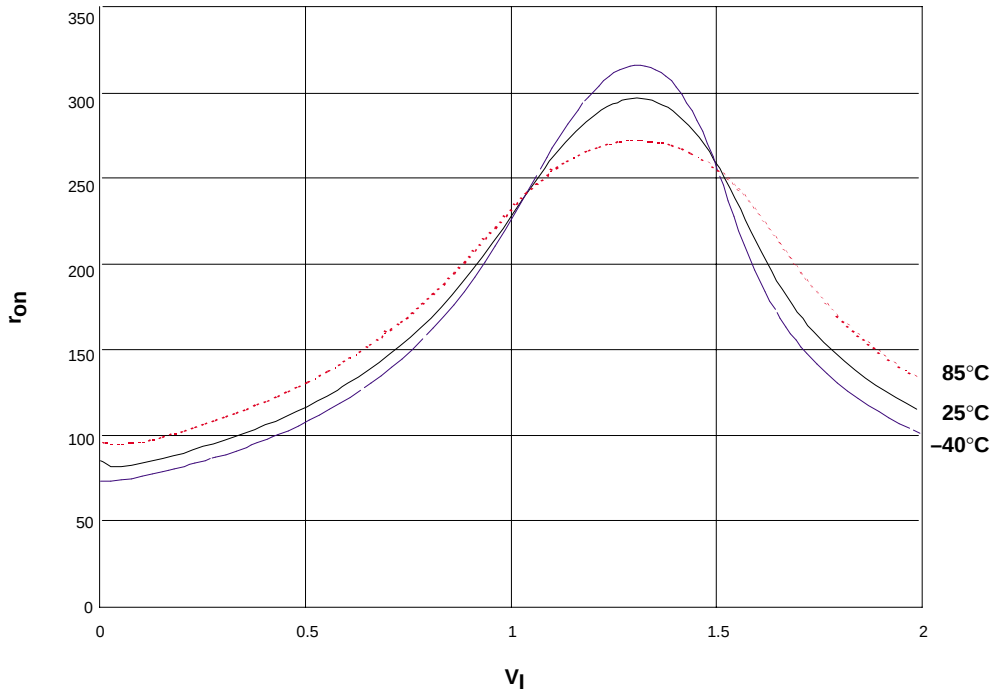


Figure 19. r_{on} vs V_I, V_{CC} = 2 V (SN74HC4066)

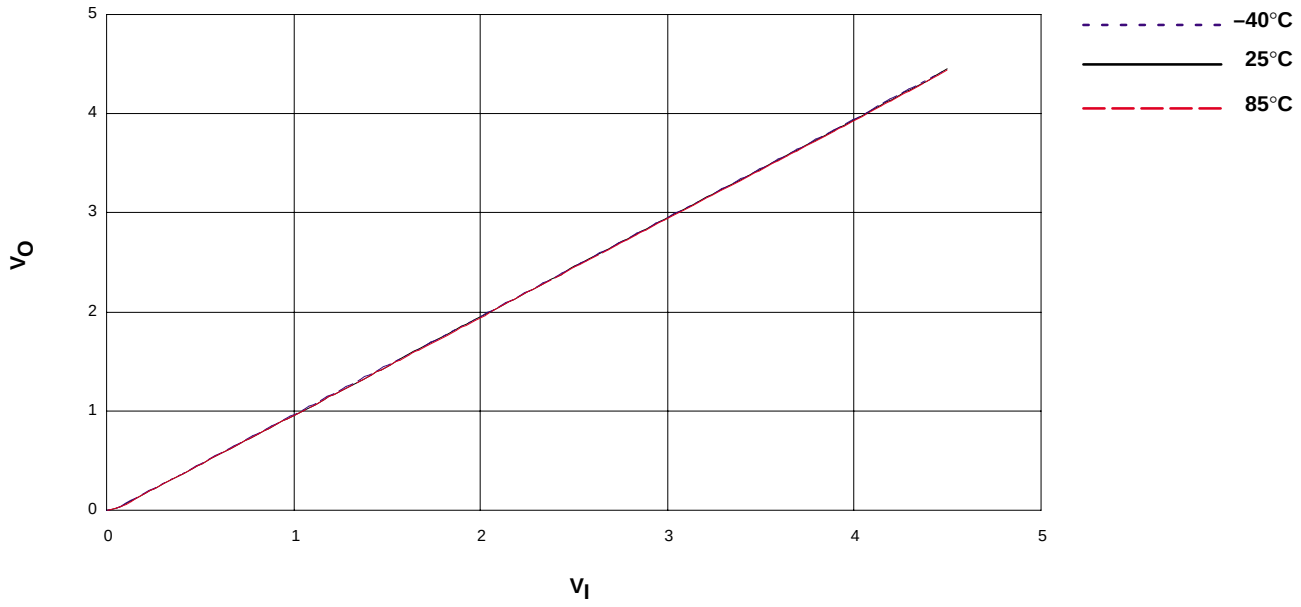


Figure 20. V_O vs V_I, V_{CC} = 4.5 V (SN74HC4066)

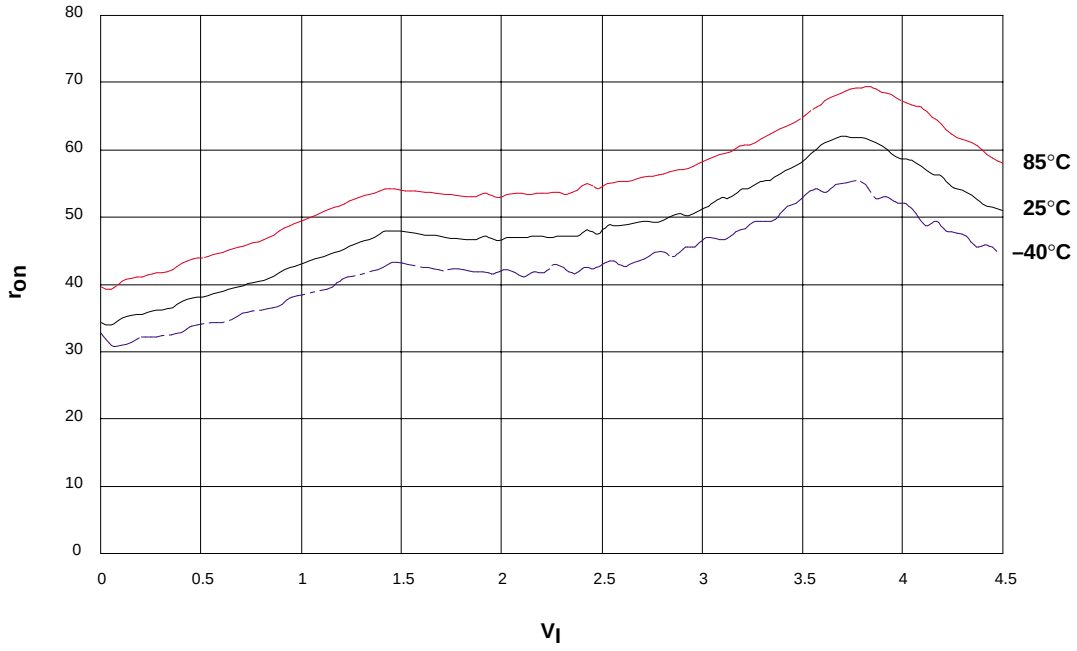


Figure 21. r_{on} vs V_I, V_{CC} = 4.5 V (SN74HC4066)

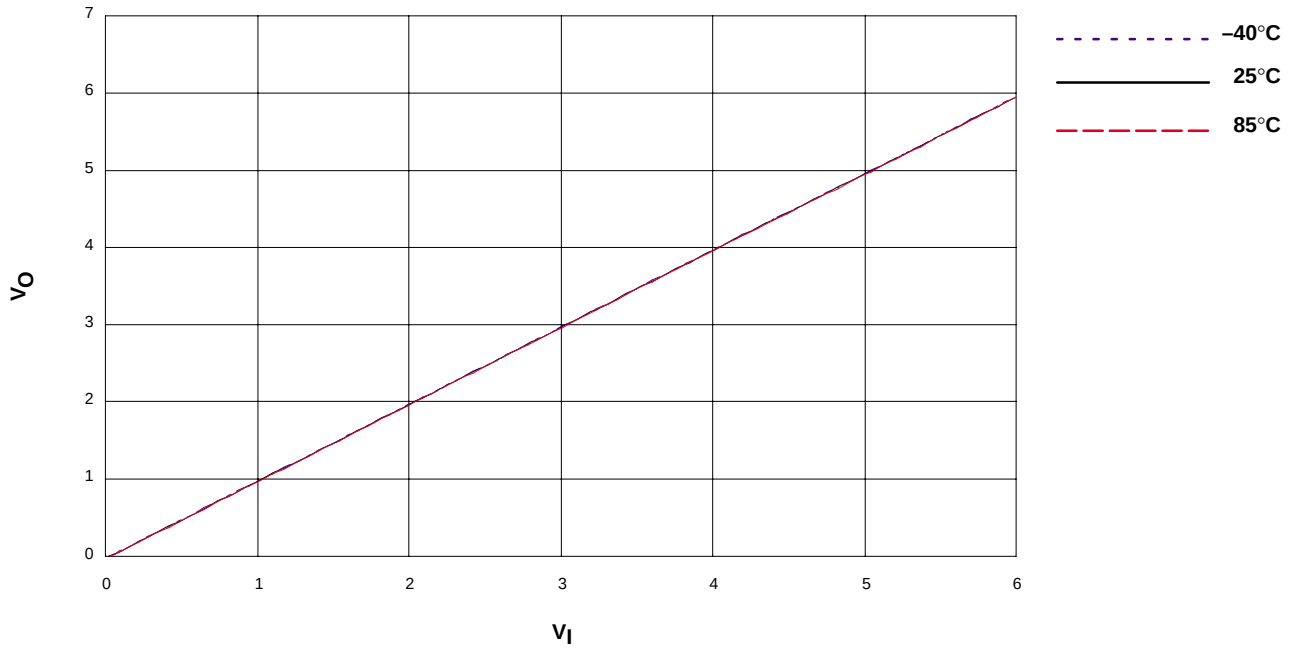


Figure 22. V_O vs V_I, V_{CC} = 6 V (SN74HC4066)

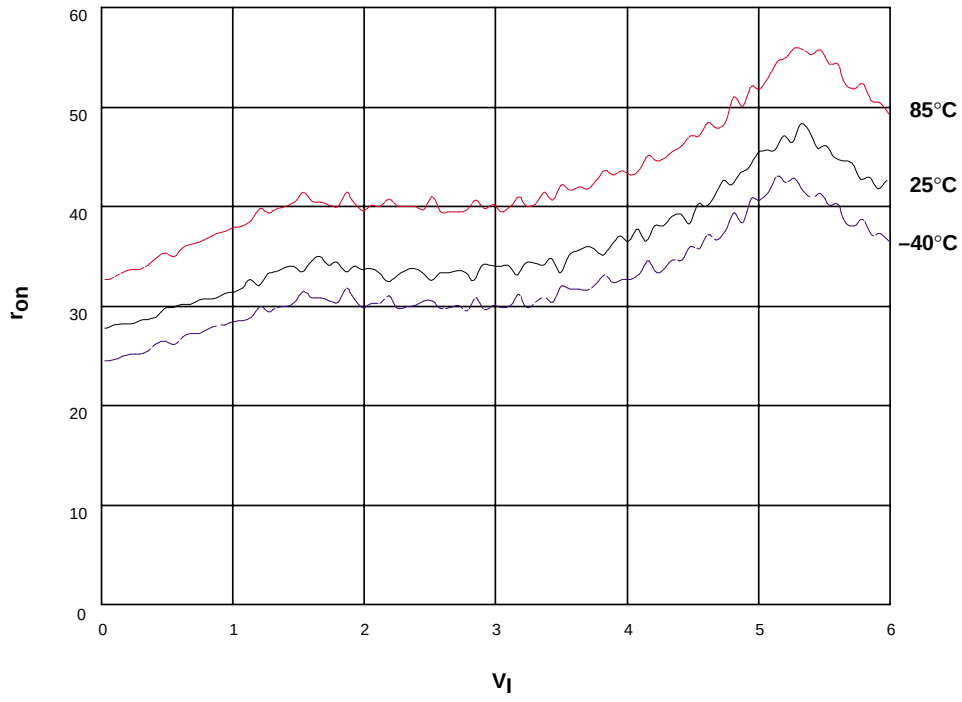


Figure 23. r_{on} vs V_I, V_{CC} = 6 V (SN74HC4066)

Table 10. SN74HC4066 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion	Crosstalk		Charge Injection‡	Feedthrough
		1 kHz	Between Switches	Enable to Output		
2 V	N/A	N/A	N/A	N/A	3.8 pC	N/A
4.5 V	30 MHz	0.05%	–45 dB	15 mV	5.9 pC	–42 dB
6 V	N/A	N/A	N/A	20 mV	7.9 pC	N/A

† Data-sheet values for SN74HC4066, except as noted
‡ Postcharacterization measurement for SN74HC4066

2.4.9 CD4066B Characteristics

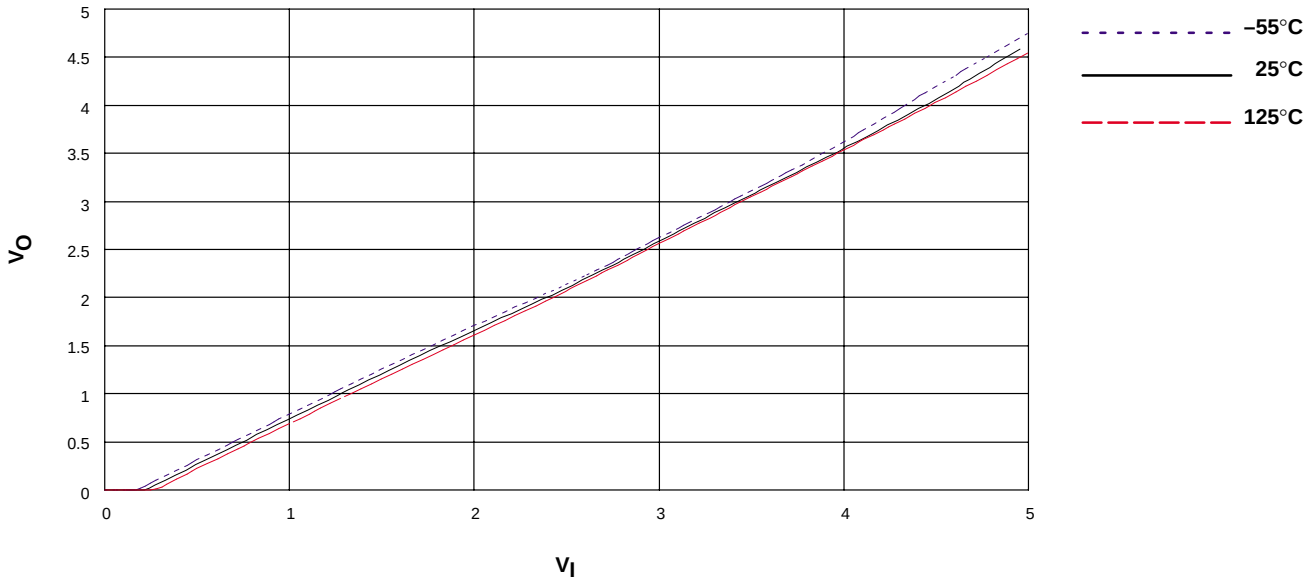


Figure 24. V_O vs V_I, V_{CC} = 5 V (CD4066B)

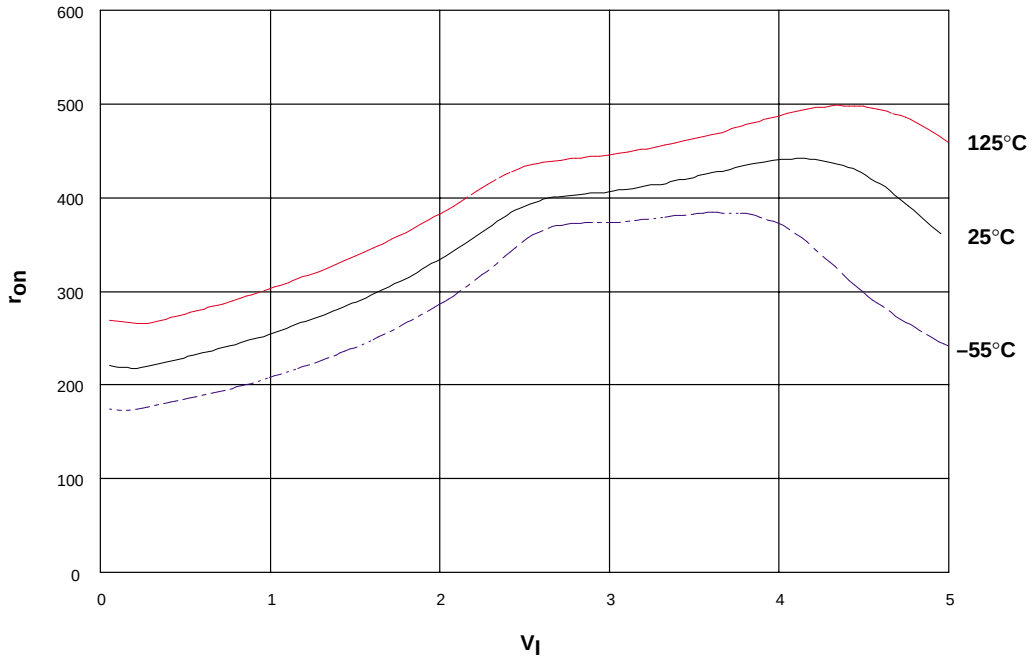


Figure 25. r_{on} vs V_I, V_{CC} = 5 V (CD4066B)

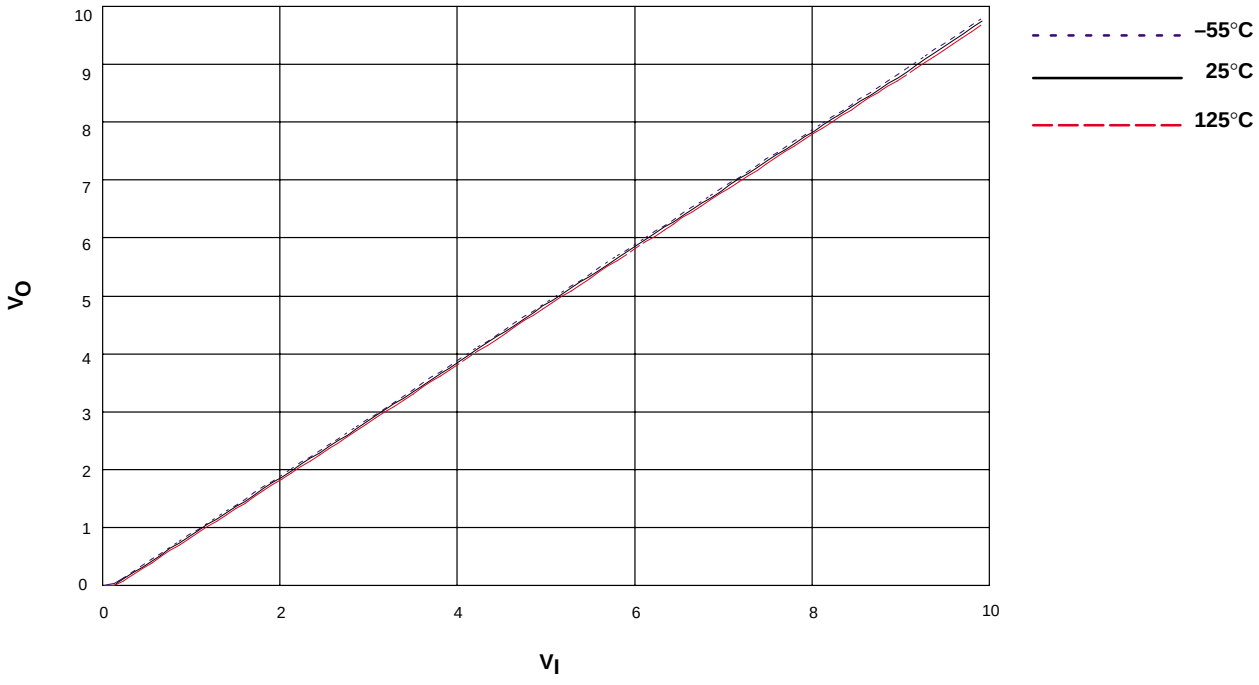


Figure 26. V_O vs V_I, V_{CC} = 10 V (CD4066B)

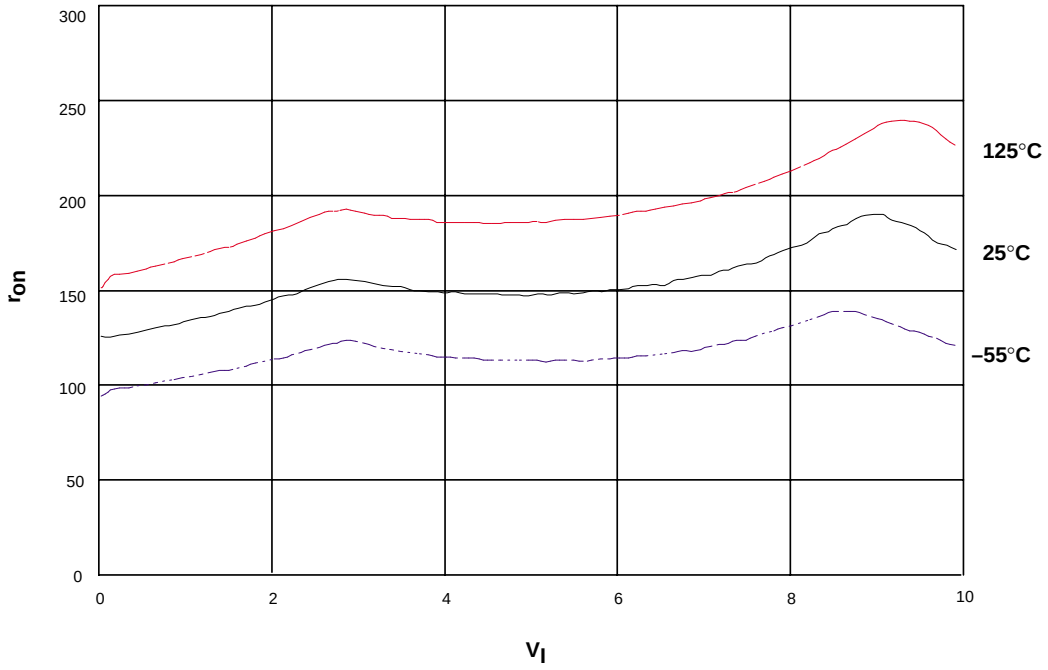


Figure 27. r_{on} vs V_I, V_{CC} = 10 V (CD4066B)

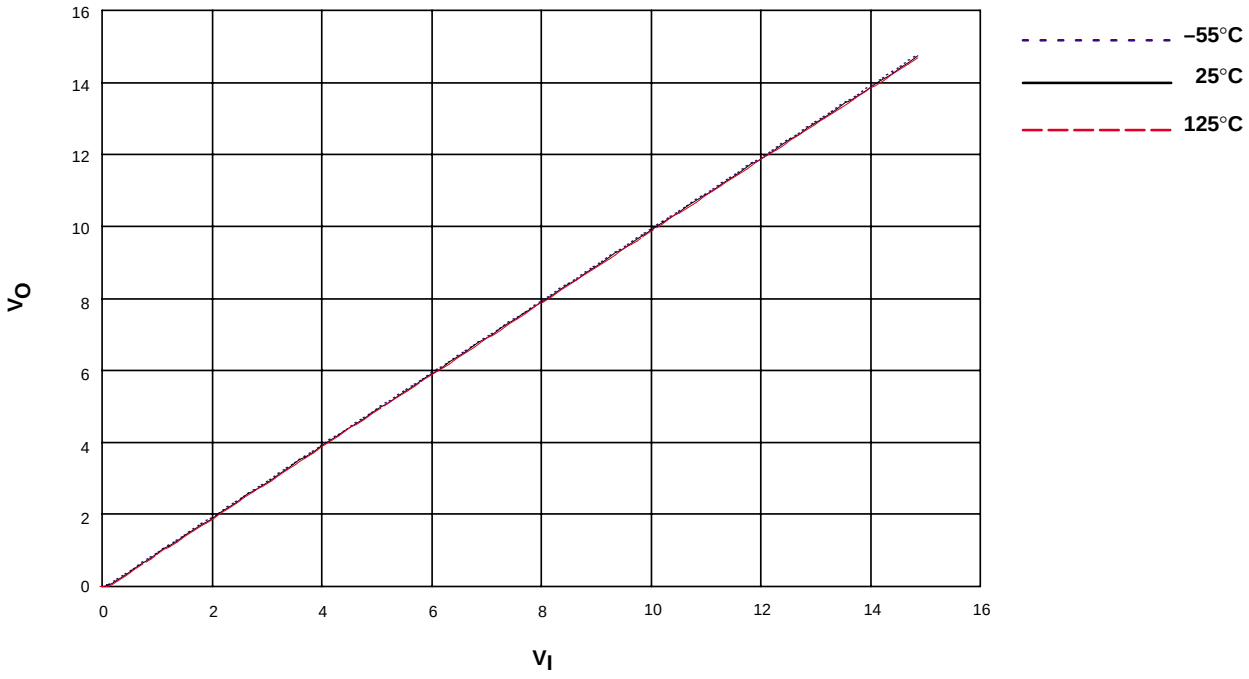


Figure 28. V_O vs V_I, V_{CC} = 15 V (CD4066B)

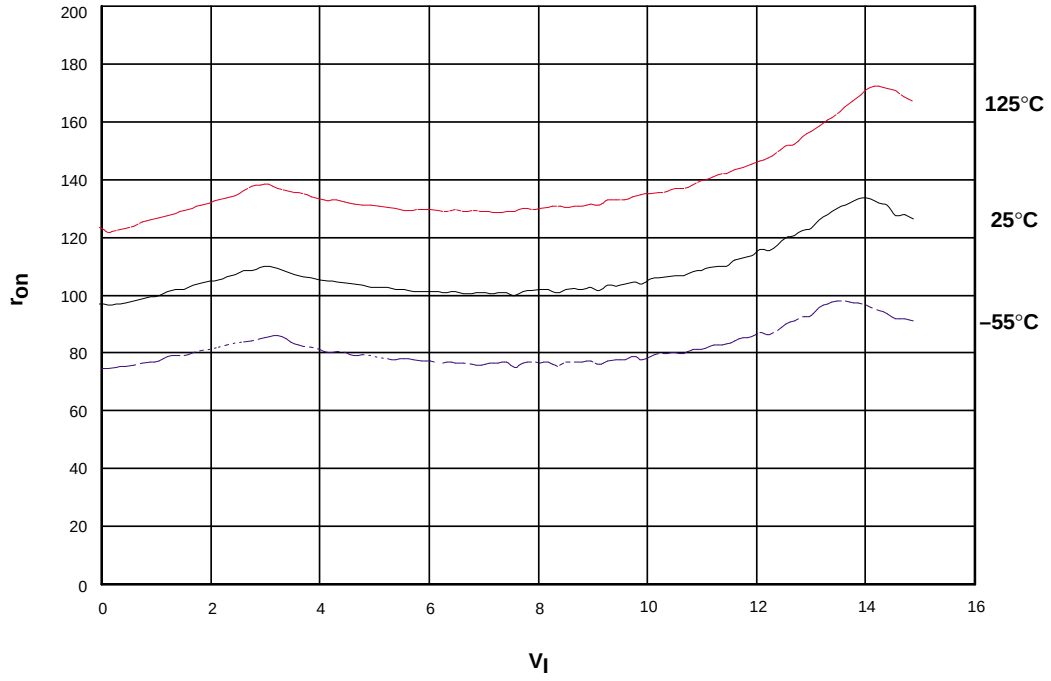


Figure 29. r_{on} vs V_I, V_{CC} = 15 V (CD4066B)

Table 11. CD4066B Analog Parameter Measurement Data†

V_{CC}/V_{SS}	Frequency Response	Total Harmonic Distortion	Crosstalk		Charge Injection‡	Feedthrough
		1 kHz	Between Switches	Enable to Output		
5 V/–5 V	40 MHz	0.04%	–50 dB at 8 MHz	50 mV		–50 dB at 1 MHz
10 V/0 V	141 MHz‡	0.032%‡	–75 dB‡	35 mV‡	18.8 pC	–65 dB‡

† Data-sheet values for CD4066B, except as noted

‡ Postcharacterization measurement for CD4066B. Frequency response, THD, crosstalk, and feedthrough measured using load conditions specified in Appendix A, in order to make a more valid comparison with other devices in this report.

2.4.10 LV-A Characteristics

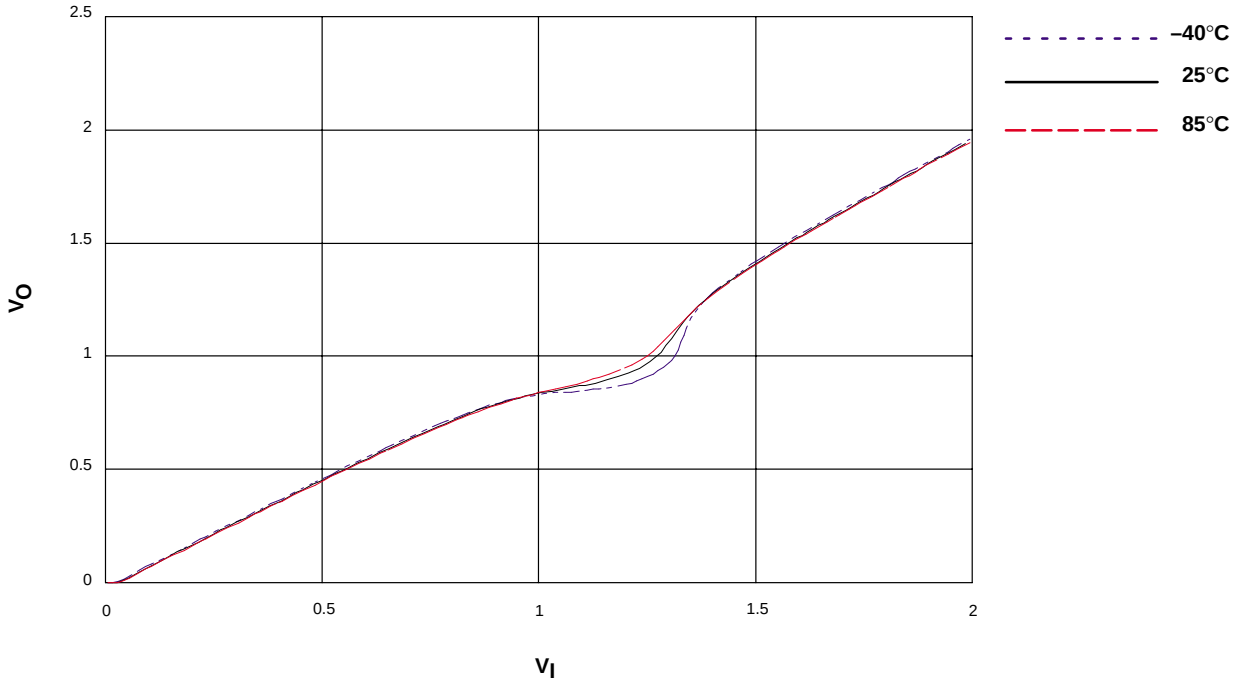


Figure 30. V_O vs V_I, V_{CC} = 2 V (SN74LV4066A)

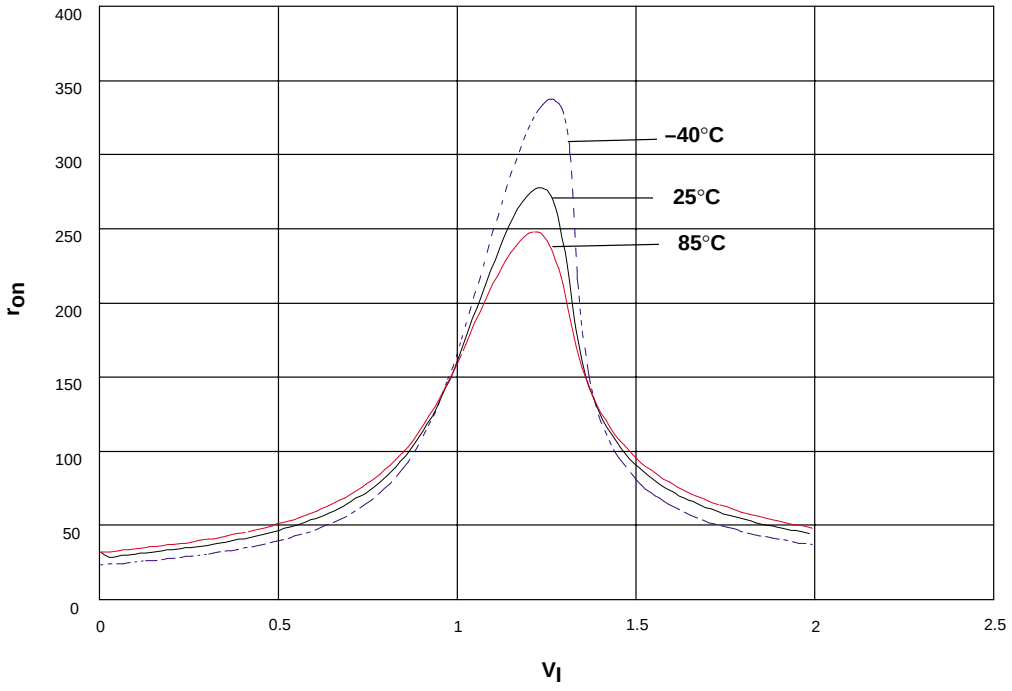


Figure 31. r_{on} vs V_I, V_{CC} = 2 V (SN74LV4066A)

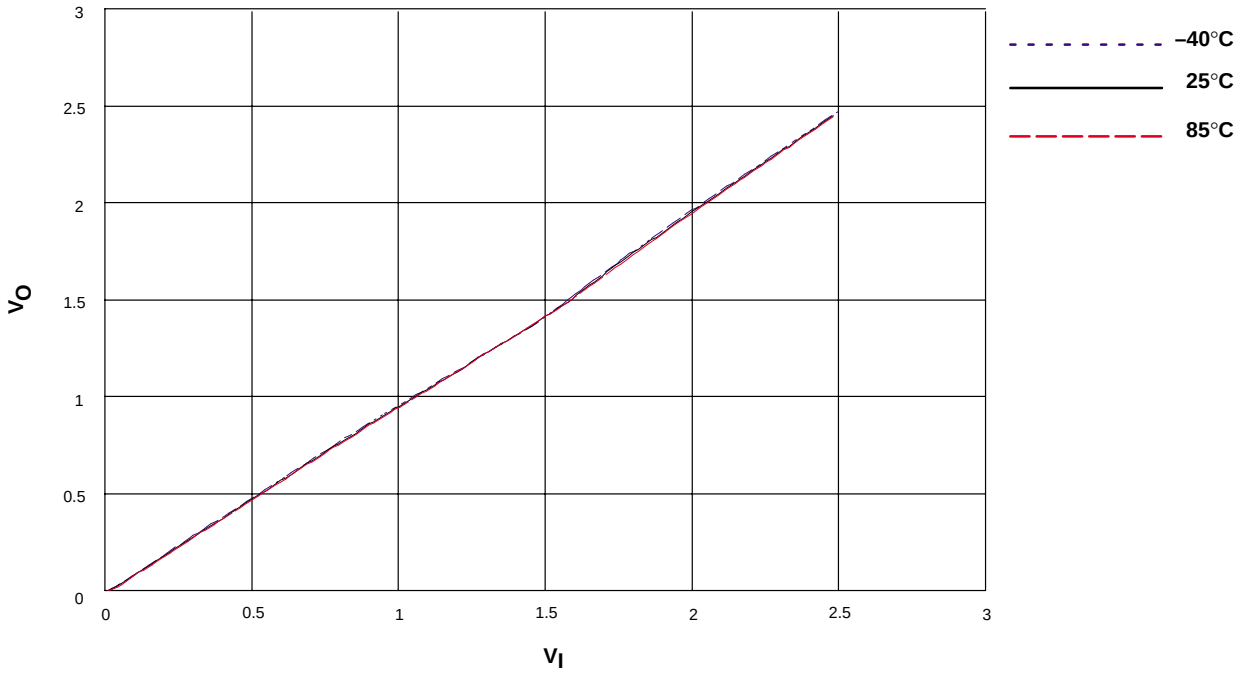


Figure 32. V_O vs V_I, V_{CC} = 2.5 V (SN74LV4066A)

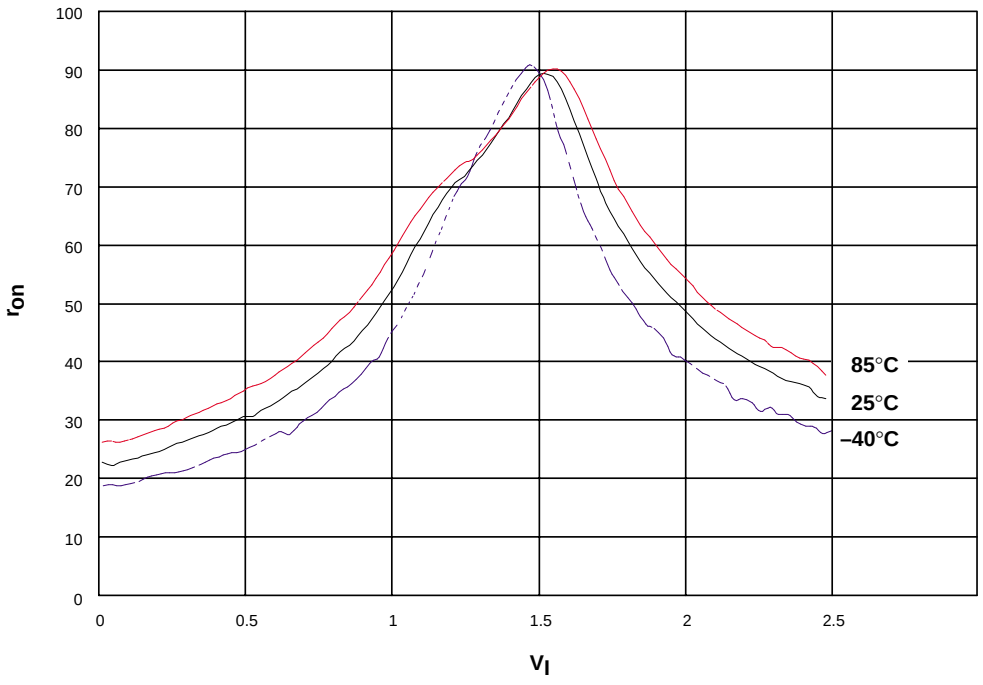


Figure 33. r_{on} vs V_I, V_{CC} = 2.5 V (SN74LV4066A)

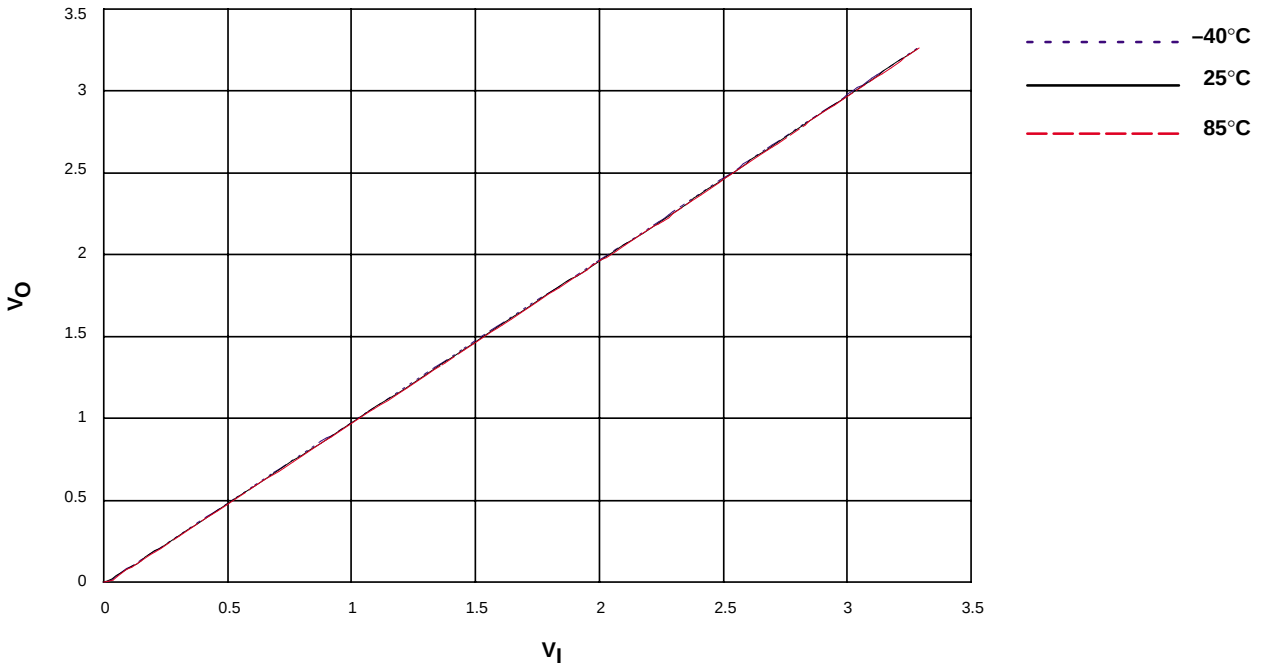


Figure 34. V_O vs V_I, V_{CC} = 3.3 V (SN74LV4066A)

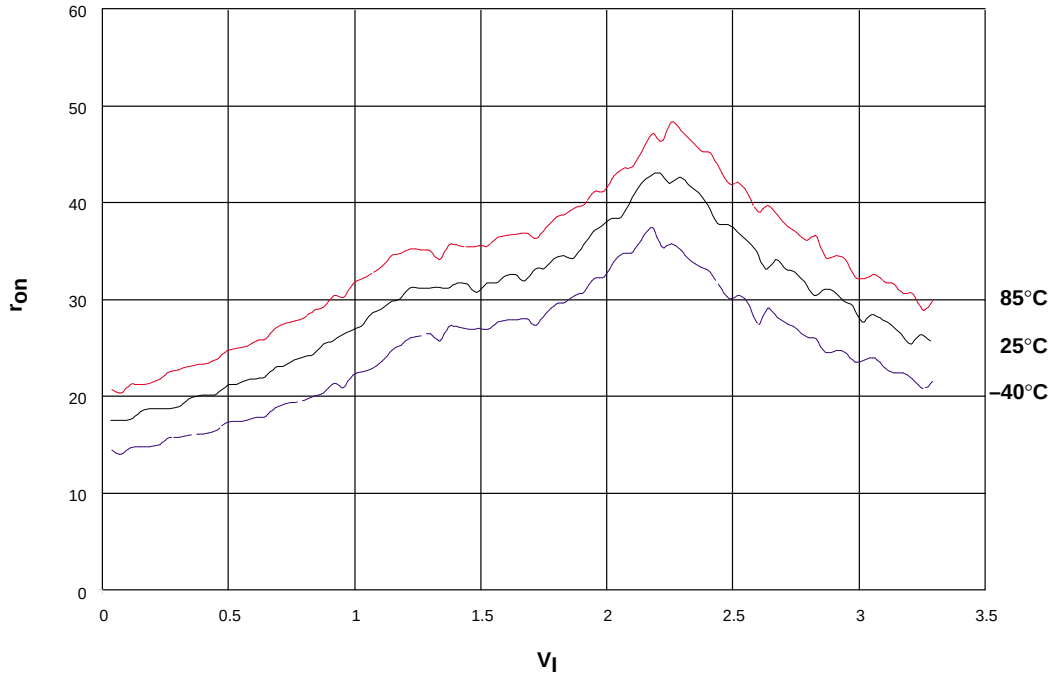


Figure 35. r_{on} vs V_I, V_{CC} = 3.3 V (SN74LV4066A)

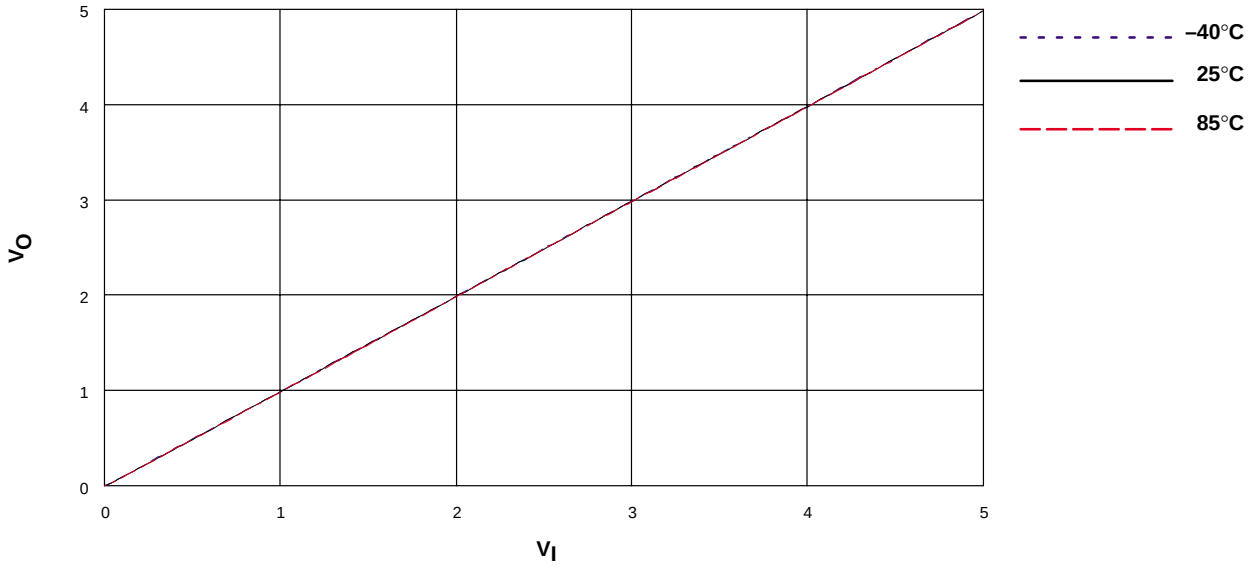


Figure 36. V_O vs V_I, V_{CC} = 5 V (SN74LV4066A)

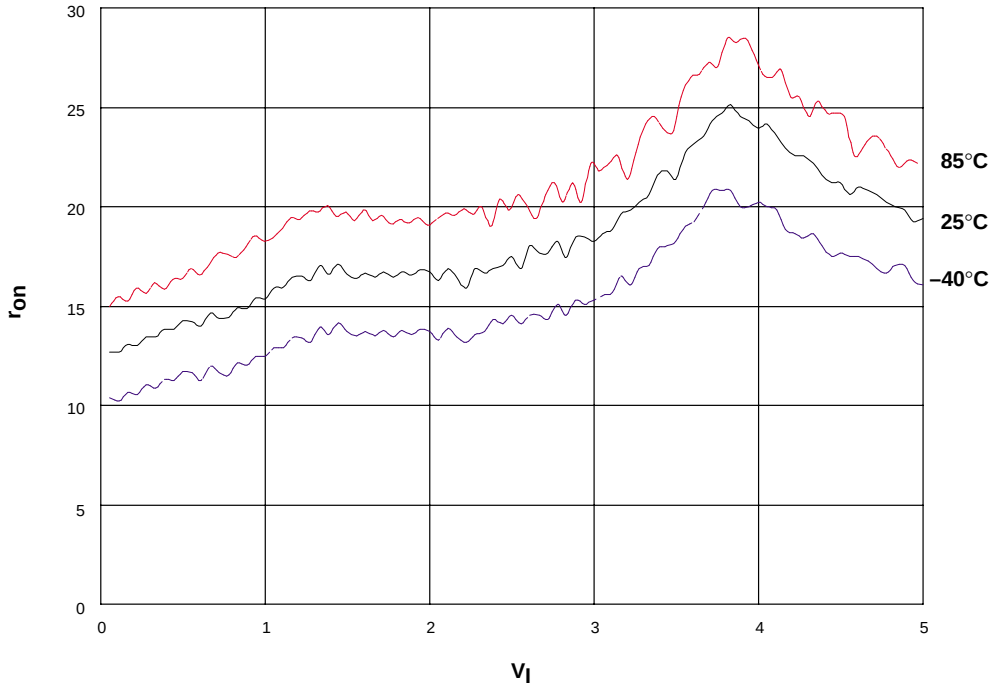


Figure 37. r_{on} vs V_I, V_{CC} = 5 V (SN74LV4066A)

Table 12. SN74LV4066A Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion	Crosstalk		Charge Injection‡	Feedthrough
		1 kHz	Between Switches	Enable to Output		
2.3 V	30 MHz	0.1%	–45 dB	15 mV	2.1 pC	–40 dB
3 V	35 MHz	0.1%	–45 dB	20 mV	2.7 pC	–40 dB
4.5 V	50 MHz	0.1%	–45 dB	50 mV	3.0 pC	–40 dB

† Data-sheet values for SN74LV4066A, except as noted
‡ Postcharacterization measurement for SN74LV4066A

2.4.11 LVC Characteristics

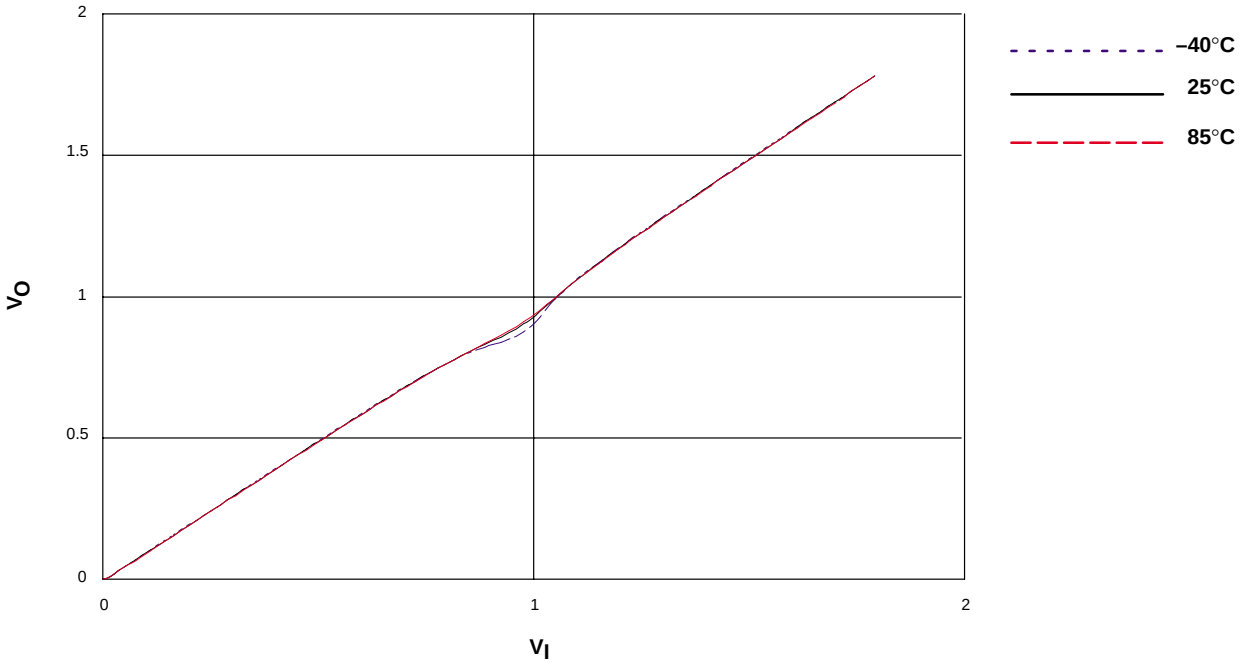


Figure 38. V_O vs V_I, V_{CC} = 1.8 V (SN74LVC1G66)

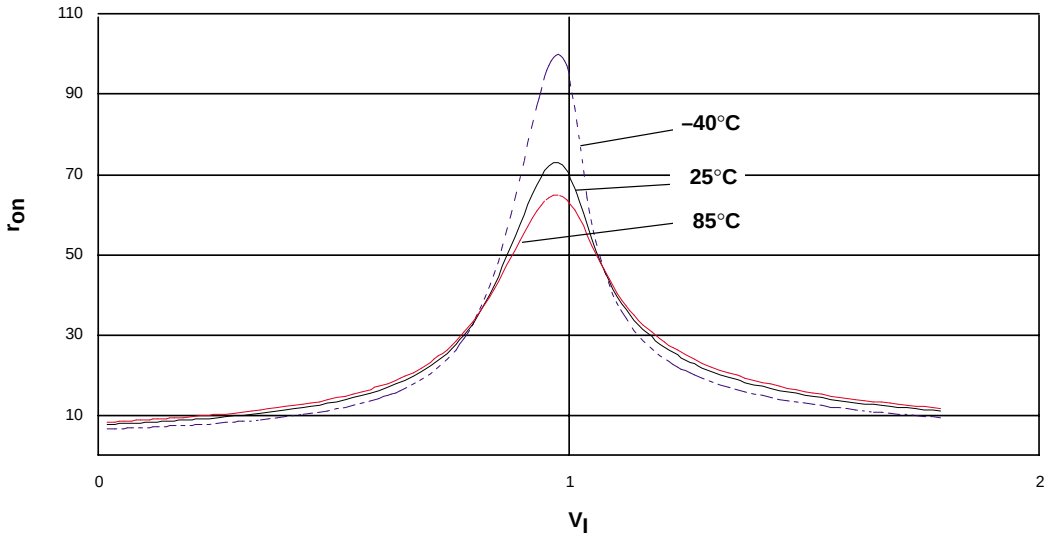


Figure 39. r_{on} vs V_I, V_{CC} = 1.8 V (SN74LVC1G66)

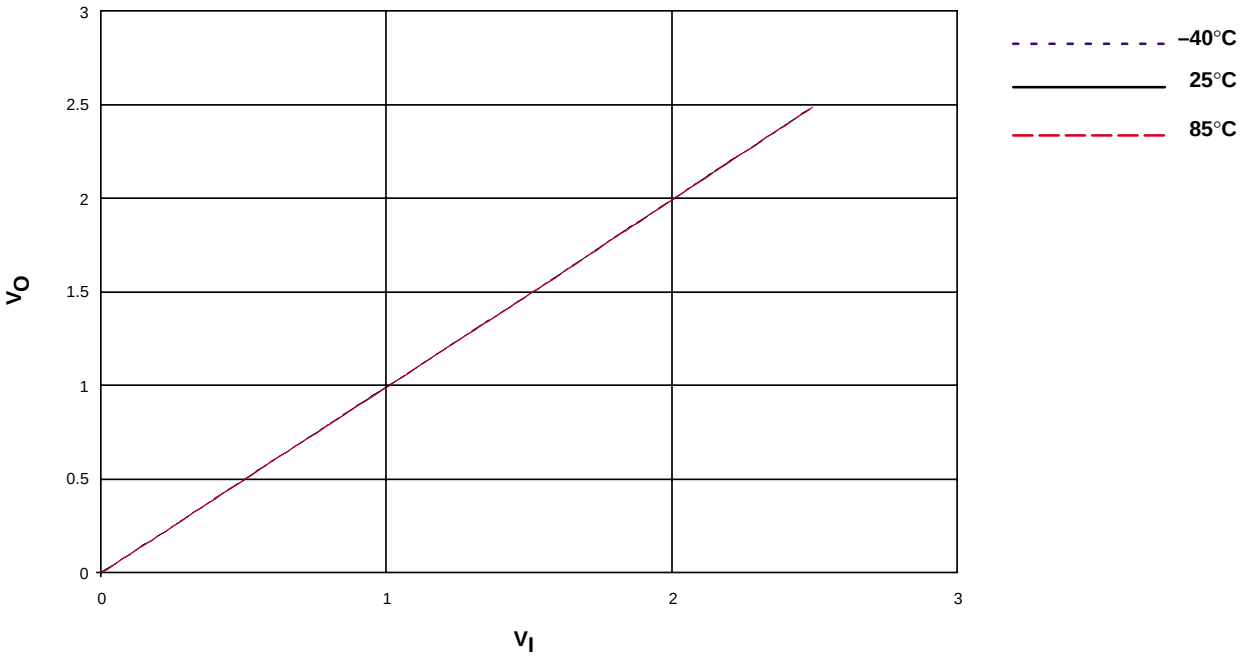


Figure 40. V_O vs V_I, V_{CC} = 2.5 V (SN74LVC1G66)

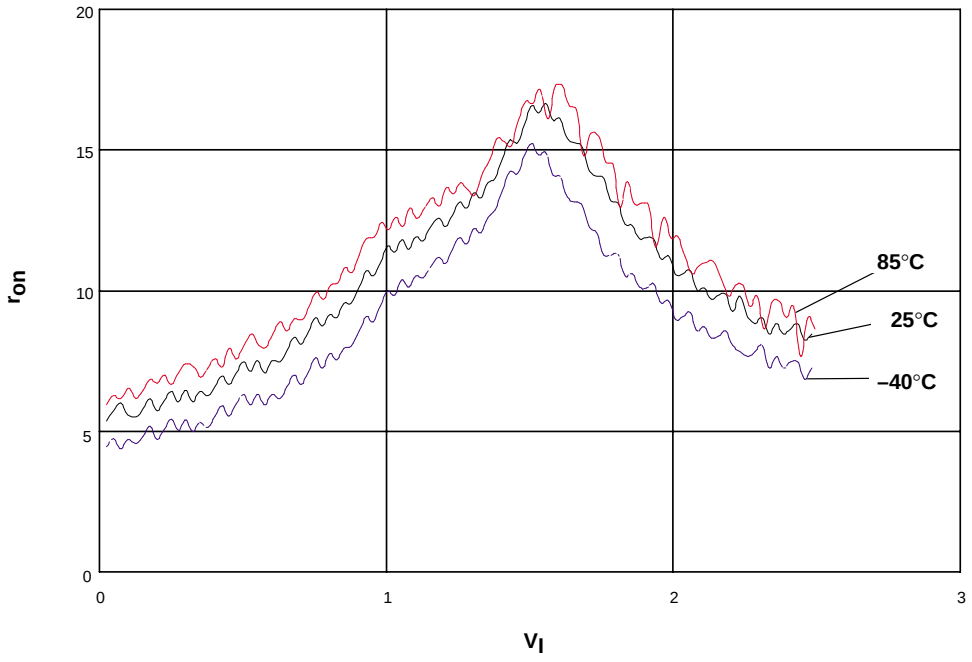


Figure 41. r_{on} vs V_I, V_{CC} = 2.5 V (SN74LVC1G66)

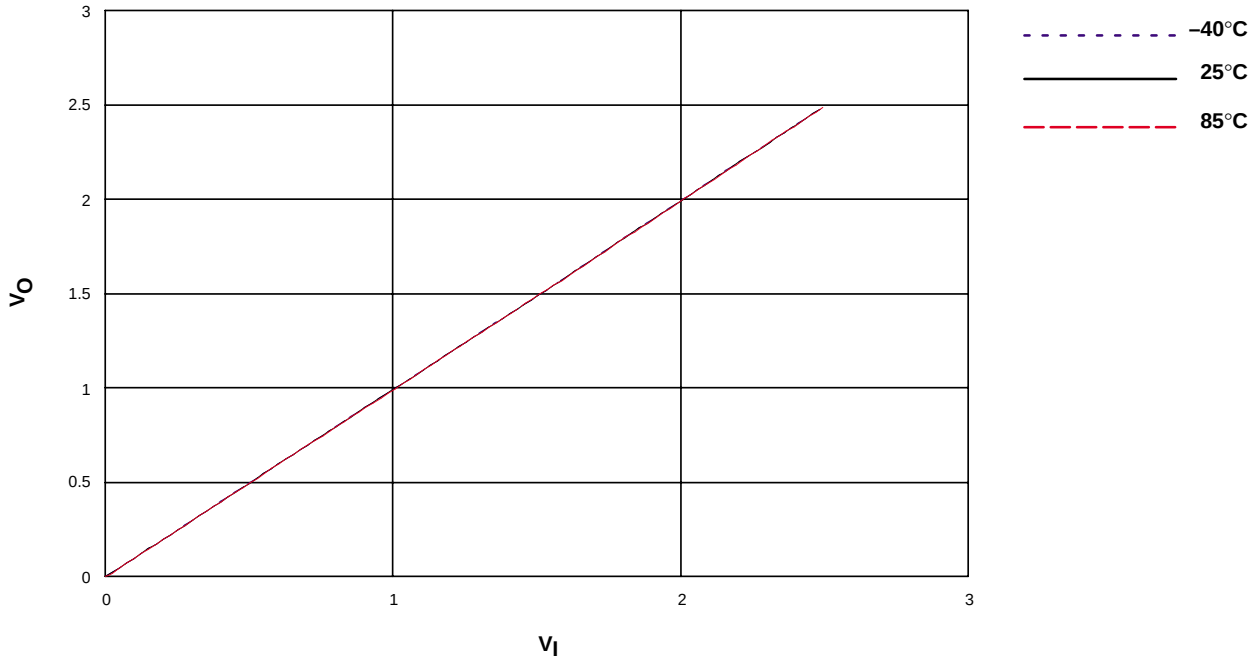


Figure 42. V_O vs V_I, V_{CC} = 3.3 V (SN74LVC1G66)

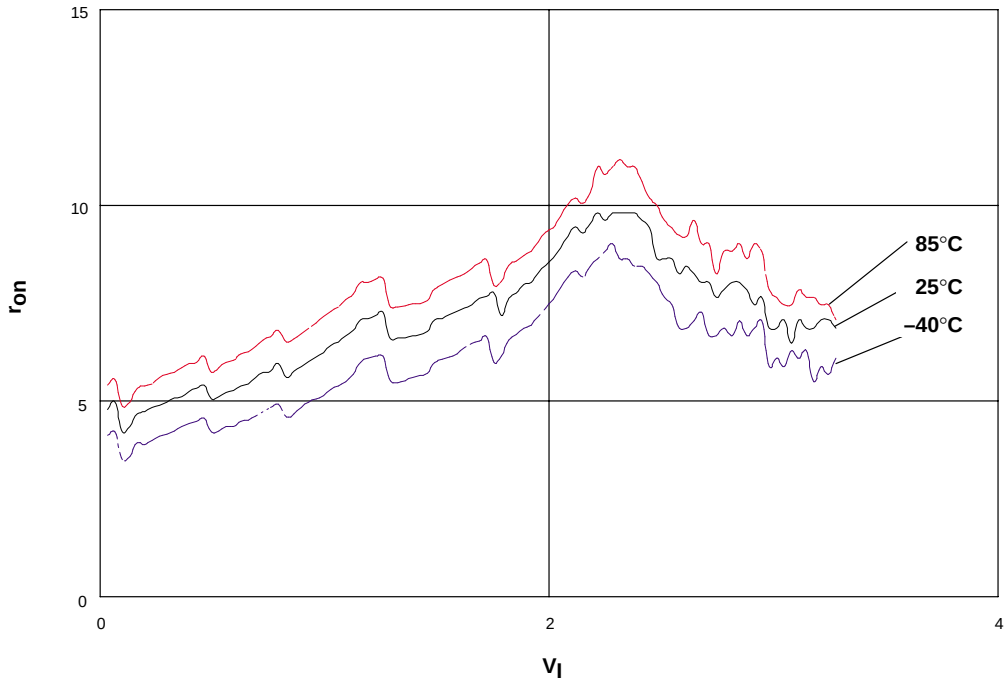


Figure 43. r_{on} vs V_I, V_{CC} = 3.3 V (SN74LVC1G66)

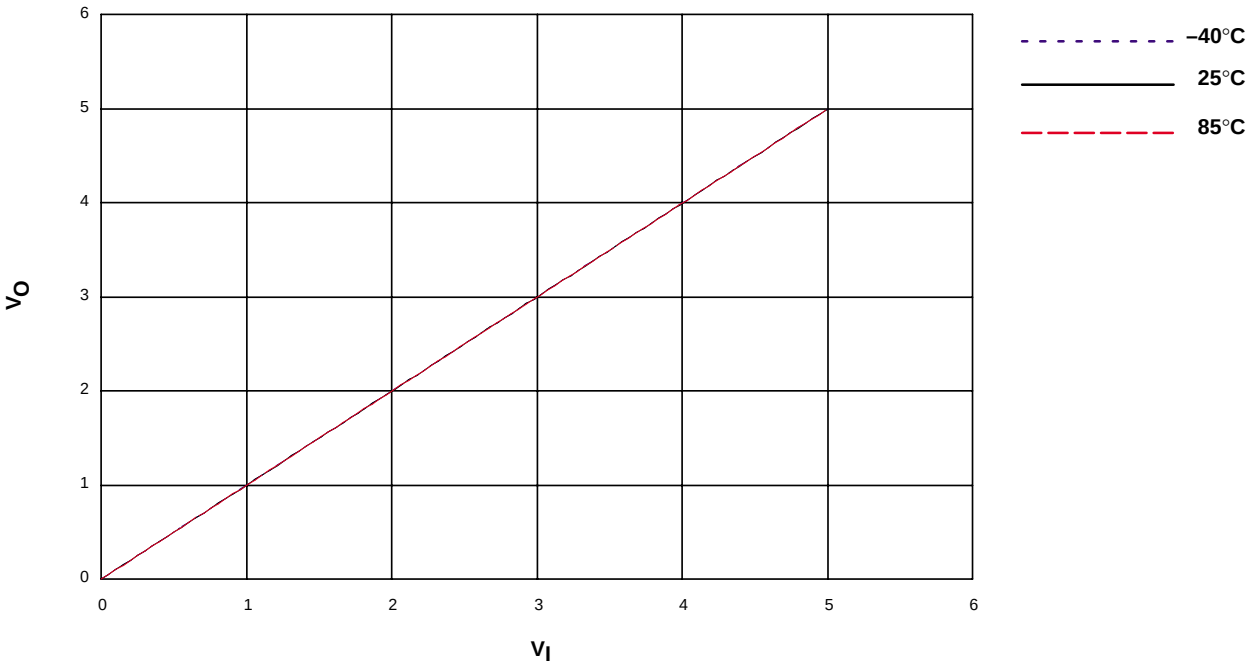


Figure 44. V_O vs V_I, V_{CC} = 5 V (SN74LVC1G66)

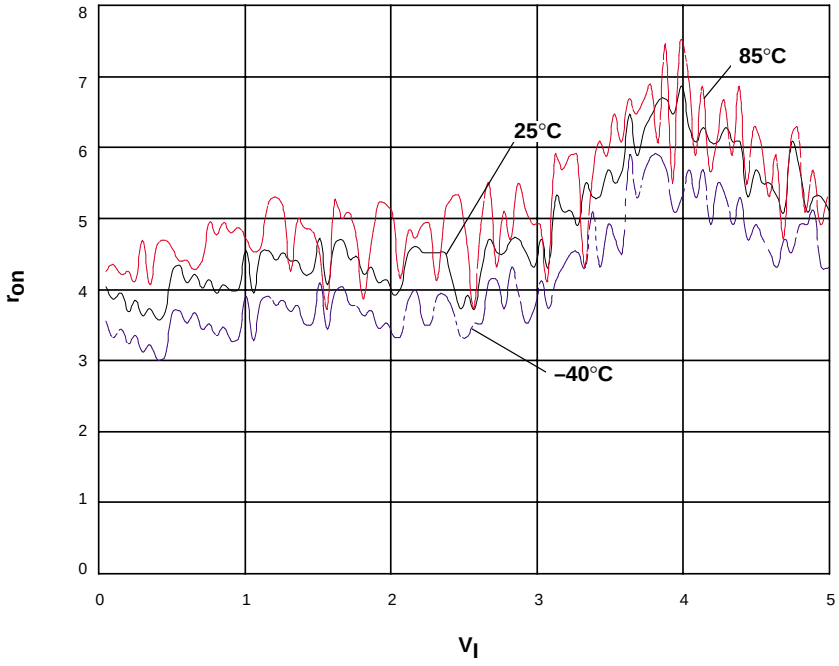


Figure 45. r_{on} vs V_I, V_{CC} = 5 V (SN74LVC1G66)

Table 13. SN74LVC1G66 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion		Crosstalk Enable to Output	Charge Injection‡	Feedthrough
		1 kHz	10 kHz			
1.8 V	35 MHz	0.1%	0.15%	35 mV	2.5 pC	–42 dB
2.5 V	120 MHz	0.025%	0.025%	50 mV	3.0 pC	–42 dB
3 V	175 MHz	0.015%	0.015%	70 mV	3.3 pC	–42 dB
4.5 V	195 MHz	0.01%	0.01%	100 mV	3.5 pC	–42 dB

† Data-sheet values for SN74LVC1G66, except as noted
‡ Postcharacterization measurement for SN74LVC1G66

2.4.12 CBTLV Characteristics

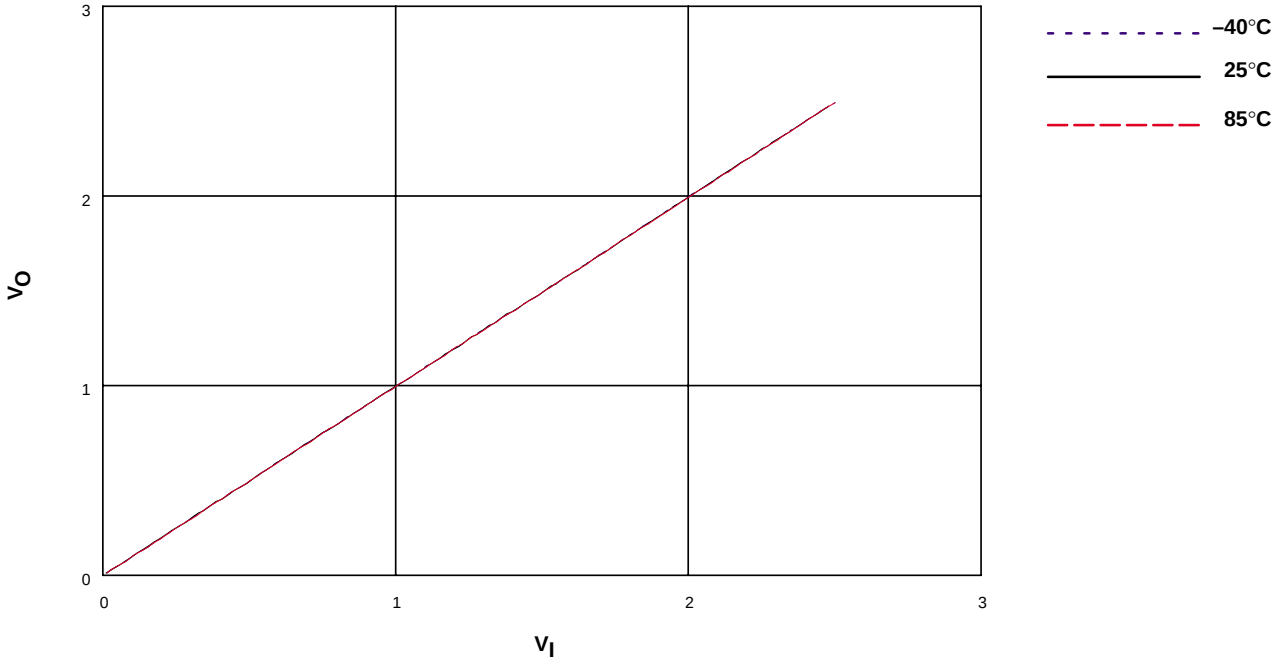


Figure 46. V_O vs V_I, V_{CC} = 2.5 V (SN74CBTLV3125)

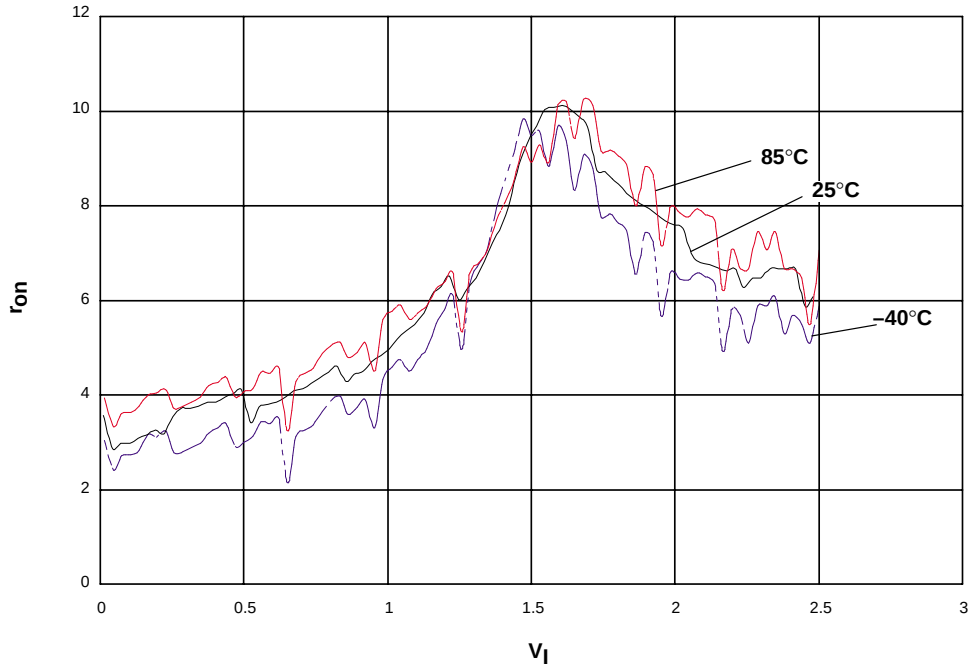


Figure 47. r_{on} vs V_I, V_{CC} = 2.5 V (SN74 CBTLV3125)

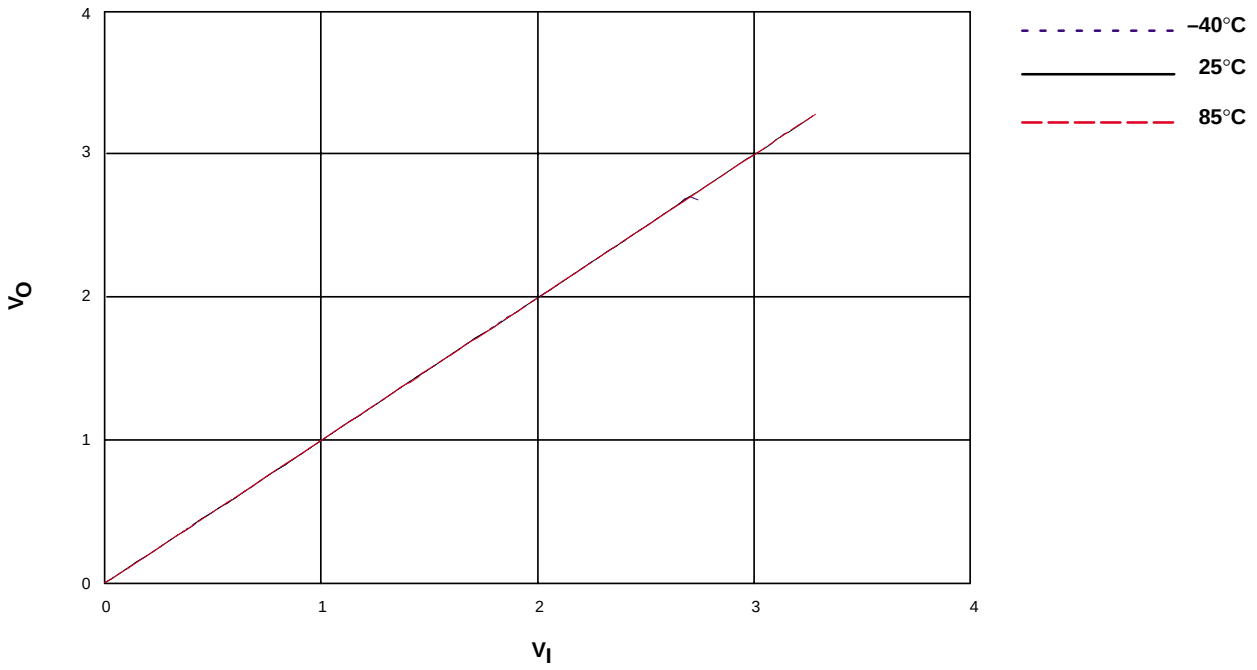


Figure 48. V_O vs V_I, V_{CC} = 3.3 V (SN74CBTLV3125)

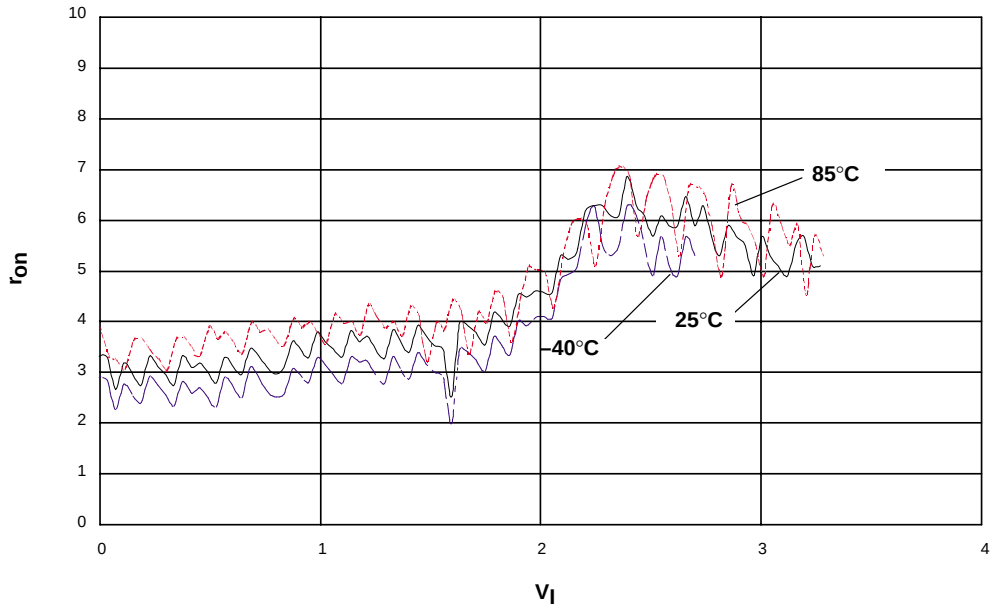


Figure 49. r_{on} vs V_I, V_{CC} = 3.3 V (SN74CBTLV3125)

Table 14. SN74CBTLV3125 Analog Parameter Measurement Data†

V_{CC}	Frequency Response	Sine-Wave Distortion	Total Harmonic Distortion	Crosstalk		Charge Injection	Feedthrough
		1 kHz	1 kHz	Between Switches	Enable to Output		
2.5 V	>200 MHz	0.089%	0.11%	–45 dB	30 mV	12.1 pC	–52 dB
3.3 V	>200 MHz	0.033%	0.09%	–49 dB	70 mV	15.5 pC	–52 dB

† Postcharacterization measurement for CBTLV3125

3 Applications

TI signal switches can be configured for numerous applications. Three switches are presented here for illustrative purposes:

- A bus switch in an analog application (digital switch in an analog application)
- Improvement of off-isolation characteristics with a T configuration
- Single-bit level shifting with an analog switch (analog switch in a digital application)

3.1 CBT3125 as a Gain-Control Circuit [for $V_I < (V_{CC} - 2\ V)$] With LMV321

An example of the CBT3125 in a gain-control circuit is shown in Figure 50.

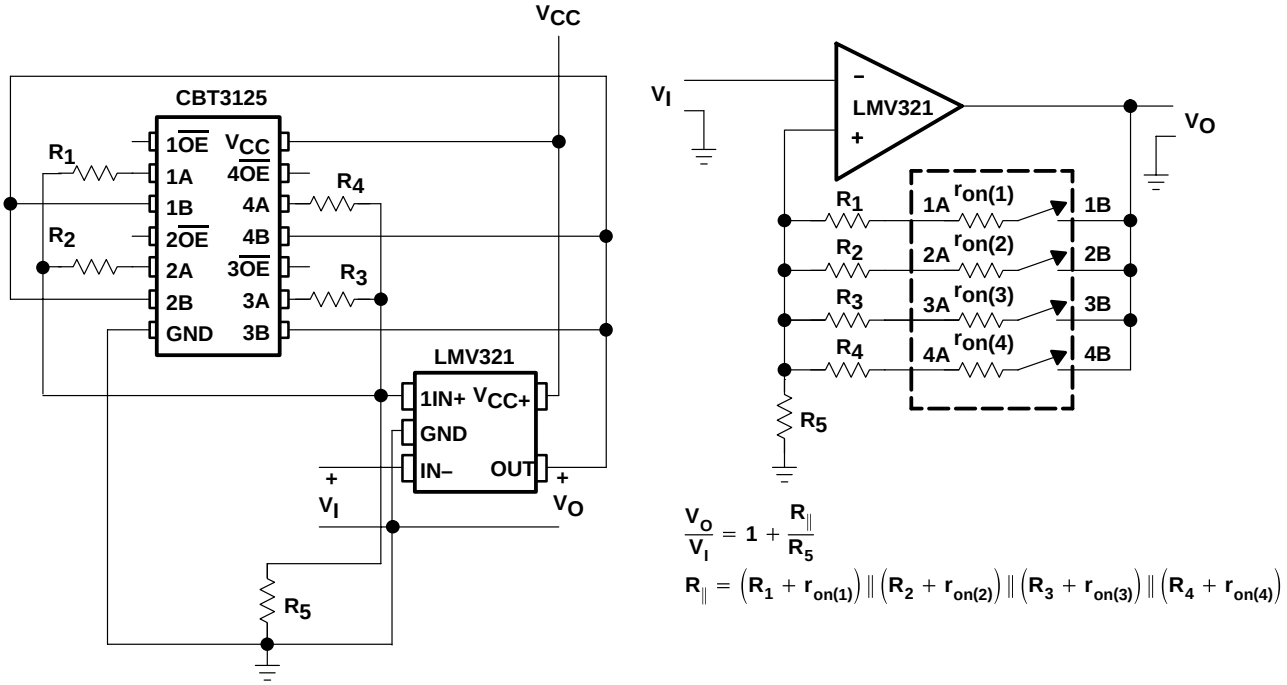


Figure 50. CBT3125 Gain-Control Circuit

By choosing values for R_1 through R_4, such that $R_X >> r_{on(x)}$, the on-state resistance of the CBT3125 can be ignored. Thus, R_{II} simplifies to:

$$R_{II} = R_1 \text{ II } R_2 \text{ II } R_3 \text{ II } R_4$$

Because the CBT device uses 5-V TTL switching levels, it can be controlled easily from either CMOS or TT logic.

3.2 LVC4066A T-Switch

The series connection doubles the effective switch r_{on} when passing signals, but the tradeoff is improved off isolation—a key concern when passing high-frequency signals. Feedthrough attenuation for the LV4066A is specified as –40 dB using a single switch. However, when connected in a T configuration as shown in Figure 51, isolation in excess of –65 dB was measured using a 5-V V_{CC}.

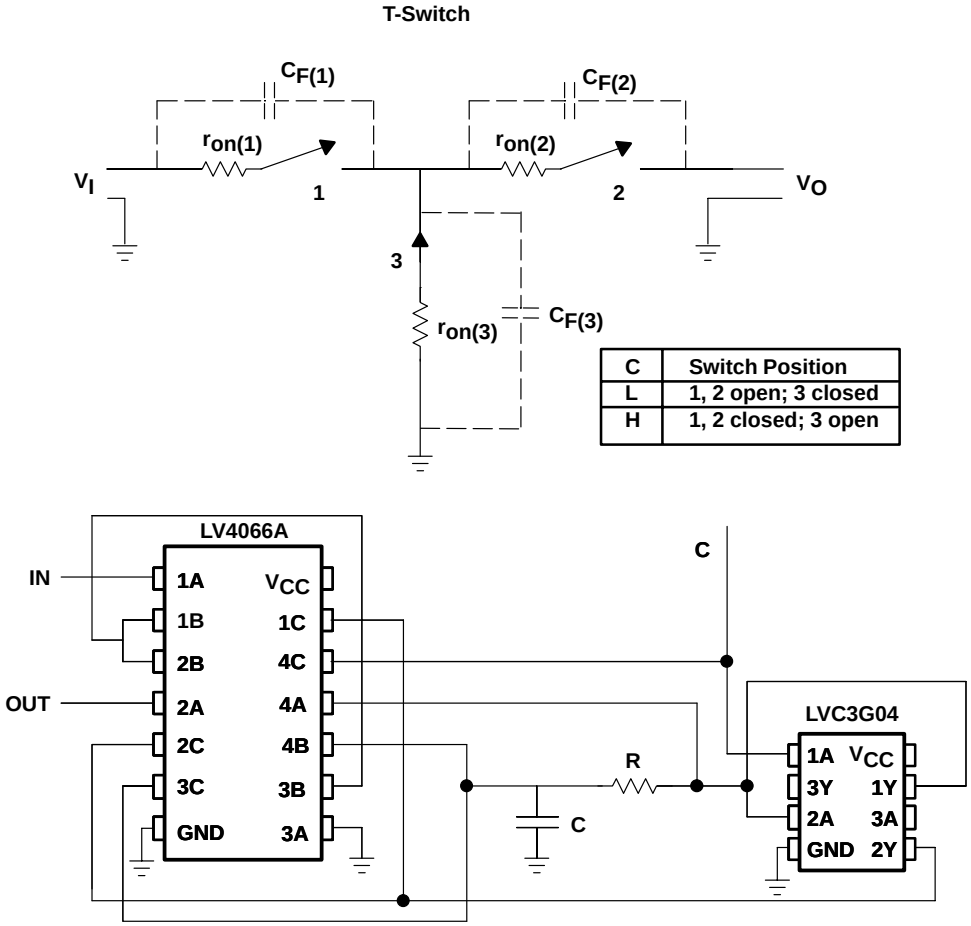


Figure 51. LV4066A/LVC2G04 T-Switch Configuration

The values of R and C (including PCB resistance and capacitance) are chosen such that the R || $r_{on(4)} \times$ C time constant is faster than the propagation delay through the inverter. This allows switch 3 to open before switches 1 and 2 close. Conversely, the R $\times$ C time constant slows the transition of the control signal to switch 3, allowing switches 1 and 2 to open before switch 3 closes.

3.3 LVC1G66 TTL-to-LVTTL Level Shifter

The LVC1G66 can be used for simple translation from 5-V TTL levels to LVTTL (see Figure 52). The control pin is tolerant to 5.5 V and, with a maximum r_{on} at V_{CC} = 3.3 V of 15 Ω, the voltage drop across the switch is only 0.36 V with 24 mA of through current.

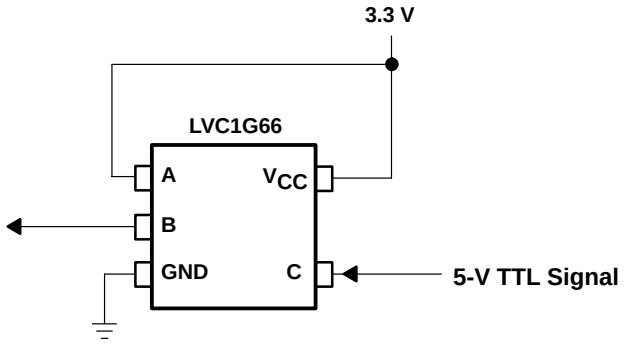


Figure 52. LVC1G66 TTL-to-LVTTL Level Shifter

4 Conclusion

Factors that go into selecting a signal switch can be numerous (analog, digital, V_{CC}, t_{en}/t_{dis}, etc.). This application report has presented the various TI signal-switch technologies (CBT, CBTLV, CD4000, HC, HCT, LV-A, and LVC), explained TI switch nomenclature, and provided example applications of switches to aid the designer in selecting the right TI signal switch.

Appendix A Test Circuits

A.1 r_{on} Measurement

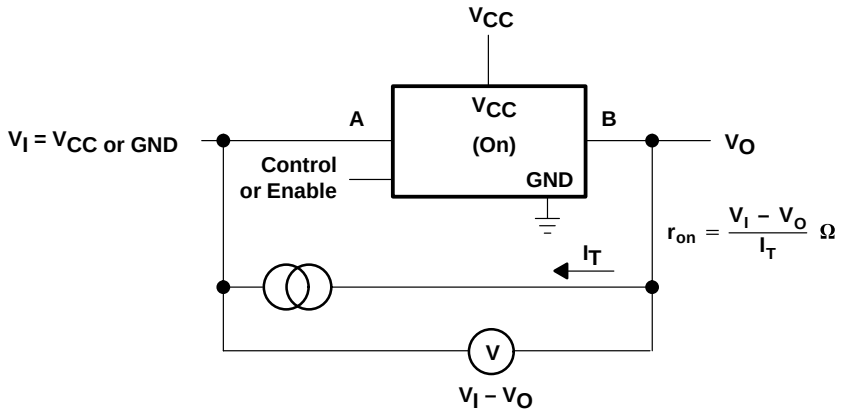


Figure A–1. r_{on} Test Circuit

A.2 V_O vs V_I Measurement

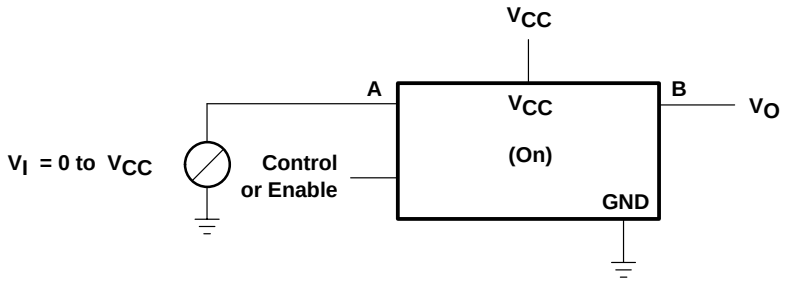
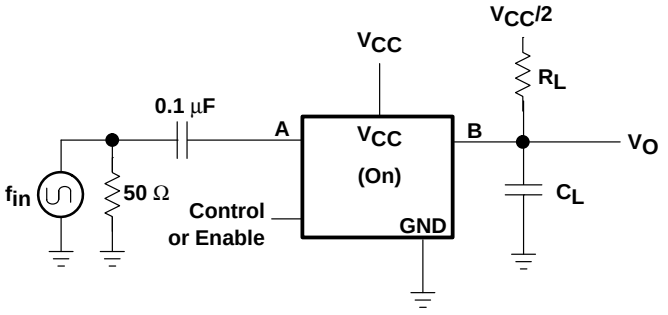


Figure A–2. V_O vs V_I Test Circuit

A.3 Frequency-Response Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	50 Ω	10 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load



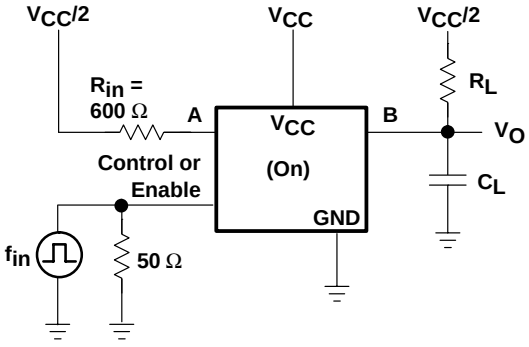
Adjust f_{in} to obtain 0 dBm at output. Increase f_{in} until dB meter reads –3 dB.

Figure A–3. Frequency-Response Test Circuit

A.4 Crosstalk Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	600 Ω	50 pF
CD74HC4066	600 Ω	50 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	10 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load



f_{in} = 1 MHz (square wave)

Figure A–4. Crosstalk (Switch Control to Output) Test Circuit

A.5 Charge-Injection Measurement

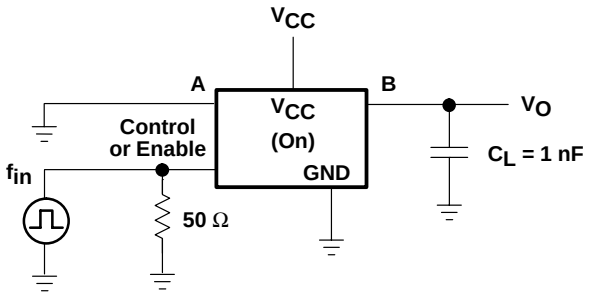
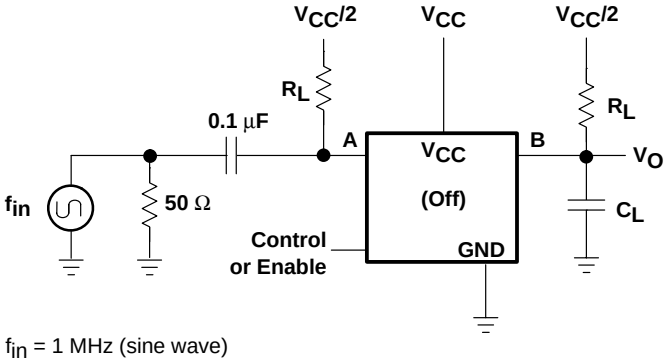


Figure A–5. Charge-Injection Test Circuit

A.6 Feedthrough Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 Ω	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	50 Ω	10 pF
SN74HC4066	600 Ω	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 Ω	50 pF
SN74LV4066A	600 Ω	50 pF
SN74LVC1G66	600 Ω	50 pF
SN74CBTLV3125	600 Ω	50 pF

† Data-sheet load
‡ Application-report load



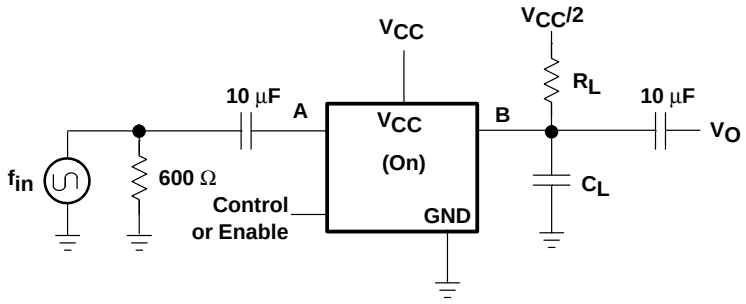
f_{in} = 1 MHz (sine wave)
Adjust f_{in} to obtain 0 dBm at input.

Figure A–6. Feedthrough Test Circuit

A.7 Sine-Wave and Total-Harmonic-Distortion Measurement

DEVICE	R_L	C_L
SN74CBT3125	10 kΩ	50 pF
CD74HCT4066	10 kΩ	50 pF
CD74HC4066	10 kΩ	50 pF
SN74HC4066	10 kΩ	50 pF
CD4066B†	10 kΩ	–
CD4066B‡	10 kΩ	50 pF
SN74LV4066A	10 kΩ	50 pF
SN74LVC1G66	10 kΩ	50 pF
SN74CBTLV3125	10 kΩ	50 pF

† Data-sheet load
‡ Application-report load



f_{in} = 1 kHz (sine wave)

Figure A–7. Sine-Wave and Total-Harmonic-Distortion Test Circuit

A.8 Crosstalk-Between-Switches Measurement

DEVICE	R_L	C_L
SN74CBT3125	600 kΩ	50 pF
CD74HCT4066	50 Ω	10 pF
CD74HC4066	10 kΩ	50 pF
SN74HC4066	600 kΩ	50 pF
CD4066B†	1 kΩ	–
CD4066B‡	600 kΩ	50 pF
SN74LV4066A	600 kΩ	50 pF
SN74LVC2G66	600 kΩ	50 pF
SN74CBTLV3125	600 kΩ	50 pF

† Data-sheet load
‡ Application-report load

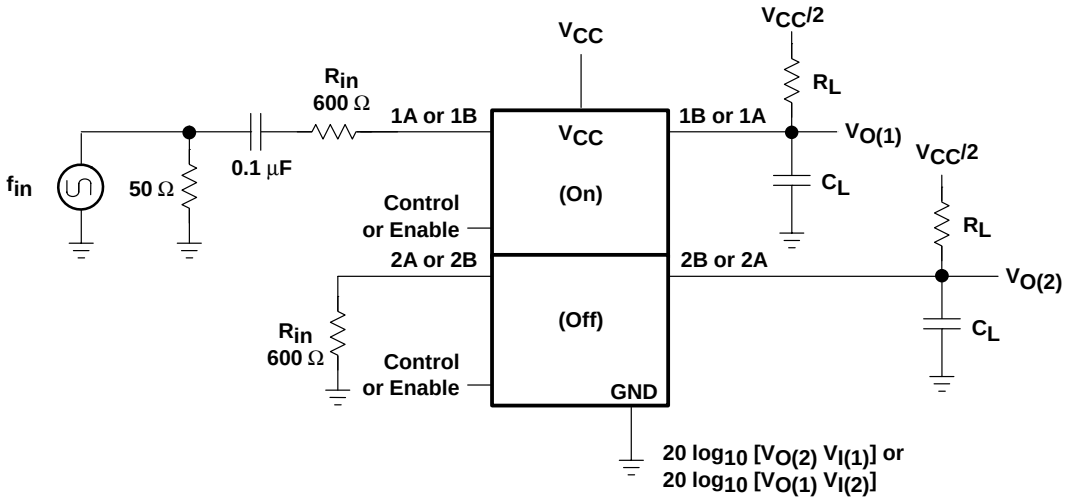


Figure A–8. Crosstalk-Between-Switches Test Circuit

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